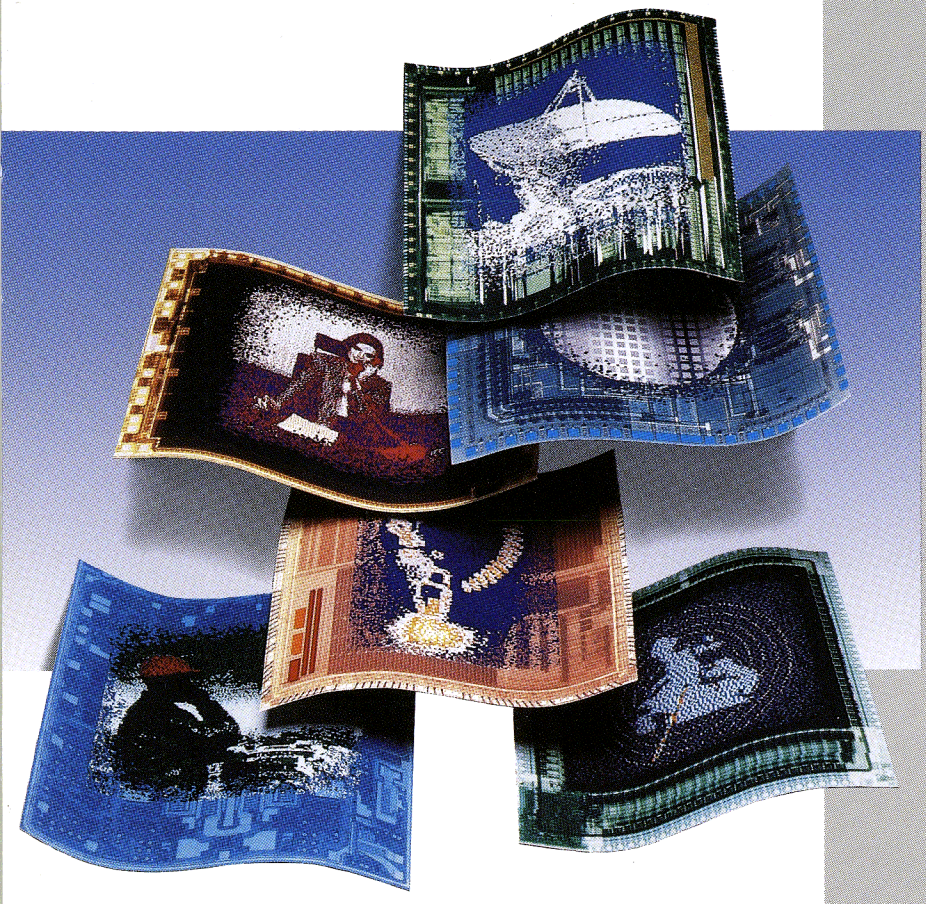
SOS Radiation Hard

Hi-Rel IC and ASIC Handbook



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SOS Radiation Hard Hi-Rel IC and ASIC Handbook

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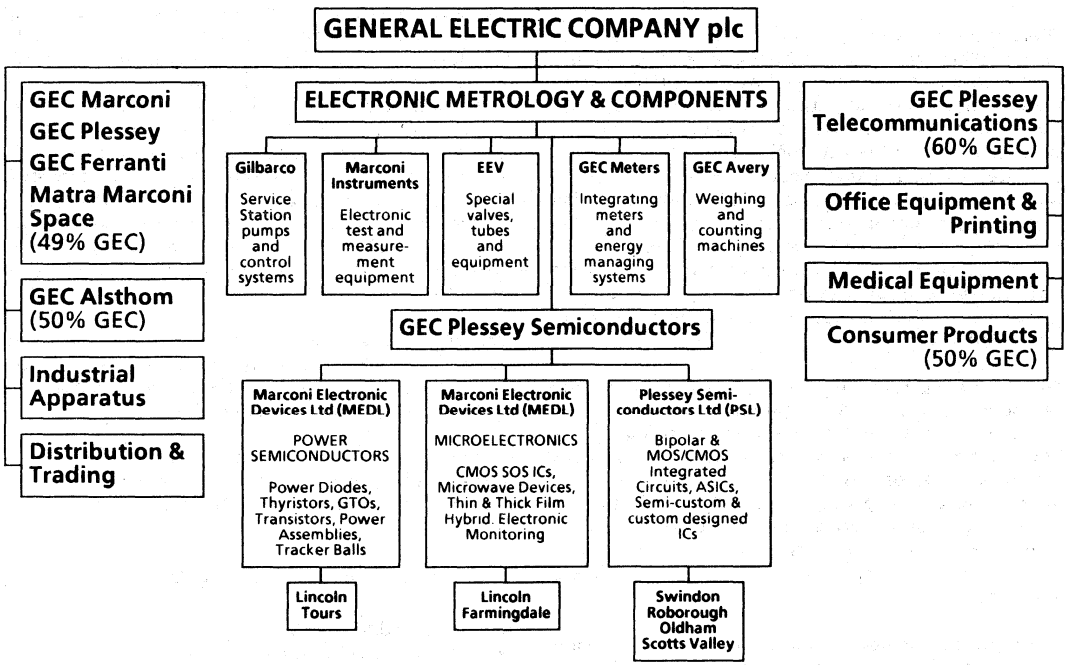
INTRODUCTION



The General Electric Company plc

GEC Plessey Semiconductors (GPS) is part of the General Electric Company plc (GEC), which is a wholly British Company. GEC is one of the largest electronics and electrical engineering organisations in the world and, with 160,000 employees is one of the largest UK employers.

GEC Plessey Semiconductors (GPS)

GPS was formed from the merger of the activities of Marconi Electronic Devices Limited (MEDL) and Plessey Semiconductors Limited (PSL). The company has 7 manufacturing sites worldwide and employs nearly 4000 people. Products include Standard products and ASICs in Bipolar and BULK/CMOS, Hybrid components, Microwave components, Power Semiconductors and CMOS-SOS Rad Hard Integrated Circuits.

CMOS-SOS Integrated Circuits

The Lincoln based Integrated Circuit operation produces specialist circuits for the space, defence and communications markets. The operation employs over 500 people with a very high percentage of graduate level engineering staff.

This IC facility manufactures product for direct sale to end customers and also to other parts of the organisation, where further integration results in more complex products.

The IC facility carries out all manufacturing from design to product shipment in Lincoln, England. In certain cases, packaging is subcontracted.

Silicon on Sapphire Technology

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Radiation Hard Silicon on Sapphire

There is an increasing demand for space and defence systems which can survive radiation effects and ensure continued operation. As satellites and space probes mature, microprocessors, static RAMS, gate arrays and other VLSI ICs with the ability to carry out complex data processing tasks in the extremely stringent environment of space become essential. Space imposes its own set of requirements, demanding a hardness to radiation which is normally screened out by the atmosphere. This radiation, in the form of cosmic rays, electrons, protons and x-rays, alters the electrical characteristics of circuits and causes a degradation in integrated circuit performance, which can lead to catastrophic device and system failures.

Of all the current silicon-based semiconductor technologies, only CMOS SOS (silicon-on-sapphire) offers the necessary resistance to the hazards of single event upset, transient and total dose radiation. It also provides the advantages of low power consumption and fast internal switching speeds, making CMOS SOS the key technology for defence and space applications. Independent investigators consider that its SEU immunity makes it the only choice for many key space applications.

The company has been involved in SOS research and development for more than 15 years and is committed to the long term support of SOS processes and products for space and defence applications. Process and design techniques are in unison to maximise the benefits of the technology.

Initial research and development on SOS began at the GEC Hirst Research Centre in 1973. This work continued through to pilot designs which were released in 1979/1980. With the formation of Marconi Electronic Devices in 1981, manufacturing was transferred to the Lincoln facility and the 5 micron process attained full production status in 1982. Development work progressed to achieve smaller geometries and increased radiation hardness. A 3 micron process was established in 1984 and a double level metal variant of this process went into production in 1986. A 2.5 micron variant was introduced in 1989. A 1.5 micron process is now being used to manufacture memories and semicustom products.

Production processes are based on in-house developed silicon on sapphire technology with drawn gate lengths of 5, 3, 2.5 and 1.5 micron. Both single and double level metal technologies are now available.

A range of standard products and semicustom capabilities have been developed to provide all the key elements required in space and defence systems.

SOS Radiation Hardness Summary (1.5 micron)

Total Dose [Rad(Si)] Digital	$>10^6$
Dose Rate Survive [Rad(Si)/S]	$>10^{12}$
Dose Rate Upset [Rad(Si)/S]	$>10^{11}$
Single Event Upset [Errors/Bit day]	$<4\times10^{-11}$
Neutrons [Neutron/cm2]	10^{15}
Latch up	not possible

SOS Performance Summary (1.5 micron)

Transistor Count	>400 K
Toggle Frequency	>100 MHz
Gate Delay	<1.0ns
Pin Count	>200
Power	<1 μW/MHz/Gate

The Lincoln wafer fabrication facility was established in 1981 and has been substantially extended and enhanced to its current capacity of 2500 wafer starts per week. A range of bulk silicon CMOS and CMOS-SOS processes are run in the facility covering feature sizes from 5 to 1.5um. Wafer size is 4 in. At present approximately 30% of the wafer throughput is SOS. This share is increasing.

All manufacturing groups operate on a 24 hour per day, 3 shift basis producing ASICs, memory circuits and microprocessors up to space standards. All manufacturing processes are controlled by means of a computer-aided manufacturing system (PROMIS) which extends through wafer fab, assembly, and test. Extensive use is made of this system to collect wafer related engineering data which is then processed using statistical software packages.

Facilities

Integrated manufacturing facilities consist of 17,000 sq ft of wafer fabrication clean room (with separate areas for manufacturing and development), 9000 sq ft of assembly floor (part Class 100 clean room), a 6000 sq ft test floor and 2000 sq ft of characterization area. Additional laboratory space is provided for functions such as product engineering.

The wafer fabrication area is primarily built to Class 100 standards with 200 sq ft of Class 10 area which is utilized for the critical steps in the 1.5 um SOS process and development programs on 1.0 um technology. These areas are environmentally controlled to temperature control limits of ± 0.5°C and humidity control of ± 2.5%. Particulate counts indicate an environment which is close to Class 1. Utilities installations are to an appropriate standard with all process gases run in continuously welded stainless steel lines using purifiers and point of use filtration as appropriate. A high purity de-ionizing water ring main is provided for 1.0 um geometry processes.

Continuous monitoring of many facility parameters is carried out by a computer based building management system and this provides the ability to datalog and generate trend data for these parameters. Where appropriate these measurements are backed up by manual measurement such as bacteria counts, carried out on a regular basis in the DI water system.

Computer Aided Manufacture

The PROMIS computer aided manufacturing system is used to define all process flows and to track material through development and mainstream manufacturing.

By this method it is possible to cope with a wide variety of process flows with minimal risk of human error and also to provide a high degree of visibility of batch status to anyone within the 400 strong user group. A natural consequence of the use of PROMIS is total traceability of material from incoming material to finished devices.

Product Assembly

The assembly capability is contained within the Lincoln (UK) facility except for plastic encapsulation (offshore) and tin plating (Power Division, Lincoln). The preseal assembly facility is enclosed in cleanroom conditions. Space products have been isolated in their own module to provide additional focus on these high quality components. The area offers total facilities for military and space manufacture of integrated circuits on one site. Current product being produced to these levels of quality include static RAMS, MIL-STD 1750 processors, standard logic circuits, MIL-STD-1553 databus products, and ASICs.

The present capacity of this assembly area is 10,000 units per week with approximately 1K available for space grade product. Expansion over the next 12 months will increase the space capacity to 2K units per week. The area also offers an engineering quick turnaround route for development prototypes and engineering experiments.

The assembly area has facilities for the production of bulk silicon CMOS and silicon on sapphire devices in numerous package styles, including custom designed packages for special applications. Current capability includes:

Dual in line - Sidebrazed and Cerdip, Leaded Flatpack, Cerpac, Leadless Chip Carrier, Pin Grid Arrays, Cerquads (J Lead and Gullwing), and Small Outline Packages (SO).Sealing methods include solder seal with Kovar or ceramic lids, glass seal and conformal coatings.

A surface mounting facility has been established to mount Class S leadless chip carriers onto motherboards to produce 1750 processor and RAM modules.

The company offers a manufacturing flow capable of screening to MIL-STD-883C class S and B, European Space Agency and British Standard quality levels.

Basic Structures Characterisation

DC measurements can be performed on a range of test systems all with pA current and mV voltage resolution.

A Keithley 250 is utilised for routine wafer assessment, where large quantities of data can be stored and analyzed using the Keithley database analysis routines. For more detailed manipulation/analysis, data can be easily transferred to the VAX system where MEDL developed routines are available.

More rigorous and detailed testing can be achieved using a HP4145 parametric analyzer controlled by a HP310 computer. Connection via a 40-channel relay matrix to an auto-prober enables any specific parameter to be measured across the whole area of a wafer. Software has been developed for instrument control as well as for data manipulation and analysis to produce colour histogram/wafermap outputs. Data can be transferred from the HP computer to the VAX, using terminal emulator software, where analysis using existing statistical software programs can be performed.Radiation effects can be studied using another HP4145/matrix/computer configuration linked to an ARACOR x-radiation system.

The 10-keV x-rays are produced within a lead-lined cabinet, which also contains an auto-prober and dosimeter. Connecting wires are passed through a shielded orifice which enables devices to be biased or measured during irradiation. Software can be developed to repeat a cycle of test, bias, and irradiate for assessment of total dose effects, without the need to open the cabinet. Facilites are available to test devices either in package or wafer form. Dose rates are determined by a suitable choice of tube current and voltage, within the range 0.25 to 160 Krads ($Si0_2$)/min.

Measurements of capacitance parameters use a HP4192 impedance analyzer, which has a resolution down to 10fF and a frequency range of 5Hz to 13MHz. A built-in power supply enables a bias of up to +35V to be applied to the device under test. A conductance value can also be obtained within the range 1 nS to 10 S. It has a four-terminal configuration making precise measurements possible when using a correctly designed test-box. Wafer measurements utilize two coaxial probes situated on a manual prober within a screened light-proof cabinet, keeping strays and external EM interference to a minimum. This equipment can be controlled by a computer where specific software can easily be written to set up, trigger and return results from the instrument.

Test Capability

The test area consists of some five Fairchild digital testers with capabilities up to 40 MHz and 120 pins. Timing resolution of 156 ps and accuracies of sub-500 ps are achievable on the most advanced in this range. Analogue and mixed signal products are covered by DIAL 2 in-house testers. A Fairchild 5588 Memory Tester is used to test memory devices up to speeds of 25MHz.

This ATE is supported by a wide range of automatic probers and environmental handlers, coupled with temperature sources, enabling full military and space level testing to be carried out.Control of the calibration of equipment, test programs, test hardware, test methodology, pratices, and device flow is maintained by an extensive quality control sytem, ensuring compliance to the various commercial, military, and space quality screening levels. Procedures for handling static sensitive device within the area.

The computer-aided manufacturing (CAM) system, using PROMIS software, is installed in this area to control work progress, provide traceability and return results from analysis.

Burn-in / Life test

Extensive burn-in facilities offer screening at any temperature up to 150°C. Burn-in voltages can be provided up to +15 volts for particular devices. The ovens have continuous monitoring of both temperature and voltage to ensure complete reliability. Sequential switching of device supplies and controlled cooling is incorporated into the device flow wherever necessary. Both static and dynamic burn-in is carried out in this area to MIL-STD-883C, ESA 9000, BS9000, and commercial standards.

High volume standard products have dedicated burn-in modules, but reconfigurable modules are available for rapid response, covering a wide range of standard packages, DIP, PGA, LCC, Cerquads, etc.

Burn-in times may vary from 1 hour to 500 hours for production screening, 100 to 200 hours for QCI testing and 2000 to 6000 hours for specific qualification exercises. Specific areas are used for engineering investigations and specialized exercises demanding modified equipment/monitoring.

The SOS Product Range

A range of products and capabilities has been developed to ensure that all the major elements in a radiation hard system are available and fully supported. The product strategy is to continue to develop products to increase the performance of the following families and release them to the appropriate military and space quality levels.

Microprocessors

The key microprocessor product is the MAS281 MIL STD 1750A microprocessor. Based on the McDonnell-Douglas MDC281, the GPS version has been enhanced to make it the only viable radiation hard, space grade, 1750A microprocessor. It is supported by a range of standard peripheral devices to satisfy standard system functions.

A high performance (3 MIPs) 1750 microprocessor will be available from late 1990. Designated as the MA31750, it will meet the requirements for higher speed processing of both 1750A and 1750B instruction sets in space and military applications.

Memories

A range of static random access memories (RAM) has been developed specifically for radiation hard applications. As the products have evolved from 1K bits to 64K bits, process and design techniques have been refined resulting in progressively harder and faster components.

Read Only Memory (ROM) is offered as a capability with either base or metal programming. ROM is also used in standard products such (micro-code ROM) and databus (protocol look-up table).

Logic

Simple logic functions and octal transceivers, latches, buffers, decoders and multipliers have been included in the SOS product range to allow non-standard functions to be configured which do not justify a semicustom development. Innovative techniques allow new products to be rapidly introduced and a wide range of devices to be manufactured with minimal lead time and cost penalties.

Databus

The Microelectronics Division has been a leading supplier of MIL STD 1553 products for more than a decade. In 1982, the division demonstrated the first full protocol LSI chip set. A more powerful, radiation hard chip set has now been produced.

The MIL STD 1553B protocol was originally defined for military avionic systems but is now used in other military systems and is being designed into future space projects.

Semicustom

Gate arrays in 2.5µ CMOS SOS ranging in complexity from 700 to 4048 gates provide rapid access to the SOS technology for non standard functions. For more complex designs, an extensive standard cell library enables Marconi design engineers to quickly and consistently produce radiation hard circuits to meet customers' specific requirements. This capability has been expanded with the introduction of a 20,000 Sea of Gates in 1.5 micron SOS.

Analogue cells are now being added to the standard cell library in 3µ CMOS SOS. A standard cell library in 1.5µ CMOS SOS is in development.

Mixed Analogue and Digital

Standard products and standard cells have been produced for such functions as analogue to digital, and digital to analogue converters, comparators and operational amplifiers. These elements are now being developed in SOS for radiation hard space and defence applications.

Radiation Hardness Definitions

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An integrated circuit is said to be radiation hard if it can continue to function within its specifications after exposure to a stated amount of radiation. On Earth, the atmosphere shields systems at ground level from most gamma and x-rays, electrons and heavy ions which occur in space, can change the electrical properties of integrated circuits and adversely affect system performance. Defence applications are also demanding increasing tolerance to a variety of radiation effects. Although all semiconductors have some intrinsic resistance to radiation, CMOS SOS is the only technology which is tolerant to all radiation effects.

Accumulated Total Dose

The total dose hardness of an integrated circuit is a measure of its ability to withstand accumulated doses of high energy radiation in the form of gamma or x-rays. In the space environment, the ionising radiation that is absorbed by a device is accumulated over a long period of time; typically 100KRad (Si) over a 10 year operating life, but may be significantly higher depending on orbit.

Ionizing radiation produces its effect in the gate oxide of a silicon-on-sapphire transistor. The major effect is one of transistor threshold voltage shifts. No field oxide effects are observed, because of the lack of parasitic field transistors normally found on bulk CMOS devices.

Ionizing radiation causes electron-hole pair generation in the oxide. Reconstruction occurrs immediately, but under a positive bias electrons are swept to the gate electrode within pico seconds. The less mobile holes move towards and eventually are trapped in the silicon-dioxide interface region, causing a negative threshold voltage shift.

Total dose hardness up to the 1M Rad(Si) level is only achieved by a constrained design system and special attention to critical process steps especially gate oxide growth. Detailed analysis of radiation effects using the in-house gamma and x-ray facilities is also required.

Transient Dose

One well known problem with most MOS technologies is their vulnerability to high transient doses of ionising radiation. These disturbances have been shown to induce the phenomenon of latch up. Ordinary CMOS circuits have certain parasitic transistors associated with adjacent P and N channel devices. These parasitics are configured so as to approximate a silicon controlled rectifier (SCR). The photo-current induced in these parasitics by a large burst of ionising radiation can be sufficient to turn on the SCR, and thus initiate a large, self perpetuating current flow capable of causing great damage to the device. Once latched, a circuit can only be returned to correct operation (if not permanently damaged), by a power down/power up procedure.

It is physically impossible for a SOS device to suffer from latch up. In SOS, each transistor is made on an individual silicon island. These islands are isolated from each other by removing all epitaxial silicon from non-active areas, leaving only insulating sapphire substrate. This removes the possibility of any parasitic structures existing between transistors, and thus completely prevents latch up.

The other effect of transient radiation is to cause data corruption in stored cell elements. This corruption is caused by the inability of the power rail to hold up the voltage on a node sufficiently to maintain the data (power rail collapse). The voltage drop is as a result of the transient burst generating a photocurrent, the magnitude of which is proportional to total junction area. The CMOS SOS technology gains its high tolerance to transient radiation from the fact that the junction area is confined to only the thin epilaxial layer rather than the much larger junction and well depletion volumes which occur on conventional CMOS processes.

Evaluations have shown corruption levels of 1×10^{11} Rad(Si) Sec^{-1} and will survive without permanent degradiation levels of $>1 \times 10^{12}$ Rad(Si) Sec^{-1} on RAMS fabricated on the 1.5 micron SOS process.

Single Event Upset

SEU within a memory cell can be defined as the corruption of data cuased by the creation of a charge in a circuit by a heavy particle ion. There is no permanent or long term damage to the circuit, data becoming valid again after the next write operation.

As a charged particle passes through a semiconductor, it will lose energy by ionization. If a charged particle passes through a reverse-biased p-n junction, the electron-hole pairs generated in the device depletion region will be separated by the high electric field. The high carrier density created along the particle's track will distort the electric field of the junction depletion region. The field will be spread along the particle track and create a "field funnel". The charges in this funnel will be collected by drift and will add to the charge collected in the junction depletion region.

If sufficient charge is deposited on the parasitic gate and junction capacitance, a voltage transient will appear. The voltage transient created by an event on a node can then cause the logic state of the cell to be inverted. The charge required to invert the state of the memory cell is referred to as the critical charge.

Silicon on Sapphire technology offers significant advantages in this area. The physical structures of SOS transistors with their individual, totally isolated silicon islands, lead to much smaller 'junction depletion region' volumes than bulk CMOS technologies.

The charged particle state can also induce latch up in bulk CMOS circuits. For the reasons outlined in the previous section this is not possible on CMOS SOS.

Evolutions carried out on a Cyclotron by the European Space Agency have shown 3.4 E-9 E/bit day with a threshold LET of 31.4 for 3 micron SOS RAMS and 4.3 E^{-11} E/bit day with a threshold LET of 59.4 for 1.5 micron SOS RAMS.

Neutron Radiation

CMOS SOS is inherently hard to neutron radiation. The main effect of neutrons are to degrade the silicon lattice giving rise to recombination sites. This has the effect of reducing minority carriers lifetime which has a significant effect on bipolar technologies.

CMOS SOS in common with all MOS is a majority carrier technology and is therefore largely unaffected.

SOS Devices have been proven to with stand neutron radiation to greater than 10^{15} neutrons/cm^2 (the limit of the equipment used) without significant degradation of critical device parameters.

section 2

MICROPROCESSORS

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S10103ADS Issue 2.3 October 1990

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

Features

- **Radiation hard**
- **3 MIP DAIS throughput @ 22 MHz clock**
- **MIL-STD-1750 A or B operation**
- **Silicon-on-sapphire technology**
- **High performance architecture**
- **64kWord address space; expandable to 1 MWord (1750A) or 8 MWord (1750B) with optional MMU**
- **Single chip CPU**

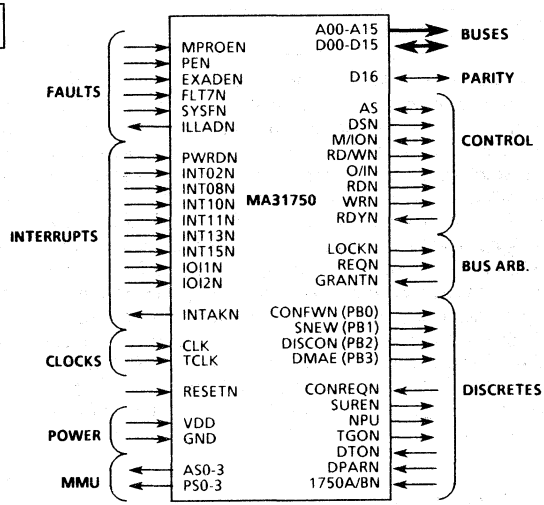


Figure 1: Pin definition; 1750A (1750B) mode

General Description

The Marconi MA31750 is a single-chip microprocessor that implements the full MIL-STD-1750A Instruction Set Architecture or option 2 of Draft MIL-STD-1750B. The processor executes all mandatory instructions and many optional features are also included. Interrupts, fault handling, memory expansion, Console, timers A and B, and their related optional instructions are also supported in full accordance with MIL-STD-1750.

The MA31750 offers a considerable performance increase over the existing MAS281. This is achieved by using a 32-bit internal bus structure with a 24 x 24 bit multiplier and 32-bit ALU. Other performance-enhancing features include a 32-bit shift network and a dedicated address calculation unit.

The MA31750 has on-chip parity generation and checking, to enhance system integrity.

A comprehensive built-in self-test has also been incorporated, allowing the processor functionality to be verified at any time.

Console communication is supported through a parallel interface using command/data registers in I/O space. A number of discrete output signals are produced to minimise external logic.

Three pins are provided to allow inclusion of the MA31750 into a multiprocessor or DMA system.

The processor can directly access 64kWords of memory in full accordance with MIL-STD-1750A. This increases to 1MWords when used with the optional MA31751 memory management unit (MMU) 1750B mode allows the system to be expanded to 8MWord with the MMU.

High Performance MIL-STD-1750 Microprocessor

(Advance data)

1 Architecture

The Marconi MA31750 Microprocessor is a high performance implementation of the MIL-STD-1750A (Notice 1) instruction set architecture. Figure 2 depicts the architectural details of the chip. Two key features of this architecture which contribute to the overall high performance of the MA31750, are a 32-bit shift network and a 24-bit parallel multiplier. These subsystems allow the MA31750 to perform multi-bit shifts, multiplications, divisions and normalisations in a fraction of the clock cycles required on machines not having such resources. This is especially true of floating-point operations, in which the MA31750 excels. Such operations constitute 16% of the Digital Avionics Instruction Set (DAIS) mix and a generally much higher percentage of many signal processing algorithms, therefore having a significant impact on system performance.

1.1 Operating modes

The MA31750 may be operated in one of two basic user selectable modes. 1750A mode follows the requirements of MIL-STD-1750A (Notice 1) and implements all of the mandatory features of this standard. In addition, many of the optional features such as interval timers A and B, a watchdog timer and parity checking are included. 1750B mode, when selected, allows the user access to a range of new instructions and features as described in the Draft MIL-STD-1750B, Option 2. These include a range of unsigned arithmetic operations and expanded addressing support instructions.

In accordance with MIL-STD-1750A, the MA31750 can access a 64K-word address space. With the addition of an external Marconi MA31751 chip configured as a Memory Management Unit (MMU), this address space may be expanded to 1MWord (1750A mode) or 8MWord (1750B mode). The MA31751 data sheet gives further information on the MMU/BPU chip. Note that although a partial implementation of MIL-STD-1750B with only 512 page registers is permitted, expanding the system to give the full compliment of page registers (8192) specified by 1750B would require several MMU chips.

For those applications not requiring adherence to the address space requirements of MIL-STD-1750 the MMU may optionally be configured with up to one megaword each of instruction and operand space (1750A) or 8MWord each (1750B).

The basic MMU function allows write or execute protection to be applied on 4kWord block boundaries. This may be further resolved to 1kWord blocks by the inclusion of a Block Protect Unit (BPU). The MA31751 can act as both an MMU and a BPU in 1750A mode, operating with the full compliment of 1MWord of memory. It will also support expansion to 8MWord in accordance with Draft MIL-STD-1750B.

In addition to implementing all of the required features of MIL-STD-1750A and the Draft standard MIL-STD-1750B, the MA31750 also incorporates a number of optional features. Interval timers A and B as well as a trigger-go counter are provided. Most specified XIO commands are decoded directly on the chip and an additional set of commands, associated with MMU and BPU operations, are decoded on chip. All commands not directly decoded by the processor are output for decoding by external logic in accordance with the XIO and VIO protocols of MIL-STD-1750A and B.

The MA31750 offers a number of extra lines to allow its use in a system utilising multiple processors. A bus request and grant system coupled with external arbitration logic allows common data and address buses to be used between devices. A lock request pin is also provided to allow the processor to maintain control of the buses when accessing areas of shared memory and executing read-modify-write instructions.

1.2 Internal Features

Key features include: (1) a three-bus (R, S, and Y) data path consisting of an arithmetic/logic unit (ALU), three-port register file, shift network, parallel multiplier and flags block; (2) instruction fetch registers C0,C1, IA, and IB; (3) operand transfer registers A, DI, and DO; (4) a state sequencer; and (5) microinstruction decode logic. A brief description of these features follows:

1.2.1 Arithmetic/Logic Unit (ALU)

A full function 32-bit ALU performs arithmetic and logic operations on one or two 32-bit operands in a single machine cycle. The ALU supports 8-bit (exponent), 16-bit (word), 24-bit (mantissa) and 32-bit (double) data in two's complement form. The ALU performs all necessary shifting and sign-extensions to allow results to be calculated and placed correctly.

1.2.2 Three Port Register File

A 28-word by 16-bit wide register file is used to store operands, addresses, base pointers, stack pointers, indexes, and temporary values. Registers R0 through R15 are general purpose and user accessible in accordance with MIL-STD-1750A; remaining registers are accessible by microcode and are not directly accessible to the user. Wrap-around concatenation of R0 through R15 allows 32- and 48-bit operands to be stored. Each register file port is 32-bits wide and the three-port architecture allows two operands to be read and a third operand to be written within one microcycle.

1.2.3 Parallel Multiplier/Accumulator

This multiplies a 24-bit multiplicand by a 24-bit multiplier in a single machine cycle. Only one iteration through the multiplier is required to complete a 16-bit by 16-bit multiply. During floating point multiply operations, the ALU generates the exponent whilst the mantissa product is being formed by the multiplier. This allows a floating point multiply operation to be accomplished in only one machine cycle.

1.2.4 Shift Network

This shifter is a 32-bit shift network, allowing multibit shifts to be accomplished in a single machine cycle. It is used by the microcode for all shift, rotate, and normalise operations.

1.2.5 Quotient Shift Network

A separate 32-bit shift register, which can be serial/parallel loaded and unloaded, is attached to the ALU. Its function is to supply quotient bits to the ALU during divide operations. The result of the divide is returned bit by bit to the Qshift block to be assembled.

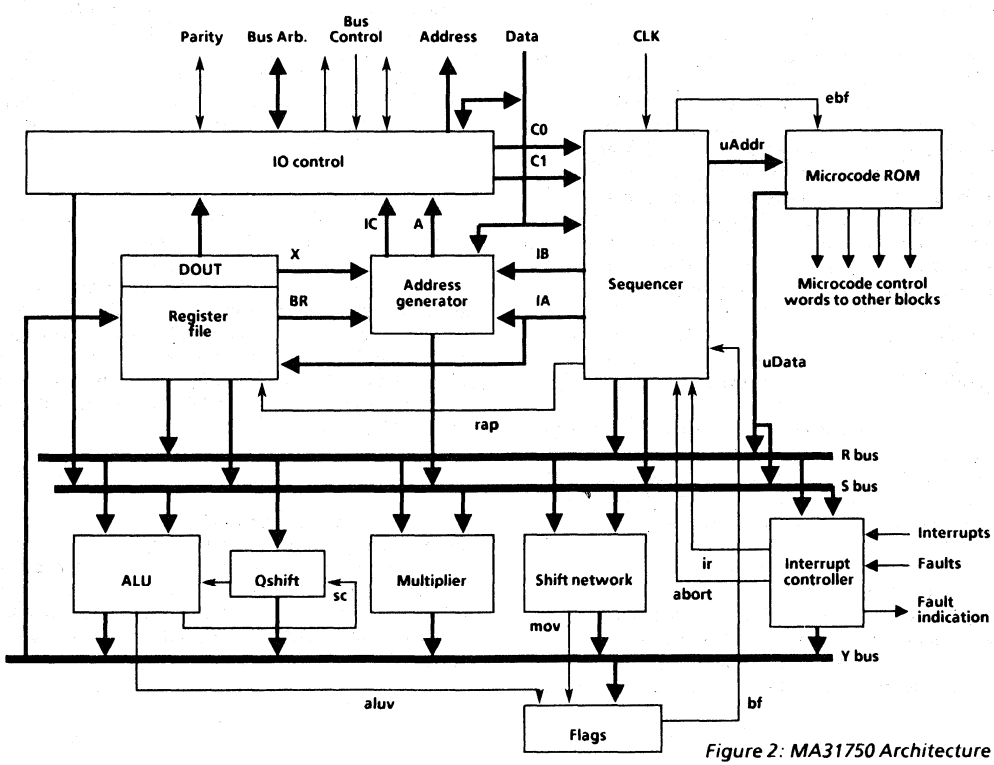


Figure 2: MA31750 Architecture

1.2.6 Flags Block
This block holds the condition status (CS) bits C, P, Z, and N (part of the system status word); the internal microcode flags (not user-accessable) and the flag decode logic. The flags are derived from the value on the Y-bus at the end of each cycle. The type of microcode operation being performed determines the position of the result on the bus.

1.2.7 Sequencer Block
A state machine, clocked by the system oscillator, generates processor timing and control signals. These signals constitute the lowest level of control available within the module, and provide the framework for basic operations such as selecting the next microinstruction to be executed or performing an operation within the ALU. Each complete pass through the state machine corresponds to one such operation and constitutes a machine cycle.

The microsequencer controls the execution of each MIL-STD-1750A or macro instruction by stepping through its corresponding microcode sequence. If the macroinstruction is a conditional, the CS bits of the status word will be interrogated to determine the necessary course of action. At the completion of each macroinstruction, the microsequencer checks to see if a Hold request or an interrupt is pending. If so, the microsequencer will branch to the appropriate microinstruction sequence. If not, the microsequencer begins sequencing the next macroinstruction.

Note that the microsequencer is under its own control. Each processor machine cycle corresponds to the execution of a single microinstruction.

All internal cycles and external cycles when running with no wait states are two system clocks (CLK) long. Any external cycle may be lengthened by adding an integral number of wait states which will extend the basic cycle by one clock period per wait state added.

1.2.8 Instruction Pipeline
There are four, 16-bit pipeline registers: IA and IB are in the sequencer block and hold the instruction currently executing (and its postword, if any); C0 and C1 are in the IO block and hold the next instruction (and postword).

During the execution of any MIL-STD-1750A or B instruction, instruction fetches are performed to replace the number of words in the current instruction.
In this way, at the end of the current instruction the pipeline already contains the next instruction. The sequencer decodes the next instruction before its execution, allowing the first microcode word in the instruction sequence to be made available right at the start of the instruction.

1.2.9 Microcode ROM Block
This is a 1.25k- (1280) word by 64-bits/word ROM which stores the microinstructions that implement the MIL-STD-1750A and B instruction sets. In addition to the microinstruction sequences corresponding to the MIL-STD-1750A/B instructions, the microcode ROM also stores sequences for performing initialisation, interrupt response, bus hold response, instruction prefetch and built-in-test (BIT). The address of the next microinstruction to be accessed is generated by the microsequencer. The accessed microinstruction is latched at the very start of each microcycle (machine cycle) and broadcasted to the rest of the processor.

1.2.10 IO Block
The IO block handles the sequencing of the bus control signals to effect a memory or IO transfer. It also manages the bus arbitration signals and the external ready interface. The Data In (DI), and Data Out (DO) registers serve to buffer transfers between the data path and the system address and data busses. These registers are used under microcode control and are not directly accessible by software. A description of the use of these registers during memory and I/O operations is provided in section 3.0.

1.2.11 Address Generator Block
The address generator block holds the two system address registers: IC - the instruction to be fetched next; A - the address of any operands associated with the current instruction. The block contains its own 16-bit ALU which allows address calculations such as (base + index) to be performed independently of the main ALU.

1.3 Interrupt Block

The interrupt block incorporates a pending interrupt register, a mask register, a priority encoder, a fault register, a status word, two interval timers (A and B), a trigger-go counter, XIO command decode logic, and microcode control logic. A brief description of these features follows.

1.3.1 Pending Interrupt Register (PI)

This 16-bit register is used to capture and hold interrupts until they can be processed by software, using a logic 1 to represent a pending interrupt. The PI supports three dedicated external, six user-definable external, and seven dedicated internal interrupts. Level-sensitive interrupts are captured at the beginning of each machine cycle, whilst edge sensitive interrupts are captured immediately.

1.3.2 Mask Register (MK)

This 16-bit register is used to store the interrupt mask. Interrupts are masked by ANDing each mask bit with its corresponding PI register bit. Interrupts which are masked will be captured in the PI register but will not be acted on until unmasked. Interrupt level 0 can not be masked. A logic 0 in a given bit position indicates that the corresponding bit in the PI register will be masked.

1.3.3 Priority Encoder

This encoder generates an interrupt request to the CU whenever one or more unmasked interrupts are pending and enabled in the PI and encodes the highest priority unmasked pending interrupt as a 4-bit vector. This vector is read during interrupt servicing in order to create the interrupt Linkage and Service pointers.

1.3.4 Fault Register

This 16-bit register is used to capture and hold both internal and user implemented external faults using positive logic, i.e., a logic "1" represents a fault. Bus cycle faults are captured at the end of each machine cycle whilst the two general purpose faults SYSFN and FLT7N are edge-triggered. Setting any one or more faults in FT will cause a level 1 (machine error) interrupt request. Once a fault is set in FT, it may only be cleared via an XIO command.

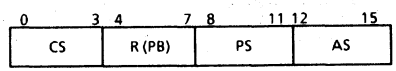
In 1750B mode, a fault mask register is provided to allow selective masking of fault conditions. Section 5 (Software Considerations) contains further information.

1.3.5 Timers A and B

These are two 16-bit software controllable timers. Timer A is clocked by the TCLK input while Timer B is clocked by the internally generated TCLK/10. Timers A and B will generate interrupt levels 7 and 9, respectively, when their maximum counts are reached. In 1750B mode, each timer has a reset register to give greater control over the count period. Section 5 (Software Considerations) contains further information.

1.3.6 Status Word

Figure 3 depicts the status register format. This 16-bit word is divided into four, 4-bit sections. Three of these sections [AS, PS and, (1750B mode) PB] are control bits for implementing expanded memory with an external MMU. The fourth section, CS, is held within the flags block. The AS field is used during expanded memory access to define the page register set to be used for instruction and operand memory references. The PS field is used during memory protect operations to define the access key used for memory accesses. The PS field is also used during execution of privileged instructions. PS must be zero for such operations to be legal. The PB field is used in conjunction with the AS field in 1750B mode to expand the number of page registers available. Note that attempting to set AS or PB to a non-zero value with no MMU, or setting PB to a non-zero value in 1750A mode is illegal. This will be aborted and a fault II will be generated (SW will remain unchanged).



Field	Bits	Description
CS		CONDITION STATUS:
	0	C- Carry from an addition or no borrow from a subtraction
	1	P- Result >0
	2	Z- Result = 0
	3	N- Result<0
R	4 - 7	RESERVED (= 0) in 1750A mode PAGE BANK SELECT in 1750B mode
PS	8 - 11	PROCESSOR STATE: (a)- Memory access key code (b)- Privileged instruction enable
AS	12 - 15	ADDRESS STATE: Page register sets for expanded memory addressing

Figure 3: Status Word Format

1.3.7 Trigger-Go Counter

This 16-bit counter is clocked by the TCLK input, is enabled during system initialisation, and may be preset under software control to give a wide range of timeout intervals.

The timer is stopped upon overflow or by presetting to zero. Overflow is signalled by a low level on the TGON discrete output, which remains low until the counter is reset by software. This counter is typically used as a system "watchdog" timer. Note that the action of the timer is independent of the main CPU and will continue to run (and produce TGON) even if CLK is disabled.

1.3.8 XIO Command Decode Logic

This logic decodes all internally supported XIO commands and generates the control signals necessary to carry out the commanded action. In addition, the validity of a command not implemented internally is verified. Figure 22c in Section 6 identifies the XIO commands which are internally supported by the MA31750.

2 Pin Descriptions

A description of each pin function follows. The function name is presented first, followed by its acronym and description. Function type is either input, output, high impedance (Hi-Z), or a combination thereof. Full timing characteristics of each of the functions are shown in section 7.

All signals - with the exception of power, ground and clock signals are TTL compatible, and are provided with Electrostatic Discharge (ESD) protection circuitry. Throughout this data sheet, active low signals are denoted either by placing a bar over the signal name, or by following the signal name with an "N" suffix, e.g., DSN. If a signal has a dual function, both function names will be used separated by a "/". The function name to the left of the "/" will be active high while the function to the right will be active low, again with an "N" suffix, e.g., RD/WN.

Pin Name	Pin N°	Function	Description
POWER			
VDD		Power supply	DC power supply input
GND		Ground	0V reference point.
CLOCK SIGNALS			
CLK		System clock	Input clock signal
TCLK		Timer clock	This clock input is used by the internal 16-bit timers A and B, and by the Trigger-Go counter. MIL-STD-1750 requires this signal to have a frequency of 100kHz.
SYSTEM BUSES			
A00-A15		System address bus	An active-high address bus which is tri-state during bus cycles not assigned to this CPU. A00 is the most significant bit.
D00-D16		System data bus	An active-high data bus which is tri-state during bus cycles not assigned to this CPU. D00 is the most significant bit, D16 is the parity check bit.
EXTERNAL REQUESTS			
RESETN		System reset	This active-low input should be asserted low to reset the processor. The low to high transition will start the initialisation sequence which will perform a Built-In-Test and will initialise the processor in accordance with MIL-STD-1750.

Figure 4. Pin Descriptions

Pin Name	Pin No	Function	Description
BUS CONTROL			
AS		Address strobe	This active-high bidirectional signal establishes the beginning and end of each bus cycle. The trailing edge (high-low transition) is used to sample bus cycle-related faults into the fault register. The leading edge guarantees that a valid address is on the address bus. The line is an input during cycles not assigned to this CPU.
DSN		Data strobe	This active-low signal indicates the presence of data on the system data bus. During a processor read cycle, DS goes low to indicate that the processor is no longer driving the bus. This signal is tristate in bus cycles not assigned to this CPU.
M/ION		Memory/IO select	This bidirectional signal indicates whether the current bus cycle is accessing memory (high) or IO (low) addressing space. This signal becomes valid shortly after the start of a machine cycle and remains valid throughout. The signal is an input during cycles not assigned to this CPU.
RD/WN		Read/write select	This signal indicates the direction of data transfer on the system data bus. Data is read in by the processor when high, and written out when low. This signal becomes valid shortly after the start of a machine cycle and remains valid throughout. RD/WN is tristate during cycles not assigned to this CPU.
O/IN		Operand/instruction select	This signal indicates whether the current bus cycle is accessing operand (high) or instruction (low) addressing space. This signal becomes valid shortly after the start of a machine cycle and remains valid throughout. O/IN is tristate during cycles not assigned to this CPU.
RDN		Read strobe	This active-low output is asserted low with DSN during read cycles. The rising edge of this signal indicates the time at which the processor reads the data bus. This signal is tristate in bus cycles not assigned to this CPU.
WRN		Write strobe	This active-low output signal is asserted low with DSN during write cycles. The rising edge should be sed by the system to latch data from the data bus. This signal is tristate in bus cycles not assigned to this CPU.
RDYN		Ready	This input signal allows the basic machine cycle of the processor to be extended to accomodate slower peripheral or memory devices. Ready may be pulled high to add an integral number of CLK cycles (wait states) to the machine cycle. The line must be pulled low to allow processing to proceed. RDYN has no effect on cycles dedicated to internal operations. [Note: If RDYN is held high during two consecutive TCLK high-to-low transitions (with DSN low), a bus timeout fault will occur and will be indicated in the appropriate bit in the fault register. The occurrence of this fault will cause the state sequencer to terminate the current machine cycle and begin a new machine cycle. Also, the presently executing macroinstruction will be aborted and execution will branch, unless masked, to the machine error interrupt (level 1) software routine. The DTON signal may be used to override this feature.]
BUS ARBITRATION			
LOCKN		Bus lock	This active-low output signal allows the system busses to be locked to one processor for successive cycles. The CPU will lock the bus during read-modify-write instructions such as DECM and TSB. During non-locked cycles, this signal remains high.
REQN		Bus request	This active-low output signal is driven low when the CPU requires the bus in the next cycle. An external arbiter should sample this signal at the third clock edge in a machine cycle. The signal becomes invalid when the CPU has started that cycle.
GRANTN		Bus grant	This active-low signal is produced by an external bus arbiter to indicate that the CPU currently has the highest priority bus request. If the bus is not locked, the CPU may begin a bus cycle commencing with the next CPU clock cycle. If the CPU is currently locking the bus then GRANTN is ignored.

Figure 4 (continued). Pin Descriptions

Pin Name	Pin No	Function	Description
INTERRUPTS			
PWRD		Power down interrupt	A low on this active low input will be captured in the PI register and sets pending interrupt 0. This is the highest priority interrupt and cannot be masked or disabled.
INT02N INT08N INT10N INT11N INT13N INT15N		User interrupt levels 2, 8, 10, 11, 13 and 15.	A low on any of these active low inputs will be captured in the PI register and will set pending interrupt levels 2, 8, 10, 11, 13, and 15, respectively. Level 2 is the highest priority user level while level 15 is the lowest priority. These interrupts are maskable and can be disabled. If edge sensitivity has been selected, interrupts will be captured on the falling edge of the interrupt input, otherwise the interrupt will be latched by the falling edge of AS. [NOTE: Interrupt levels 1, 3, 4, 5, 6, 7, and 9 are dedicated to internal machine interrupts] Unused inputs should be pulled up to VDD.
IOI1N IOI2N		I/O dedicated interrupts levels 1 and 2.	A low on either IOI1N or IOI2N will be captured in the PI register and will set pending interrupt levels 12 and 14, respectively. These inputs are level sensitive only and are captured by the falling edge of AS. Unused inputs should be pulled up to VDD.
INTAKN		Interrupt acknowledge	This active-low output indicates the start of an interrupt service When low, the processor outputs the linkage pointer (LP) address to the system The INTAKN signal may be used to remove level-sensitive interrupt inputs: the current interrupt priority can be ascertained by reading the address bus.
FAULTS			
MPROEN		Memory protect error	A low placed on this active-low input, sampled on falling AS, indicates that an access fault, execute protect or write protect fault has been detected. Bit 0 of the fault register is set if this signal is applied during a memory cycle; bit 1 is set if the line goes low during an IO cycle. Either condition sets pending interrupt level 1 and, in the case of a memory cycle error, aborts the current 1750 instruction. Although the MA31750 aborts the macroinstruction, system memory management, and/or block protect hardware is responsible for preventing the erroneous bus cycle from accessing memory. To effectively use this feature, MPROEN should be pulled low prior to the start of the next machine cycle. This can be accomplished by injecting wait states to hold off the new cycle until the system protection circuitry can decide whether or not to allow the transaction.
PEN		Parity error	A low on this active-low input, sampled on falling AS, informs the CPU that an external parity error has occurred. Bit 2(memory), 3(I/O) or 4(DMA) of the fault register is set, depending upon the type of transfer taking place. This asserts a level 1 pending interrupt,
EXADEN		External address error	A low on this active-low input, sampled on falling AS, informs the CPU that an external address error has occurred. Bit 8 of the fault register is set if this signal goes low during a memory cycle; bit 5 is set if the signal goes low during an IO cycle Either error condition asserts a level 1 pending interrupt and causes an abort of the current 1750 instruction.
FLT7N		General purpose fault input	A low at any time on this active-low input sets bit 7 of the fault register, causing a pending interupt level 1 This fault is user-definable
SYSFN		System fault input	A low at any time on this active-low input sets bits 13 and 15 of the fault register, causing a pending interupt level 1. This fault is user-definable.
ERROR INDICATION			
ILLADN		Illegal address	This active-low output drops low if the EXADEN input drops low or if the bus fault timeout circuitry causes an interface timeout.

Figure 4 (continued). Pin Descriptions

Pin Name	Pin Nº	Function	Description
MMU CONTROL			
AS0-AS3		Address state bus	This active-high bus indicates the current address state of the CPU. The value on this bus is copied from the status register within the CPU. These lines are tristate during bus cycles not assigned to this CPU.
PS0-PS3		Processor state bus	This active-high bus indicates the current process state of the CPU. The value on this bus is copied from the status register within the CPU. These lines are tristate during bus cycles not assigned to this CPU.
PB0-PB3		Page bank select bus	This active-high bus indicates the current CPU page bank when operating in 1750B, 8 MWord addressing mode. The value on this bus is copied from the status register within the CPU. These lines are tristate during bus cycles not assigned to this CPU. When operating in 1750A mode, these lines have the alternative functions CONFWN (PB0), SNEW (PB1), DISCON (PB2) and DMAE (PB3)
DISCRETES			
CONFWN		Configuration word read	This active-low output signal is driven low when the processor reads the external configuration register. The line may be used as an output enable for this register. The configuration register is read during initialization to determine the system configuration. (Note: In 1750B mode this pin is reassigned to PB0. To derive this signal in B mode, the user must decode the IO read from locaton 8410)
SNEW		Start new cycle	This active-high output will be asserted high during the first cycle of each new MIL-STD-1750 instruction sequence. This signal may be used for test purposes. (Note: In 1750B mode this output is reassigned to PB1)
DISCON		Discrete output select	This active-low output will be asserted low by the processor during an XIO DO command. It may be used as the enable signal for an external discrete output register. (Note: In 1750B mode this output is reassigned to PB2)
DMAE		DMA enable	This active-high output indicates that an external DMA device is enabled. It is disabled (low) following a reset and is toggled under program control using XIO commands DMAE and DMAD. (Note: In 1750B mode this output is reassigned to PB3)
CONREQN		Console request	This active-low input initiates and controls console operation following the end of a 1750 instruction. Commands and data are passed to the processor in this mode via three dedicated registers in IO space. Pending interrupts always take precedence over console operation.
SUREN		Start-up ROM enable	This active-low output indicates that start-up ROM is enabled. The signal is asserted low following initialisation or by XIO ESUR. The signal remains asserted until removed with XIO DSUR. When a start-up ROM is present on the system, this signal should be used to qualify its chip select or output enable such that the ROM may be accessed only when SUREN is low. [NOTE: Instruction pipelining must be considered in transitioning from Start-Up ROM to RAM. See Section 5 on Software Considerations]
NPU		Normal power-up	This output is driven high to indicate that the Built-In Test (BIT) sequence, performed on reset or power-up, has completed successfully. This output drops low when an external reset is applied. It may also be reset by software using the XIO RNS command.

Figure 4 (continued). Pin Descriptions

Pin Name	Pin N°	Function	Description
DISCRETES (Continued)			
TGON		Trigger-go output	This active-low output drops low whenever the trigger-go counter overflows (rolls over to 0000). It returns to the high state when the counter is reset by software (using XIO GO command).
DTON		Disable timeout	A low on this input will reset and disable the bus fault timeout circuitry.
DPARN		Disable parity	A low on this input will reset and disable the on-chip parity verification. Note that parity generation on write data is not disabled by this pin.
1750A/BN		1750A/1750B mode select	This input line allows the operating mode of the processor (1750A/1750B) to be selected. When high, the processor will be placed in 1750A mode. When low, the processor assumes 1750B mode. This line allows the new 1750B instructions to be trapped as illegal in 1750A mode, and switches the function of the dual-purpose control lines PB0-PB3.

Figure 4 (continued). Pin Descriptions

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

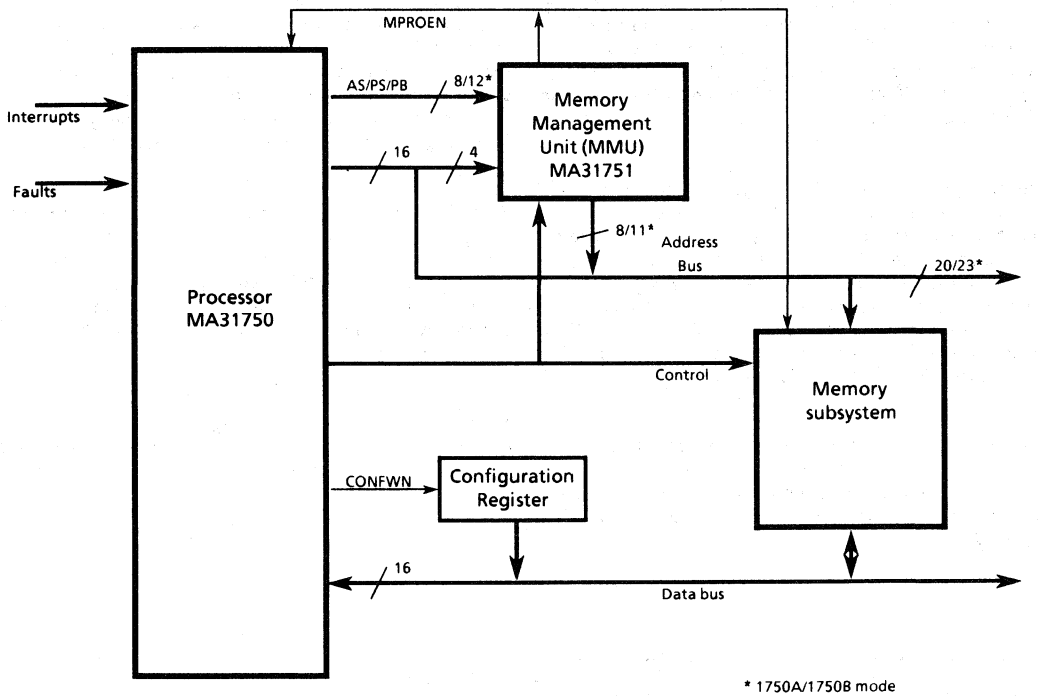


Figure 5: Typical MA31750/MA31751 System Interface

Configuration Register

The system configuration register allows the MA31750 to function with a variety of different system designs. Implemented features such as an BPU should be indicated as present by setting a bit in an externally-implemented, 16-bit latch in IO space defined by the table of XIO commands, figure 22c.

The configuration register is read by the processor during Initialisation. Alternatively, the register may be read from software by executing an XIO RCW command. The processor decodes this command internally and produces a discrete output signal CONFWN which may be used as the register Output Enable control. Alternatively the user may decode the IO command RCW to derive CONFWN (this must be done in 1750B mode since CONFWN is not available).

The bit position corresponding to each feature or optional device is shown in figure 6 below. Note that bits 8 through to 15 are unused by the processor. These may be used as discrete input lines by the user if required.

Although it is possible to change the system configuration in operation, this is not recommended. For example, if the interrupt level/edge trigger select bit (bit 4) is changed during normal operation of the device, one or more spurious interrupts may occur. It is strongly recommended that the user reset the processor following a change in the system configuration.

When in 1750B mode, the processor needs to know how many Page Banks are implemented in the external system so that Status Word changes can be protected properly. MIL-STD-1750B allows the options 0,1,2,4,8 or 16. The actual selection should be coded into the three configuration register bits MMU0, MMU1 and MMU2 as shown in figure 7 below.

Note that in 1750A mode, setting any of the MMU select bits indicates the presence of an MMU, the actual code is unimportant in this mode.

Bit No.	Function
0	MMU select 0
1	1 = BPU in system
2	1 = Console operation
3	MMU select 1
4	Interrupts (1 = Level, 0 = edge)
5	MMU select 2
6	Parity, 1 = odd, 0 = even
7	BIT on power-up, 1 = yes, 0 = no
8-15	Not used (may be used as discrete inputs)

Figure 6: Configuration Register Bit Assignment

Selected bit			Function
MMU2	MMU1	MMU0	
0	0	0	No MMU in system
0	0	1	1 Page Bank (PB0)
0	1	0	2 Page Banks (PB0-1)
0	1	1	4 Page Banks (PB0-3)
1	0	0	8 Page Banks (PB0-7)
1	0	1	16 Page Banks (PB0-15)
1	1	X	16 Page Banks (PB0-15)

Figure 7: MMU Select Bit Assignments

3 Operating Modes

MA31750 operating modes include: (1) initialisation, (2) instruction execution, (3) interrupt servicing, (4) fault servicing, (5) Console support and (6) timer operations.

3.1 Initialisation

The module executes a microcoded initialisation routine in response to a hardware reset. This routine clears module registers, disables and masks interrupts, reads the configuration register, resets the output discrete register (if implemented), initialises the MMU and BPU (if implemented), performs Built-In-Test (BIT), raises the Start-Up ROM enable discrete, clears and starts timers A and B, resets the trigger-go counter, and loads the instruction pipeline. Figure 8 summarises the resulting initialisation state.

BIT consists of ten subroutines, as outlined in figure 9, and begins by pulling NPU low. This is the first time after reset that NPU is guaranteed low. If all ten subroutines execute successfully, NPU is raised high. If any part of BIT fails, a corresponding bit identifying the failed subroutine is set in General Register R0, Fault Bit 13 is set in the Fault register (FT) and NPU is left in the low state. Figure 9 defines the coding of BIT results in R0. In the event of such a failure, the resulting module reset state will be dependent on where in BIT the error occurred and may not be the same as that shown in figure 8. A BIT failure indication in FT will set the level 1 interrupt request bit of the Pending Interrupt (PI) register. Since initialisation disables and masks interrupts, this interrupt request will not be asserted. Any external interrupts or faults occuring during BIT will be ignored and cleared before program execution begins.

The last action performed by the initialisation routine is to load the instruction pipeline. Instruction fetches start at memory location zero with AS = 0, PS = 0 and PB = 0 and will be from the Start-Up ROM if implemented. Whether BIT passes or not, the processor will begin instruction execution at this point. The system start-up code may include a routine to enable and unmask interrupts in order to detect and respond to a BIT failure if required.

MA31750	
Instruction Counter	Zero
Status Word	Zero
Fault Register	Zero
Fault Mask Register (1750B)	All ones
Pending Interrupt Register	Zero
Interrupt Mask Register	Zero
General Registers	Indeterminate
Interrupts	Disabled
Timers A and B	Zeroed and started
Timer Reset Registers (1750B)	Zero
Start Up ROM	Enabled
DMA Enable	Disabled
Triger Go Counter and TGON line	Reset and started
MMU	
Page Registers	Bank 0, Group 0, PS = 0
Page Register AL/W/E Fields	Zero
Page Register PPA Field	Logical to physical
BPU	
Memory Protect RAM	Disabled, zero
Global Memory Protect	Enabled

Figure 8: Initialisation State

3.2 Instruction Execution

Once initialisation has been completed, the module will begin instruction execution. Instruction execution is characterised by a variety of operations, each one or more machine cycles in duration. Depending on the instruction being executed at the time, these operations include: (1) internal CPU cycles, (2) instruction fetches, (3) operand transfers, and (4) input/output transfers. Instruction execution may be interrupted at the end of any individual machine cycle by an interrupt or console request.

3.2.1 Internal CPU Cycles

Internal CPU cycles are used to perform all CPU data manipulation operations. Internal CPU cycles are two clock periods in duration and are characterised by AS low, DSN high and M/ION high. Tables 22a and 22b in Section 6 provide machine cycle counts associated with each MIL-STD-1750A instruction.

3.2.2 Instruction Fetches

Instruction Fetches are used to keep the instruction pipeline full. This ensures that the next instruction is always ready for execution when the preceding instruction is completed. During jump and branch instruction execution the pipeline is flushed and refilled with two consecutive instruction fetches starting at the new instruction location. The pipeline is also refilled as part of interrupt request processing.

Instruction fetches are characterised by OP/IN low but are otherwise identical to an operand read transfer. For a detailed explanation of the function of various bus control signals during instruction fetches, refer to the discussion of operand transfers below. Section 6.5 provides timing characteristics for instruction fetches. Machine cycles associated with instruction fetches are a minimum of two oscillator periods in duration. The RDYN signal may be used to insert wait states to accommodate slow memory. Machine cycle counts included in figure 22a of Section 6.5 include instruction fetches.

Instruction fetches use instruction pipeline registers IA, IB, C0, C1, the instruction counter (IC) and the data input register (DI). Action is as follows. The contents of IC are placed on the A bus. The returned value, which will be an instruction, is stored in the IB or C0 register depending upon whether the current instruction is one or two words long. If the current instruction is two words long, the value in IC is incremented (via its dedicated counter) and the next fetch is performed. This second returned value, which may be either an instruction or an immediate operand, is stored in either C0 or C1 (again dependent upon the length of the current instruction).

At the end of the currently executing macroinstruction, the complete pipeline is advanced by either one or two places, thus bringing the new prefetched macroinstruction into IA and its associated post-word (if any) into IB. Since the opcode section of the new instruction (most significant 8 bits) has been prefetched the decoding of the instruction may be performed during the last cycle of the preceeding instruction, allowing the microcoded control information relevant to the new instruction to be made available right from the start of that instruction.

3.2.3 Operand Transfers

Operand transfers are used to obtain (read in) operands to be used by an instruction and to save (write out) any results of an instruction's execution. Section 7 provides timing characteristics for operand transfers. Machine cycles associated with operand transfers are a minimum of two oscillator periods in duration. The RDYN signal may be used to insert wait states to accommodate slow memory. Machine cycle counts in figure 22a of Section 6.5 include operand transfers.

Operand transfers use the address register (A), the data input register (DI), and data output register (DO). Before the operand transfer begins, the processor calculates the effective operand address in the address generator and stores this value in A. For write transfers, the processor loads the operand into the DO register.

All operand transfers between the CPU and memory are referenced to the AS and DSN bus control signals and are characterised by O/IN high and by M/ION high. The transfer begins by placing the contents of A (the address register) onto the A bus immediately following the start of the machine cycle. The AS strobe then goes high to indicate the presence of a valid address and remains high until the end of the cycle.

The RD/WN signal indicates the direction of the transfer. If the operation is a write, the operand in DO is placed onto the data bus, indicated by WRN low. DSN should be used to enable any data buffers present in the system. Data is guaranteed valid at the low-to-high transition of WRN. The memory system must pull RDYN low to conclude the transfer.

During operand read transfers, the data bus drivers are placed in a high impedance state before DSN is asserted low to give the memory system access to the bus. This transition can be used by the memory system to generate an output enable. The memory system must pull RDYN low to conclude the transfer. Data will be read into the DI register on the RDN rising edge.

3.2.4 Input/Output Transfers

Input/Output transfers utilize the MIL-STD-1750 XIO and VIO protocols and are characterized by M/ION low and O/IN high. RD/WN defines the direction of the transfer. AS, DSN and WRN cycle as with operand transfer operations. IO transfers may be divided into three groups; those commands which are implemented internally by the CPU; those commands which are implemented by external system hardware; and those commands defined as illegal by MIL-STD-1750A and B.

During the execution of an XIO command the processor will perform a test to determine the instruction group as defined above. If the instruction is implemented internally (e.g. Read Timer A) then the XIO data will be directed to or read from an internal register. If the instruction is implemented externally then data will be written to or read from the external system via the system data bus. In both of these cases the command appears on the system address bus but in the case of an internal transfer the data will be ignored (read) or invalid (write).

BIT	Test Coverage	Cycles
7	Temporary Registers (T0 - T11)	47
7	General Registers (R0 - R15)	79
8	Flags Block	18
9	Sequencer Operation and ROM checksum	5129
10	Divide routine Quotient Shift Network	12
11	Multiplier and ALU	13
12	Barrel shift Network	13
13	Interrupts and fault handling and detection	17
14	Address generator block	13
15	Instruction pipeline	15

Note: BIT pass is indicated by all zeros in FT bits 13, 14, and 15

Figure 9. Built-in Test Coverage and Timing

If a command is implemented internally, no RDYN pulse will be required to complete the cycle. A complete list of commands implemented internally by the MA31750 appears in figure 22c.

If an instruction is determined as illegal, or an EXADEN occurs during the execution of an optional external command then the instruction will be treated as a NOP but will set the appropriate bit in the system fault register (as defined in MIL-STD-1750A and B).

XIO is a priviledged instruction and, as such, may only be executed when the Status Word, PS field equals zero. Any attempt to violate this condition will be trapped by the command microsequence.

3.3 Interrupt Servicing

Nine user interrupt request inputs are provided for programmed response to asynchronous system events. A low on any of these inputs will be detected at the falling edge of AS and latched into the Pending Interrupt (PI) register on the following sync falling edge (where sync is an internal clock running at half the frequency of CLK. Stalling the CPU stops sync.) This sequence occurs whether interrupts are enabled or disabled or whether the specific interrupt is masked or unmasked.

All of the user interrupts INT02N-INT15N may be programmed to be either level or edge sensitive by setting or clearing the appropriate bit in the system configuration register (if implemented). If edge sensitivity is selected then an interrupt request input must transition to the high state before a subsequent request on that input will be detected. If level sensitivity is selected then holding an interrupt input low will cause a new interrupt to be latched following each service. Note that interrupts IOI1 and IOI2 are level sensitive only.

In order that the system may recognise when a service has been started, an interrupt acknowledge pin has been provided. At an early stage in the service of an interrupt, the processor will execute XIO command RLP and place a 4-bit code onto the data bus to indicate the service priority level. At the same time this command will be decoded internally to cause the INTAKN line to be asserted low. This signal may be used to release the latched interrupt line.

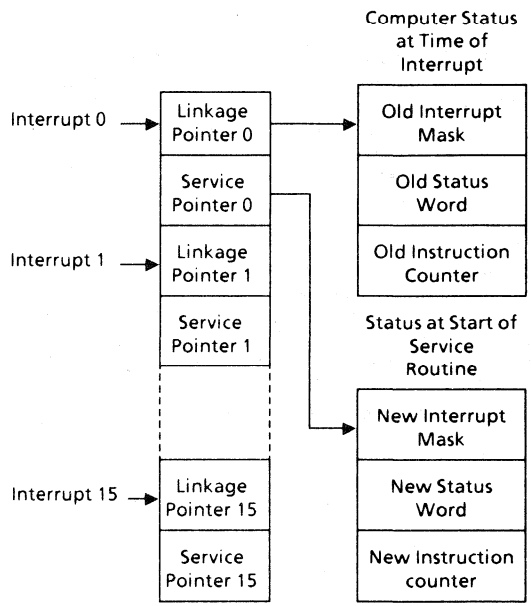


Figure 10. Interrupt Vectoring

When an interrupt request is latched into PI, it is ANDed with its corresponding mask bit in the mask register (MK). Interrupt level 0 is not maskable. Any unmasked pending interrupts are output to the priority encoder where the highest priority is encoded as a 4-bit vector. If interrupts are enabled, and an unmasked interrupt is pending, the priority encoder will assert an interrupt request to the sequencer.

Upon completing execution of a given MIL-STD-1750A or B instruction, the sequencer checks the state of the priority encoder's interrupt request. If an interrupt request is asserted, the sequencer branches to the microcode interrupt service routine. This routine performs a read of the priority encoder's 4-bit pending interrupt vector and then uses this value to calculate the appropriate interrupt linkage and service pointers. The pointers serve as addresses to data structures used in servicing interrupts. Figure 10 depicts this relationship. Figure 11 defines the pointer values.

Using the linkage and service pointers, the microcode interrupt service routine performs the following: (1) the current contents of the status word, mask register, and instruction counter are saved; (2) a write status word (WSW) I/O command is executed with an all zero data word; (3) the new mask is loaded into MK and interrupts are disabled; (4) the new status word is read and checked for a valid Address State (AS) field - If the address state is non-zero and an MMU is not present, the AS is set to zero and fault 11 (address state error) is set in the fault register FT; (5) a write status word command using the new status word is performed; and (6) the new IC value is loaded into IC, the instruction pipeline is flushed and refilled starting at the new address, and instruction execution begins.

[NOTE: The steps listed above represent a summary of actions performed during interrupt servicing and do not necessarily reflect the actual order in which these events take place.]

If an interrupt is latched during the interrupt service routine, it will not be processed until interrupts are re-enabled. If an AS fault occurs during the service routine, interrupt level 1 will be set. This interrupt will be serviced when interrupts are re-enabled unless it is masked by the new value in MK.

3.4 Fault Servicing

Five user fault inputs are provided. A low on any of the three bus-cycle-related fault inputs EXADE, MPROEN or

	Interrupt	LP Address	SP Address
PWRD	0	20	21
ME	1	22	23
INT02	2	24	25
Fl.P o/f	3	26	27
Fx.P o/f	4	28	29
BEX	5	2A	2B
Fl.P u/f	6	2C	2D
Timer A	7	2E	2F
INT08	8	30	31
Timer B	9	32	33
INT10	10	34	35
INT11	11	36	37
IOI1	12	38	39
INT13	13	3A	3B
IO12	14	3C	3D
INT15	15	3E	3F

Figure 11. Interrupt Pointer Definitions

MPE will be latched into the Fault Register (FT) on the next falling edge of AS. A low on either of the two general-purpose fault inputs FLT7N or SYSFN will set the appropriate fault bit immediately.

No falling edge detectors are provided to prevent repeat latching of faults held low beyond the first falling edge of AS. However, all FT bits are ORed together and input to the PI bit 1 through an edge detector to prevent the fault register from causing multiple level 1 interrupts.

The sequence of events following a fault capture depends on the type of fault as follows:

3.4.1 MPROEN, EXADEN, PEN and Bus Fault Time-Out

The capture of one or more of these faults sets pending interrupt level 1 (machine error) of the Pending Interrupt (PI) register on the falling edge of AS. Furthermore, the instruction currently executing is aborted at the AS high-to-low transition following the AS high-to-low transition that latched the fault. The IC value saved in the interrupt linkage table for the level 1 interrupt always points to the instruction which was in instruction pipeline register IA at the time of the abort. Anti-repeat logic between the FT and PI prevents latching more than a single interrupt into the PI before the user interrupt service routine has cleared the FT.

The microcoded interrupt service routine reads the interrupt priority vector from the Interrupt Unit and clears the serviced interrupt from the PI. However, the FT maintains the interrupting bit(s). Therefore, a level 1 interrupt would be latched again if there was no anti-repeat logic to prevent a never-ending loop of interrupts.

3.4.2 FLT7N and SYSFN

The capture of one or bothof these faults immediately sets pending interrupt level 1 (machine error) of the Pending Interrupt (PI) register. Anti-repeat logic between the FT and PI prevents latching more than a single interrupt into the PI before the user interrupt service routine has cleared the FT.

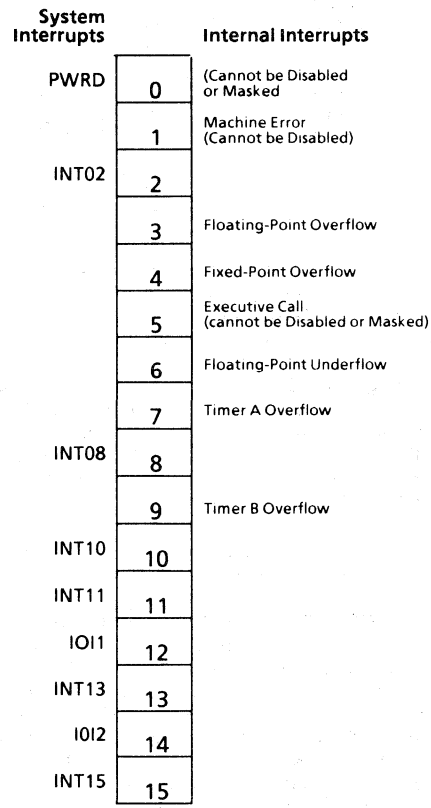


Figure 12. Pending Interrupt Register Bit Assignments

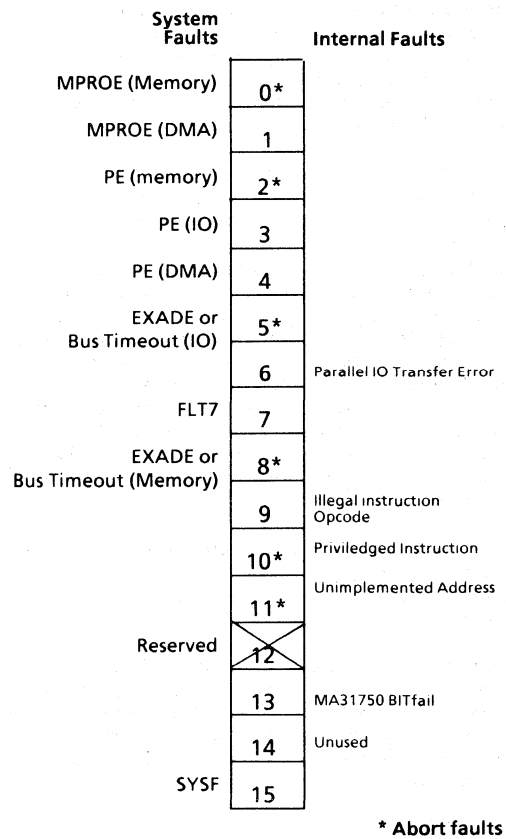


Figure 13. Fault Register Bit Assignments

Faults 0, 2, 5, 8, 10 and 11 cause the current instruction to be aborted. Although the current instruction will complete, any attempted writes to either the internal register file or to the sytem will be inhibited. The RDYN line will be ignored during these inhibited cycles.

During the machine cycles between fault capture and the beginning of the microcode interrupt handling routine, AS, DSN, RDN and WRN are forced to their inactive states. In the case of MPROEN, which may reflect an attempted write violation, it is required that system hardware provide the additional protection necessary to inhibit any memory write strobe.

Interrupts are serviced at the end of the currently executing instruction if not masked and if interrupts are enabled. System software servicing level 1 interrupts must clear the FT via the XIO RCFR command at some point in the routine to allow subsequent faults to latch a level 1 interrupt request. A non-destructive read of the FT is provided by the command XIO RFR, but this command should be used carefully.

3.4.3 Parity Generation and Checking

The MA31750 features on-chip parity generation and checking on all data bus transfers. Data generated by the processor has a parity bit attatched to it to allow external logic to verify write transfers. On read transfers, the processor will check the incoming parity (if enabled) and will generate the appropriate parity error fault if detected. Parity checking may be disabled when operating with devices which do not support parity generation by asserting the DPARN (Disable Parity) input low. The checking polarity (odd or even) is selectable with Configuration register bit 6.

3.5 Console Operations

The MA31750 will interface directly to an external console, allowing the operator to examine and change the contents of internal registers, memory and IO devices. All console transactions are conducted through one of three addresses in IO space:

Address	Function
8402_{16}	Console command input
$C000_{16}$	Data input
4000_{16}	Data output

Console mode may be entered in one of two ways:

1. By driving the CONREQN input low. This causes the processor to perform an IO read of the Console command (8402_{16}) following the completion of the current 1750 instruction and no pending interrupt. Valid console commands are shown in figure 15.

2. By executing the breakpoint (BPT) instruction. When the CPU encounters a BPT the internal copy of the system configuration register is read. If a console device is indicated then the MA31750 enters console mode and reads the command previously placed in 8402_{16}. If no console is present, BPT is treated as a NOP.

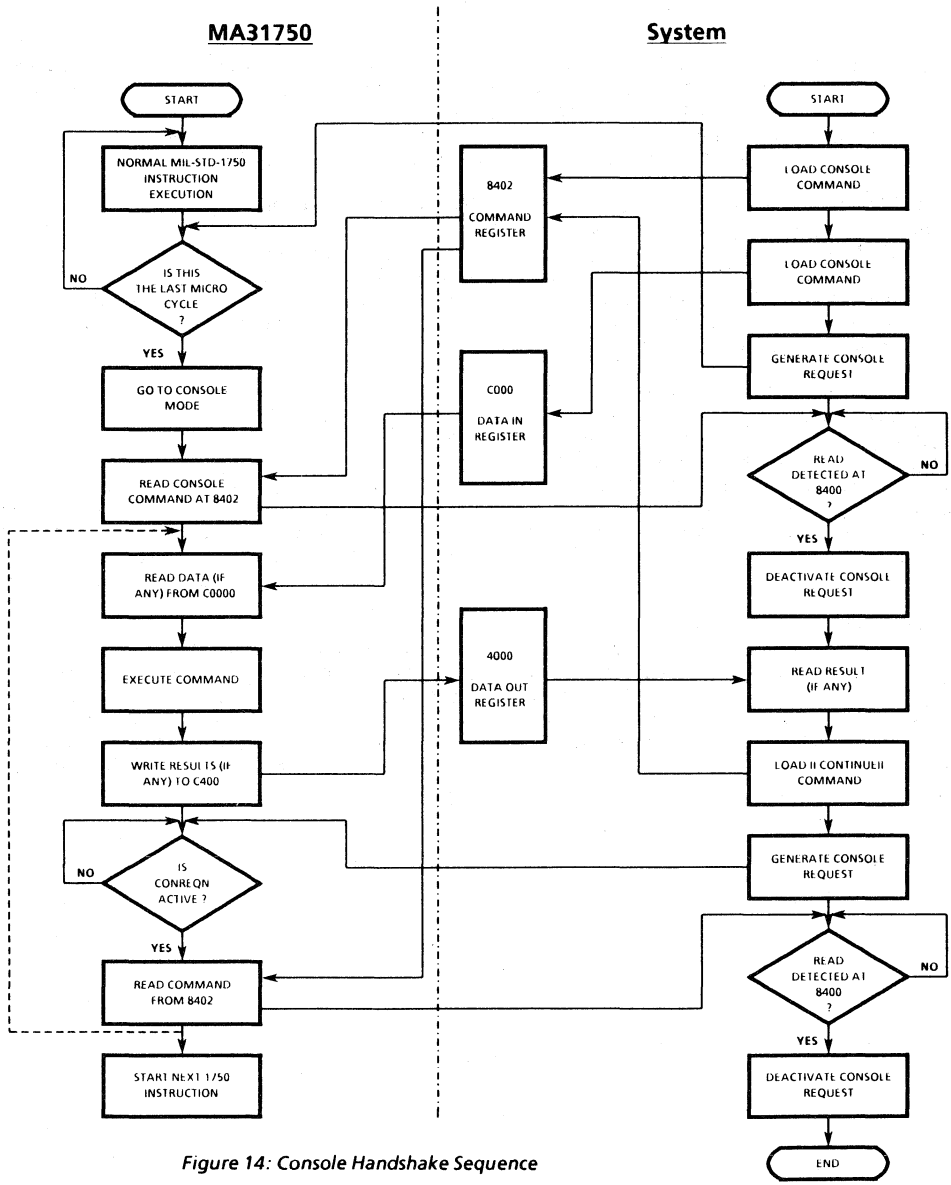
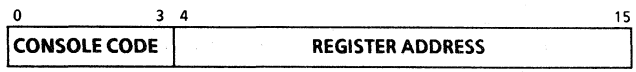


Figure 14: Console Handshake Sequence



CODE	FUNCTION
1	READ REGISTER
2	WRITE REGISTER
3	READ & CLEAR FAULT REGISTER
4	WRITE STATUS WORD
5	READ MEMORY
6	WRITE MEMORY
7	READ NEXT MEMORY
8	WRITE NEXT MEMORY
9	XIO
A	NEXT XIO
0	CONTINUE
B	DISABLE

REGISTER(S)	DESCRIPTION OF REGISTER(S)	HEX.
RN = R0-R15	GENERAL PURPOSE REGISTERS R0 TO R15	000-00F
TN = T0-T11	MICROCODE REGISTERS T0-T11	010-01B
A	OPERAND ADDRESS REGISTER	01C
IC	INSTRUCTION COUNTER	01D

Figure 15: Console Command and Register Definitions

3.5.1 Using BPT

Console mode may be entered by executing a BPT instruction with Console present indicated in the Configuration Word. On encountering a BPT instruction, the processor reads the Configuration Word to check for the presence of a Console. If a Console is indicated, the microsequencer branches to the microcode BPT Console service routine. This routine decrements IC once and enters the Console state.

To release the MA31750 from a BPT initiated Console state, the CONREQN input must be pulsed low following a continue command in accordance with the timing diagrams in Section 7. When CONREQN returns high, the Hold state will be released on the following AS high-to-low transition. Instruction execution resumes with the first instruction loaded into the pipeline.

3.5.2 Single-Stepping

Software can be single-stepped through the proper use of the CONREQN input and the BPT instruction. Use the BPT instruction to mark the beginning of the section of code which will be stepped through. Pulse CONREQN low to release the BPT initiated Hold state and then pull CONREQN low again during the two subsequent machine cycles that refill the instruction pipeline. When the first instruction following Hold release completes execution, the module will once again enter the Hold state. Again pulling CONREQN low will cause the next instruction to execute. This process may be repeated as long as required. Raising CONREQN high will resume normal operation.

3.6 Timer Operations

The MA31750 implements interval timers A and B, a trigger-go counter, and a bus fault timer. A discussion of each follows:

3.6.1 Timers A and B

Timer A is clocked by the TCLK input; timer B is clocked by an internally generated TCLK/10. The divider circuitry is reset when Timer B is reset to give deterministic processor operation. MIL-STD-1750A requires TCLK to be a 100-kHz pulse train. If allowed to overflow, timers A and B will set level 7 and level 9 interrupt requests, respectively. Timing characteristics of each timer are defined in Section 7. Each timer can be read, loaded, started and stopped by using XIO commands as identified in figure 15 of Section 3.5.

Each timer has associated with it a reset register from which the timer is automatically loaded following a software reset or overflow. These registers are initially loaded with zero but may be reloaded from software to provide greater control over the count period.

The MA31750 timers A and B will be disabled upon execution of a BPT software instruction when a Console is connected, as required by MIL-STD-1750A (Notice 1).

3.6.2 Trigger-Go Counter

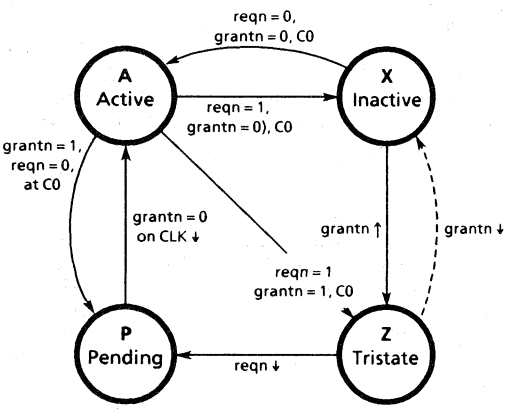
The trigger-go counter is also clocked by the TCLK input. In order that the count period may be controlled, a reset register is provided. On reset, this register is loaded with the maximum count of $FFFF_{16}$ but can be reloaded under software control to take any value between 0 and $FFFF_{16}$ (a value of zero disables the timer and TGON). This allows the timeout period to be varied between 20us and 0.65s.

The counter is decremented on each machine cycle. Whenever the trigger-go counter overflows, TGON drops low and remains low until the counter is reloaded from the reset register via the GO internal XIO command. Timing characteristics for trigger-go counter operation are defined in Section 7.

3.6.3 Bus Fault Timer

All bus operations are monitored to ensure timely completion. A hardware timeout circuit is enabled at the start of each memory and I/O transfer (DSN high-to-low transition) and is reset upon receipt of the external ready (RDYN) signal. If this circuit fails to reset within a minimum of one TCLK period or a maximum of two TCLK periods, either bit 8 (if the transaction is with memory) or bit 5 (if the transaction is with I/O) of the Fault Register (FT) is set. This sets pending interrupt level 1 and causes the current bus cycle to be terminated by forcing DSN high. The MIL-STD-1750A instruction is aborted, and control passes to the level 1 interrupt service routine (if the level 1 interrupt is unmasked). The timeout mechanism is disabled and reset if DTON is asserted low.

Multiprocessor Support



C0 - Falling clock at end of cycle.

Figure 16: Processor Bus Arbitration State Diagram

4.1 Bus Arbitration

Once initialisation has been completed, the processor will begin instruction execution by executing a sequence of microinstructions each one machine cycle (two system clock periods) long. Each machine cycle may perform either an internal or an external operation; if the operation is purely internal then the system buses will not be in use and may be reassigned to another processor.

The MA31750 uses three signals to control the ownership of the system buses. The REQN (Bus Request) line drops low towards the end of a machine cycle to indicate that the CPU can make use of the busses on the next cycle. The GRANTN (Bus Grant) pin should be asserted by an external arbiter to signal to the processor that the buses are clear and available for use. This signal is polled by the CPU on each falling clock edge after REQN is asserted low; the CPU will wait in this pending (P) state until granted. When grant is recognised, the CPU begins to drive the system buses. REQN, however, is not asserted high until after AS rises, to prevent the bus being reassigned very early in the new cycle.

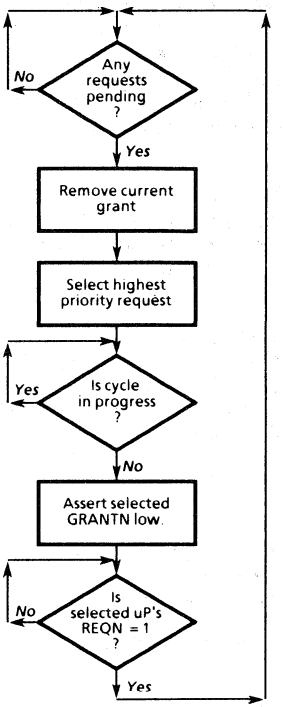


Figure 17: Possible Bus Arbitration Scheme

If the arbiter receives no further requests then GRANTN should be maintained low to prevent any delay from being introduced at the boundary between two consecutive transfers. The processor in this case will remain either in state A (during bus transfers) or state X (during internal cycles).

A third signal, LOCKN, signals that the CPU wishes to hold on to the bus prevent access by other processors during read-modify-write instructions. If a higher priority request is received, the arbiter must wait until the bus is inactive and unlocked before granting control to another processor. This is indicated by AS low and LOCKN high.

5 Software Considerations

5.1 Operating Modes

The MA31750 is capable of being operated in one of two basic modes, as previously mentioned. These are described in detail below:

5.1.1 1750A Mode

1750A mode is a full implementation of MIL-STD-1750A (Notice 1) and includes some of the optional features mentioned in this standard.

5.1.2 1750B Mode

1750B mode is an implementation of the proposed MIL-STD-1750B, Option 2, Draft of 17-July-1988. This mode extends the basic 1750A mode operation by allowing access to the larger address space and 'long' address-mode instructions of the 'B' standard. These instructions include the long load and store instructions and unsigned integer arithmetic. Note that the transcendental functions SIN, COS, LN etc. (Option 3 of MIL-STD-1750B) are not supported. Features new to MIL-STD-1750B which are in violation of MIL-STD-1750A are only enabled in 1750B mode. These include the new instructions, timer A and B reset registers, a Fault Mask register and the Page Bank select feature of the MMU.

There is a difference in the way in which 1750A and 1750B detect the overflow condition which may occur during floating point and extended floating point multiply and divide operations. In 1750A an overflow occurs if the sum (multiply) or difference (divide) of the exponents exceeds $7F_{16}$ or 80_{16} before the instruction is started. In 1750B the overflow is detected at the last point in the operation, i.e. after any normalization has taken place. The MA31750 takes the operating mode A or B into account when calculating the overflow in these cases, in order to comply with both specifications.

5.2 Using Start-Up ROM

The transition between code execution from Start-up ROM and system RAM must be made with care. If a system overlays RAM with the Start-Up ROM and the transition is made by simply executing XIO DSUR from the ROM, then the instruction pipeline will contain the value stored in the ROM location immediately following the XIO DSUR command. This value will be treated as an instruction and the module will attempt to execute it. In such cases, it is recommended that DSUR be followed by an unconditional branch instruction with offset, i.e., the BR instruction. An alternative approach is simply to jump to a portion of RAM not overlaid by the Start-Up ROM and execute DSUR from RAM.

5.3 Using Software Timers A and B

The MA31750 implements the two software timers A and B as defined int the MIL-STD 1750A specification. These are general purpose timers which are clocked at 100kHz and 10kHz respectively, giving clock 'tick' intervals of 10us and 100us respectively. They may be started using the XIO TAS and XIO TBS instructions, and stopped using XIO TAH and XIO TBH. If a timer is allowed to overflow ($FFFF_{16}$ - 0000_{16}) it will generate pending interrupt levels 7 (A) or 9 (B).

In 1750B mode, each timer has associated with it a reset register which may be loaded with any 16-bit value from software. If a timer is allowed to overflow, an automatic reset will take place which will reload the timer with the value held in its on-chip reset register, provided that the timer had previously been loaded using XIO OTA/OTB. If this is not the case then the timers will reset to zero on overflow. Each of the reset registers is initialised to zero but may be changed using XIO OTAR or XIO OTBR.

5.4 Fault Mask Register

A fault mask register is accessible in 1750B mode. Its function is similar to that of the Interrupt Mask register and allows selective enabling and disabling of all bits in the Fault Register. All faults are maskable. Setting a bit in this register allows the corresponding fault bit to be seen by the system. The register is loaded with all ones on initialisation.

6 Performance

6.1 Benchmarking

Figure 22 defines the number and type of machine cycles associated with each MIL-STD-1750A instruction. This information may be used when benchmarking MA31750 performance. The Digital Avionics Instruction Set (DAIS) mix, which defines a typical frequency of occurrence for MIL-STD-1750A instructions, is used here for this purpose.

One problem with the DAIS mix, however, is that it does not reflect the impact of data dependencies on system performance. For example, a multiplication in which the operand is zero may be performed much faster than one with two non-zero operands. Also, the DAIS mix does not specify such time consuming operations as normalization and alignment.

Realistic benchmarks must therefore take both the instruction mix and data dependencies into account. To this end, machine cycle counts in figure 22 which have data dependencies, are annotated with either an "a" or "wa" suffix.

An "a" suffix reflects an average number of machine cycles (where each of several possibilities is equally likely) and a "wa" suffix reflects a weighted average number of machine cycles (where some data possibilities are more likely than others).

Weighted averages are only applicable to floating-point operations. Weighted averages provided in figure 22 are based on the Sweeney (IBM) guidelines. These guidelines take a wide range of data dependencies into consideration. Normalization and alignment operations are also represented. Figure 18 shows MA31750 throughput, at various frequencies and wait states, for the DAIS mix using Sweeney data dependencies.

6.2 Expanded Memory Performance

The inclusion of an MMU (Memory Management Unit) will degrade the throughput performance of the processor in two ways. Firstly, each memory access will have an additional overhead associated with the formation of the extended address from the MMU. This may require that the system inserts wait states to lengthen each external cycle. Secondly, the MMU itself may require that some 'housekeeping' work be done by the processor, which will lengthen the program execution time.

No of waitstates	Frequency MHz			
	0	1	2	3
20	2.7	2.1	1.7	1.4
22	3.0	2.3	1.8	1.5
25	3.4	2.6	2.1	1.7

Figure 18. Throughput (MIPS) with waitstates.

There are no widely accepted benchmarks which may be used to measure the resultant decrease in throughput. The MA31751 MMU holds the references to the current instruction and operand pages in a fast translation-lookaside buffer which allows the extended address to be produced without having to add wait states, providing the current page has not been altered. If access to a different page is required then one wait state must be inserted into the first external cycle following the page register change. Note that if sequential code is being executed then one wait state will be inserted after each block of 4096 transfers (assuming no data waits).

6.3 Data Types

The MA31750 fully supports 16-bit fixed-point single-precision, 32-bit fixed-point double-precision, 32-bit floating-point, and 48-bit extended precision floating-point data types. Figure 19 depicts the formats of these data types.

All numerical data is represented in two's complement form. Floating-point numbers are represented by a fractional two's complement mantissa with an 8-bit two's complement exponent. All floating-point operands are expected to be normalised. If not normalised, the results from an instruction are not defined.

6.4 Addressing Modes

The MA31750 supports the eight addressing modes specified in MIL-STD-1750A. These addressing modes are depicted in figure 21 and are defined below.

6.4.1 Register Direct (R)
The register specified by the instruction contains the required operand.

6.4.2 Memory direct (D,DX)
Memory Direct (without indexing) is an addressing mode in which the instruction contains the memory address of the required operand. In Memory Direct-Indexed (DX), the memory address of the required operand is specified by the sum of the contents of an index register (RX) and the instruction address field (A). Register R1 through R15 may be specified for indexing.

6.4.3 Memory Indirect (I, IX)
Memory Indirect (without indexing) is an addressing mode in which the memory address specified by the instruction contains the address of the required operand. In Memory Indirect with Pre-Indexing (IX), the sum of the contents of a specified index register and the instruction address field in the address that contains the address of the required operand. Registers R1 through R15 may be specified for pre-indexing.

6.4.4 Immediate Long (IM, IMX)
There are two formats which implement Immediate Long Addressing; one allows indexing and one does not. For the indexable form, if the specified index register, RX, is not equal to zero, the contents of RX are added to the immediate field to form the required operand; otherwise, the immediate field contains the required operand.

6.4.5 Immediate Short (IS)
In this mode the required 4-bit operand is contained within the 16-bit instruction. The Immediate Short addressing mode accommodates two formats; one which interprets the contents of the immediate field as positive data and the other which interprets the contents of the immediate field as negative data.

6.4.6 Immediate Short Positive (ISP)
The immediate operand is treated as a positive integer between 1 and 16.

6.4.7 Immediate Short Negative (ISN)
The immediate operand is treated as a negative integer between -1 and -16. Its internal form is a two's complement, sign-extended 16-bit number.

6.4.8 Instruction Counter Relative (ICR)
This addressing mode is used for 16-bit branch instructions. The contents of the instruction counter minus two (the address of the current instruction) is added to the sign-extended 8-bit displacement field within the instruction. This sum then points to the memory address to which control will be transferred if the branch is taken.

6.4.9 Base Relative (B)

There are two formats which implement Base Relative Addressing; one allows indexing and one does not. For the non-indexable form, the contents of the instruction specified base register (BR = BR' + 12) is added to the 8-bit displacement field (DU) of the 16-bit instruction. In indexed mode, the sum of the contents of a specified index register and a specified base register forms the address of the required operand. Registers R1- R15 may be specified for indexing, whilst registers R12 - R15 may be specified as the base register.

6.4.10 Special

This addressing mode is applicable to instructions that do not follow the above formats. The instructions that use this special mode are indicated in figure 21.

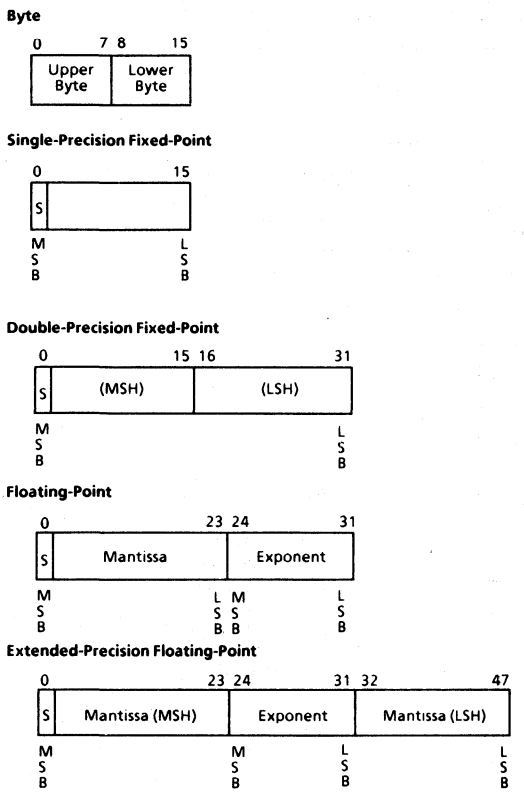


Figure 19. Data Formats

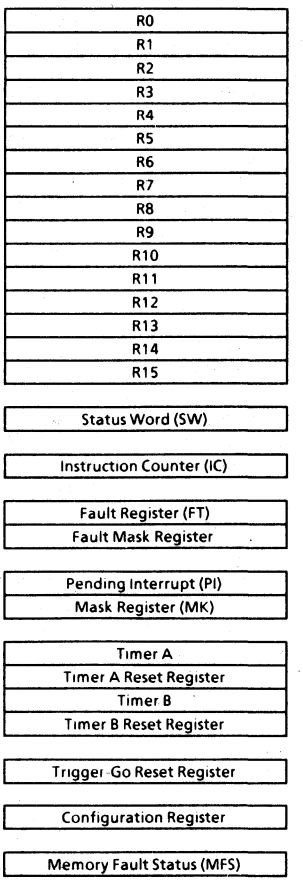


Figure 20. Register Set Model

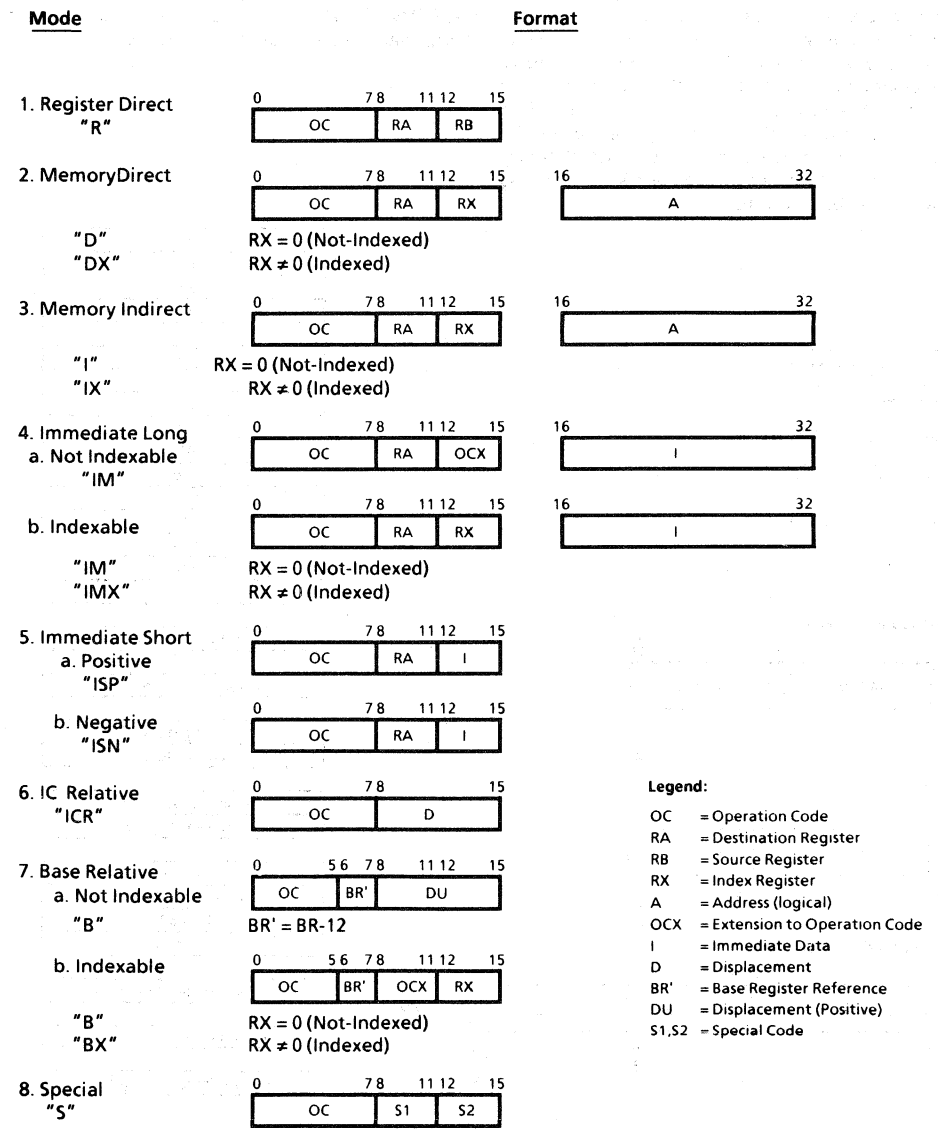


Figure 21. Addressing Modes

6.5 Instruction Summary

Operation	Mnemonic	Format	Op Code/Ext	Cycles *	
				M	P
LOAD/STORE					
Single Precision Load	LR	R	81	1	0
	LB	B	0X	2	1
	LBX	BX	4X 0	2	1
	LISP	ISP	82	1	0
	LISN	ISN	83	1	0
	L	D,DX	80	3	0
	LIM	IM,IMX	85	2	0
	LI	I,IX	84	4	0
Double-Precision Load	DLR	R	87	1	0
	DLB	B	0X	3	1
	DLBX	BX	4X 1	3	1
	DL	D,DX	86	4	0
	DLI	I,IX	88	5	0
Single-Precision Store	STB	B	0X	2	0
	STBX	BX	4X 2	2	1
	ST	D,DX	90	3	0
	STI	I,IX	94	4	0
Store a Non-Negative Constant	STC	D,DX	91	3	0
	STCI	I,IX	92	4	0
Double-Precision Store	DSTB	B	0X	3	0
	DSTX	BX	4X 3	3	1
	DST	D,DX	96	4	0
	DSTI	I,IX	98	5	0
Load Multiple Registers	LM	D,DX	89	3 + n	0
Store Multiple Registers	STM	D,DX	99	2 + n	1
INTEGER ARITHMETIC					
Single-Precision Integer Add	AR	R	A1	1	0
	AB	B	1X	2	1
	ABX	BX	4X 4	2	1
	AISP	ISP	A2	1	0
	A	D,DX	A0	3	0
	AIM	IM	4A 1	2	0
Increment Memory by a Positive Integer	INCM	D,DX	A3	4	0
Single-Precision Absolute Value of Register	ABS	R	A4	1	1.5a
Double-Precision Absolute Value of Register	DABS	R	A5	1	1.5a

*M = memory, P = processor (2 CLK cycles)
a = average if more than one alternative exists
n = number of registers specified by move instruction

Figure 22a. Instruction Summary

Operation	Mnemonic	Format	Op Code/Ext	Cycles *	
				M	P
Double-Precision Integer Add	DAR	R	A7	1	0
	DA	D,DX	A6	4	0
Single Precision Integer Subtract	SR	R	B1	1	0
	SBB	B	1X	2	1
	SBBX	BX	4X 5	2	1
	SISP	ISP	B2	1	1
	S	D,DX	B0	3	0
	SIM	IM	4A 2	2	0
Decrement Memory by a Positive Integer	DECM	D,DX	B3	4	0
Single Precision Negate Register	NEG	R	B4	1	1
Double-Precision Negate Register	DNEG	R	B5	1	1
Double-Precision Integer Subtract	DSR	R	B7	1	0
	DS	D,DX	B6	4	0
Single Precision Integer Multiply with 16-Bit Product	MSR	R	C1	1	1
	MISP	ISP	C2	1	1
	MISN	ISN	C3	1	2
	MS	D,DX	C0	3	1
	MSIM	IM	4A 4	2	1
Single Precision Integer Multiply with 32-Bit Product	MR	R	C5	1	0
	MB	B	1X	2	1
	MBX	BX	4X 6	2	1
	M	D,DX	C4	3	0
	MIM	IM	4A 3	2	0
Double-Precision Integer Multiply	DMR	R	C7	1	13.5a
	DM	D,DX	C6	4	13.5a
Single Precision Integer Divide with 16-Bit Dividend	DVR	R	D1	1	23.5a
	DISP	ISP	D2	1	23.5a
	DISN	ISN	D3	1	23.5a
	DV	D,DX	D0	3	23.5a
	DVIM	IM	4A 6	2	23.5a
Single Precision Integer Divide with 32-Bit Dividend	DR	R	D5	1	28a
	DB	R	1X	2	29a
	DBX	BX	4X 7	2	29a
	D	D,DX	D4	3	28a
	DIM	IM	4A 5	2	28a
Double-Precision Integer Divide	DDR	R	D7	1	41a
	DD	D,DX	D6	4	41a

*M = memory, P = processor (2 CLK cycles)
a = average if more than one alternative exists

Figure 22a. (continued). Instruction Summary

Operation	Mnemonic	Format	Op Code/Ext	Cycles *	
				M	P
LOGICAL					
Inclusive Logical OR	ORR	R	E1	1	0
	ORB	B	3X	2	1
	ORBX	BX	4X F	2	1
	OR	D,DX	E0	3	0
	ORIM	IM	4A 8	2	0
Logical AND	ANDR	R	E3	1	0
	ANDB	B	3X	2	1
	ANDX	BX	4X E	2	1
	AND	D,DX	E2	3	0
	ANDM	IM	4A 7	2	0
Exclusive Logical OR	XORR	R	E5	1	0
	XOR	D,DX	E4	3	0
	XORM	IM	4A 9	2	0
Logical NAND	NR	R	E7	1	0
	N	D,DX	E6	3	0
	NIM	IM	4A B	2	0
Set Bit	SBR	R	51	1	0
	SB	D,DX	50	4	0
	SBI	I,IX	52	5	0
Reset Bit	RBR	R	54	1	0
	RB	D,DX	53	4	0
	RBI	I,IX	55	5	0
Test Bit	TBR	R	57	1	0
	TB	D,DX	56	3	0
	TBI	I,IX	58	4	0
Test and Set Bit	TSB	D,DX	59	2	2.5a
Set Variable Bit in Register	SVBR	R	5A	1	0
Reset Variable Bit in Register	RVBR	R	5C	1	0
Test Variable Bit in Register	TVBR	R	5E	1	0
Store Register Through Mask	SRM	D,DX	97	4	1
BYTE					
Load From Upper Byte	LUB	D,DX	8B	3	1
	LUBI	I,IX	8D	4	1
Load From Lower Byte	LLB	D,DX	8C	3	0
	LLBI	I,IX	8E	4	0
Store Into Upper Byte	STUB	D,DX	9B	4	0
	SUBI	I,IX	9D	5	0
Store Into Lower Byte	STLB	D,DX	9C	4	1
	SLBI	I,IX	9E	5	1
Exchange Bytes in Register	XBR	S	EC	1	0

*M = memory, P = processor (2 CLK cycles)
a = average if more than one alternative exists

Figure 22a (continued). Instruction Summary

Operation	Mnemonic	Format	Op Code/Ext	Cycles *	
				M	P
COMPARE					
Single-Precision Compare	CR	R	F1	1	0
	CB	B	3X	2	1
	CBX	BX	4X C	2	1
	CISP	ISP	F2	1	1
	CISN	ISN	F3	1	0
	C	D,DX	F0	3	0
	CIM	IM	4A A	2	0
Compare Between Limits	CBL	D,DX	F4	4	2.7a
Double-Precision Compare	DCR	R	F7	1	0
	DC	D,DX	F6	4	0
JUMP/BRANCH					
Jump on Condition	JC	D,DX	70	3a	0
	JCI	I,IX	71	3.5a	0
Jump to Subroutine	JS	D,DX	72	2	1
Subtract One and Jump	SOJ	D,DX	73	3a	0
Branch Unconditionally	BR	ICR	74	2	1
Branch if Equal to (Zero)	BEZ	ICR	75	2a	0
Branch if Less than (Zero)	BLT	ICR	76	2a	0
Branch to Executive	BEX	S	77	11	14
Branch if Less than or Equal to (Zero)	BLE	ICR	78	2a	0
Branch if Greater than (Zero)	BGT	ICR	79	2a	0
Branch if Not Equal to (Zero)	BNZ	ICR	7A	2a	0
Branch if Greater than or Equal to (Zero)	BGE	ICR	7B	2a	0
SHIFT					
Shift Left Logical	SLL	R	60	1	0
Shift Right Logical	SRL	R	61	1	0
Shift Right Arithmetic	SRA	R	62	1	0
Shift Left Cyclic	SLC	R	63	1	0
Double Shift Left Logical	DSLL	R	65	1	0
Double Shift Right Logical	DSRL	R	66	1	0
Double Shift Right Arithmetic	DSRA	R	67	1	0
Double Shift Left Cyclic	DSLC	R	68	1	0
Shift Logical, Count in Register	SLR	R	6A	1	2
Shift Arithmetic, Count in Register	SAR	R	6B	1	5a
Shift Cyclic, Count in Register	SCR	R	6C	1	2
Double Shift Logical, Count in Register	DSLR	R	6D	1	2
Double Shift Arithmetic, Count in Register	DSAR	R	6E	1	5
Double Shift Cyclic, Count in Register	DSCR	R	6F	1	2

*M = memory, P = processor (2 CLK cycles)
a = average if more than one alternative exists

Figure 22a (Continued). Instruction Summary

Operation	Mnemonic	Format	Op Code/Ext	Cycles *	
				M	P
CONVERT					
Convert Floating-Point to 16-Bit Integer	FIX	R	E8	1	7.1a
Convert 16-Bit Integer to Floating-Point	FLT	R	E9	1	3
Convert Extended-Precision Floating-Point to 32-Bit Integer	EFIX	R	EA	1	8.5a
Convert 32-Bit Integer to Extended-Precision Floating-Point	EFLT	R	EB	1	9
STACK					
Stack IC and Jump to Subroutine	SJS	D,DX	7E	3	1
Unstack IC and return from Subroutine	URS	S	7F	3	1
Pop Multiple registers off the Stack	POPM	S	8F	1 + n (n = 0 to 15)	4
Push Multiple Registers onto the Stack	PSHM	S	9F	1 + n (n = 0 to 15)	8
I/O (See I/O Command Summary)					
Execute I/O	XIO**	IM,IMX	48	3	4.3a
Vectored I/O (n transfers)	VIO**	D,DX	49	2 + n	TBD
SPECIAL					
Move Multiple Words, Memory-to-Memory	MOV	S	93	1 + 2n	7
Exchange Words in Registers	XWR	R	ED	1	2
Load Status	LST**	D,DX	7D	6	1
	LSTI**	I,IX	7C	7	1
No Operation	NOP	S	FF	1	2
Break Point	BPT	S	FF	1	6

*M = memory, P = processor (2 CLK cycles)
a = average if more than one alternative exists
** Privileged instruction.
n = number of words to be transferred

Figure 22a (Continued). Instruction Summary

Operation	Mnemonic	Format	Op Code/Ext	Cycles *	
				M	P
FLOATING-POINT					
Extended-Precision Floating-Point Load	EFL	D,DX	8A	5	0
Extended-Precision Floating-Point Store	EFST	D,DX	9A	5	0
Floating-Point Absolute Value of Register	FABS	R	AC	1	2wa
Floating-Point Negate Register	FNEG	R	BC	1	3wa
Floating-Point Compare	FCR	R	F9	1	3.7wa
	FCB	B	3X	3	3.7wa
	FCBX	BX	4X D	3	3.7wa
	FC	D,DX	F8	4	3.7wa
Extended-Precision Floating-Point Compare	EFCR	R	FB	1	4wa
	EFC	D,DX	FA	5	2wa
Floating-Point Add	FAR	R	A9	1	7wa
	FAB	B	2X	3	8.5wa
	FABX	BX	4X 8	3	8.5wa
	FA	D,DX	A8	4	8.5wa
Extended-Precision Floating-Point Add	EFAR	R	AB	1	21wa
	EFA	D,DX	AA	5	20wa
Floating-Point Subtract	FSR	R	B9	1	9wa
	FSB	B	2X	3	10wa
	FSBX	BX	4X 9	3	10wa
	FS	D,DX	B8	4	9wa
Extended-Precision Floating-Point Subtract	EFSR	R	BB	1	23wa
	EFS	D,DX	BA	5	22wa
Floating-Point Multiply	FMR	R	C9	1	0
	FMB	B	2X	3	1
	FMBX	BX	4X A	3	1
	FM	D,DX	C8	4	0
Extended-Precision Floating-point Multiply	EFMR	R	CB	1	27wa
	EFM	D,DX	CA	5	26wa
Floating-Point Divide	FDR	R	D9	1	42.8wa
	FDB	B	2X	3	43.8wa
	FDBX	BX	4X B	3	43.8wa
	FD	D,DX	D8	4	42.8wa
Extended-Precision Floating-Point Divide	EFDR	R	DB	1	112.6wa
	EFD	D,DX	DA	5	112.6wa

*M = memory, P = processor (2 CLK cycles)
a = average if more than one alternative exists
wa = weighted average favouring one or more possible alternatives.

Figure 22a (Continued). Instruction Summary

Operation	Mnemonic	Format	Op Code/Ext	Cycles *	
				M	P
1750B MODE INSTRUCTIONS The following instructions may only be executed in 1750B mode - illegal in 1750A					
'LONG' LOADS AND STORES					
Long Load Single	LSL	S	CC	3	11
Long Load Double	LDL	S	CD	4	20
Long Load Extended Precision Floating Point	LEFL	S	CE	5	27
Long Store Single	LSS	S	DC	4	9
Long Store Double	LDS	S	DD	6	16
Long Store Extended Floating Point	LEFS	S	DE	8	23
UNSIGNED ARITHMETIC					
Unsigned Integer Add	UAR UA	R D, DX	AD AE	1 3	4 4
Unsigned Integer Subtract	USR US	R D, DX	BD BE	1 3	4 4
Unsigned Integer Compare	UCR UC UCIM	R D, DX IM	FC FD 4A 0	1 3 2	5 5 5
BYTE LOADS AND STORES					
Load Byte	LBY	S	BF	2	3
Load Byte With Increment	LBYI	S	AF	2	3
Store Byte	SBY	S	DF	2	3
Store Byte With Increment	SBYI	S	CF	2	3
MISCELLANEOUS					
Search First Bit Set	SFBS	R	95	1	3.75a

*M = memory, P = processor (2 CLK cycles)
a = average if more than one alternative exists

Figure 22b: MIL-STD-1750B Instruction Summary

6.6 I/O Comman Summary

Operation	Command Code (Hex)	Mnemonic
Implemented in MA31750 1750A or 1750B mode		
Set Fault Register	0401	SFR
Set Interrupt Mask	2000	SMK
Clear Interrupt Request	2001	CLIR
Enable Interrupts	2002	ENBL
Disable Interrupts	2003	DSBL
Reset Pending Interrupt	2004	RPI
Set Pending Interrupt Reg.	2005	SPI
Reset Normal Power Up Line	200A	RNS
Write Status Word	200E	WSW
Enable Start-Up ROM	4004	ESUR
Disable Start-Up ROM	4005	DSUR
Direct Memory Access Enable	4006	DMAE
Direct Memory Access Disable	4007	DMAD
Timer A Start	4008	TAS
Timer A Halt	4009	TAH
Output Timer A	400A	OTA
Reset Trigger-Go	400B	GO
Timer B Start	400C	TBS
Timer B Halt	400D	TBH
Output Timer B	400E	OTB
Read Configuration Word	8410	RCW
Read Fault Register,no Clear	8401	RFR
Read Interrupt Mask	A000	RMK
Read Pending Interrupt Reg.	A004	RPIR
Read Status Word	A00E	RSW
Read and Clear Fault Reg.	A00F	RCFR
Input Timer A	C00A	ITA
Input Timer B	C00E	ITB
MEDL Defined XIOs		
Write Internal config. word	040C	WCW
Read Fault Register (No clear)	8401	RFR
Read Linkage Pointer	8404	RLP
Read Processor Status	8405	RPS
Read OAS register	8406	ROS
Input Internal config. word	840C	ICW
Run Built In Test	840D	BIT
Read External Configuration	8410	RCW

Operation	Command Code (Hex)	Mnemonic
Implemented in MA31750 - 1750B mode only		
Output Timer A Reset Reg.	4002	OTAR
Output Timer B Reset Reg.	400F	OTBR
Input Timer A Reset Register	C002	ITAR
Input Timer B Reset Register	C00F	ITBR
Set Fault Mask	2006	SFMK
Write Page Bank Select	200F	WPBS
Read Page Bank Select	A00C	RPBS
Read Fault Mask	A006	RFMK
Implemented in BPU		
Memory Protect Enable	4003	MPEN
Load Memory Protect RAM	50XX	LMP
Read Memory Protect RAM	D0XX	RMP
Load Ext. Mem. Protect RAM	4XXX	LXMP
Read Ext. Mem. Protect RAM	CXXX	RXMP
Implemented in MMU		
Write Instruction Page Reg.	51XY	WIPR
Write Operand Page Reg.	52XY	WOPR
Read Memory Fault Status	A00D	RMFS
Read Instruction Page Reg.	D1XY	RIPR
Read Operand Page Reg.	D2XY	ROPR
Console Mode		
Console Output	4000	CO
Console input	C000	CI
Clear Console	4001	CLC
Reserved by MEDL (Not available to the user)		
Initialise PIC	0403	PICINIT
Load OAS register	0406	LOS
Set NPU	040A	RNPU

Figure 22c. Internal I/O Command Summary

7 Timing Diagrams

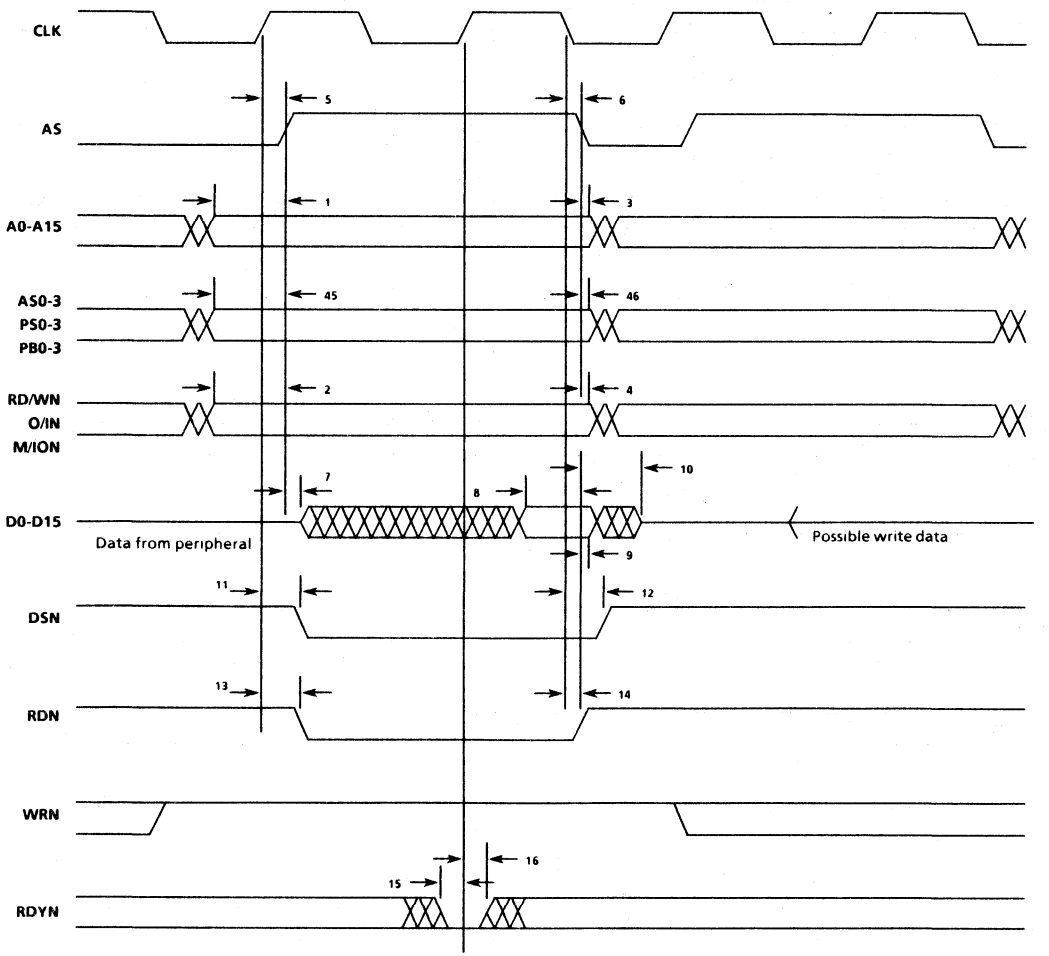


Figure 23: Read Cycle Timing

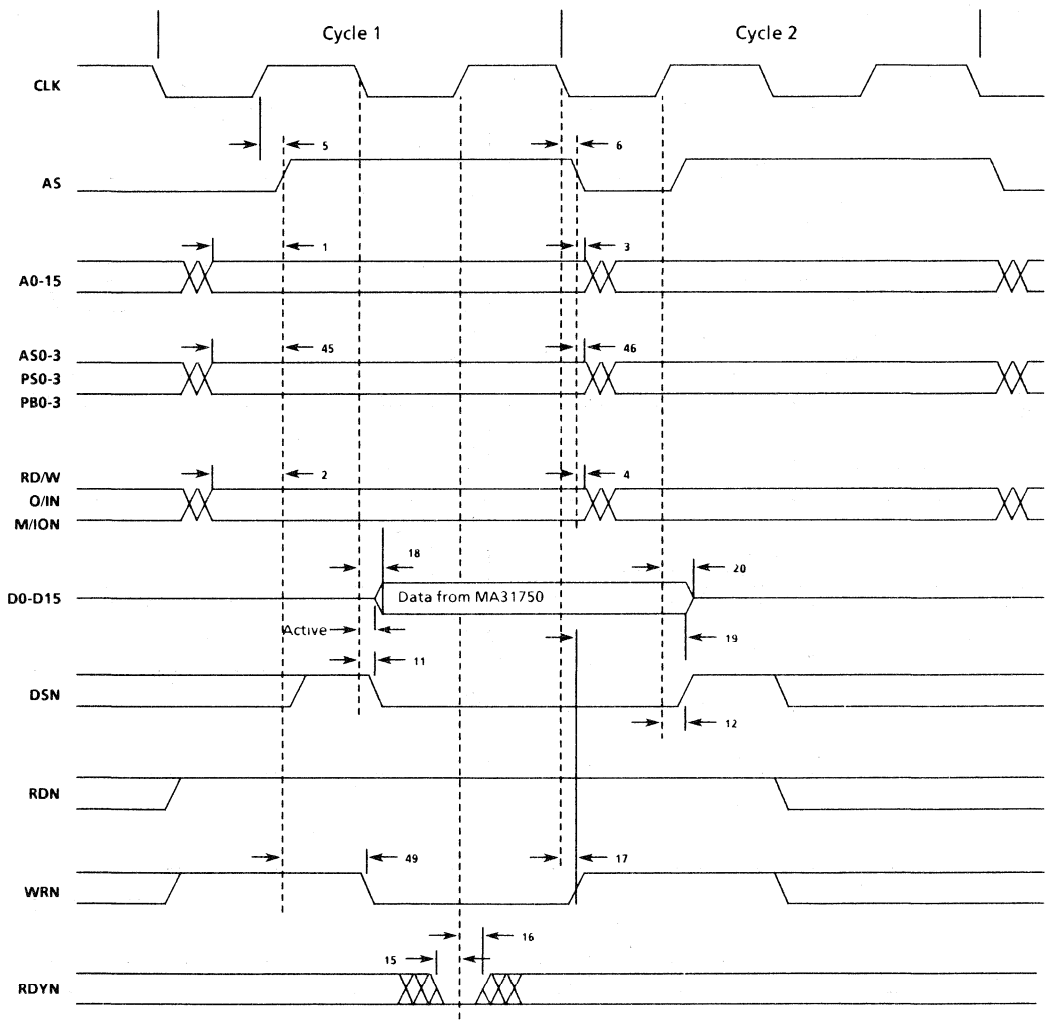


Figure 25: Write Cycle Timing

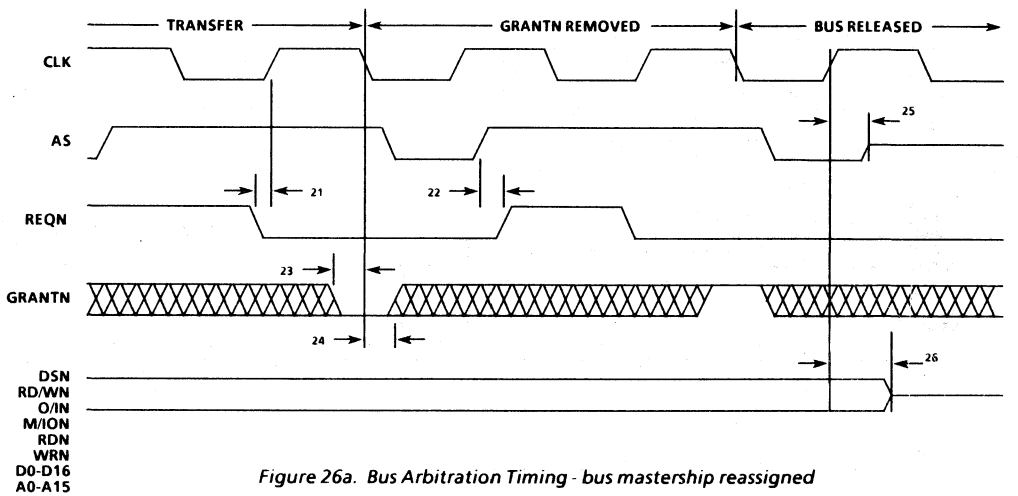


Figure 26a. Bus Arbitration Timing - bus mastership reassigned

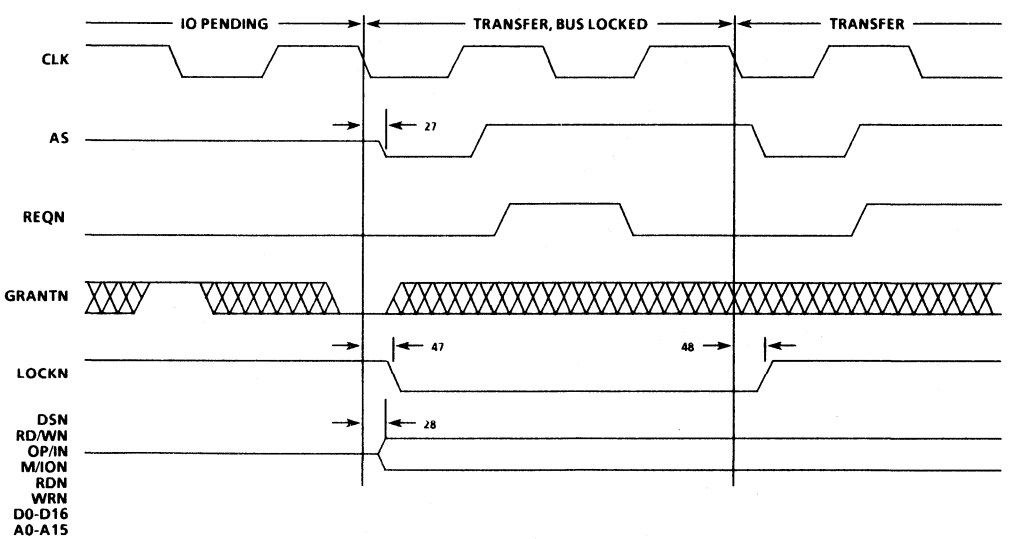


Figure 26b. Bus Arbitration Timing - processor becoming bus master

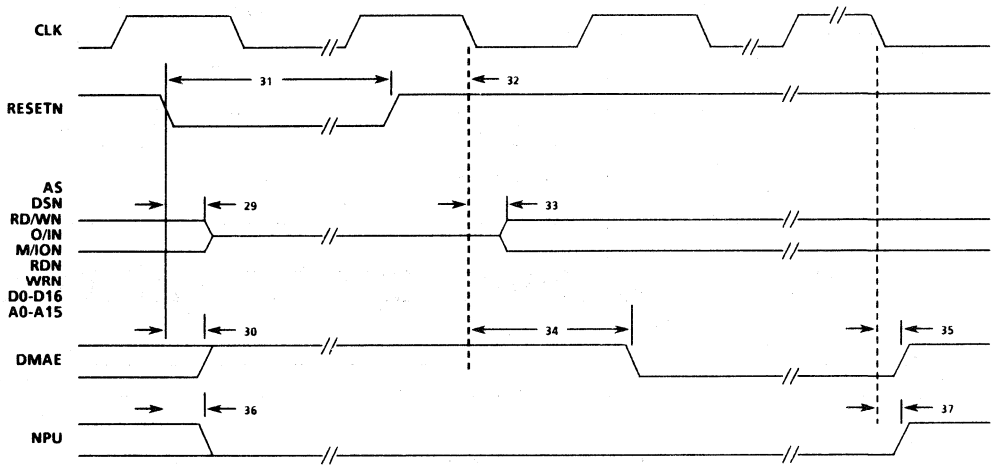


Figure 27. Reset Timing

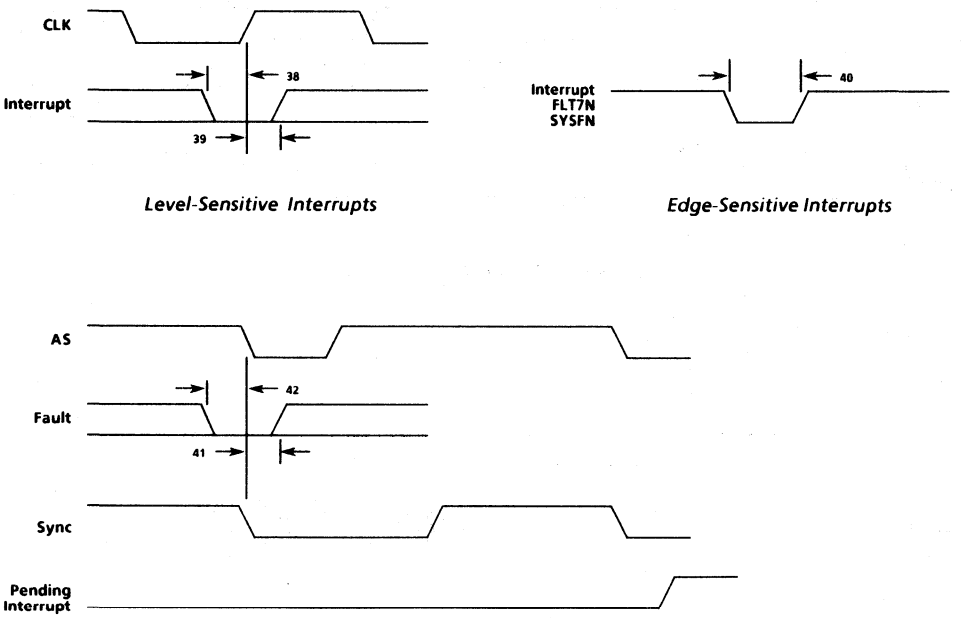


Figure 28. External Interrupt and Fault timing

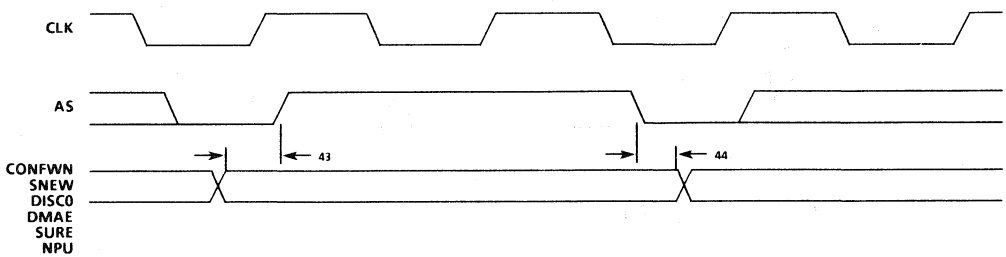


Figure 29. Discrete Output Timing

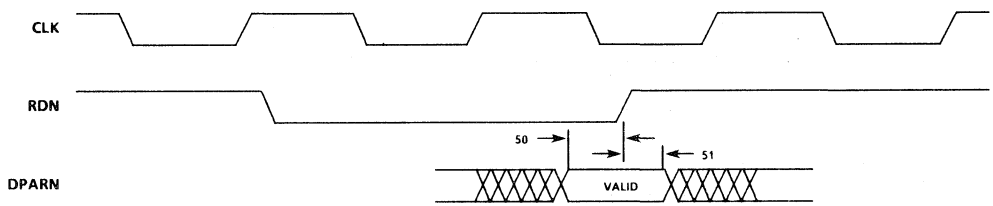


Figure 30. DPARN Input Timing

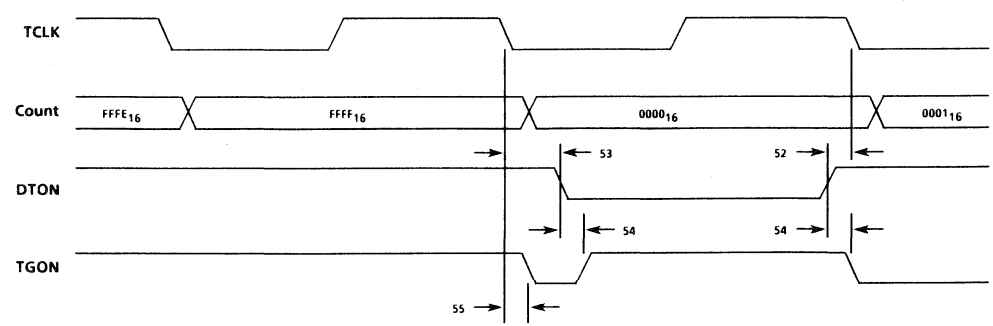


Figure 31. Trigger-Go Timing

8 Preliminary Timing Parameters

NO.	Parameter	Min.	Typ.	Max.	Units
1	Address valid to AS ↑	-	10	-	ns
2	RD/WN, OP/IN & M/ION valid to AS ↑	-	10	-	ns
3	Address hold after AS ↓	-	5	-	ns
4	RD/WN, OP/IN & M/ION valid after AS ↓	-	5	-	ns
5	AS ↑ from CLK ↑	-	10	-	ns
6	AS ↓ from CLK ↓	-	10	-	ns
7	AS ↑ to data bus low-Z (read)	5	-	-	ns
8	Data setup to RDN ↑ (read)	10	-	-	ns
9	Data hold after RDN ↑ (read)	-	-	0	ns
10	RDN ↑ to data bus high-Z (read)	-	-	30	ns
11	CLK ↓ to DSN ↓	-	10	-	ns
12	CLK ↑ to DSN ↑	-	10	-	ns
13	CLK ↑ to RDN ↓	-	10	-	ns
14	CLK ↓ to RDN ↑	-	-	5	ns
15	RDYN setup to CLK ↑	0	-	5	ns
16	RDYN hold after CLK ↑	0	-	5	ns
17	CLK ↓ to WRN ↑	-	10	-	ns
18	Data valid from CLK ↑	10	-	-	ns
19	Data valid after WRN ↑	20	-	-	ns
20	CLK ↓ to data bus high-Z (write)	-	-	15	ns
21	REQN ↓ to CLK ↑	0	-	-	ns
22	REQN ↑ from AS ↑	0	-	5	ns
23	GRANTN setup to CLK ↓	-	-	10	ns
24	GRANTN hold after CLK ↓	-	-	0	ns
25	CLK ↑ to AS high-Z	-	-	15	ns
26	CLK ↑ to control lines and busses high-Z	-	-	15	ns
27	CLK ↓ to AS low-Z	-	-	10	ns
28	CLK ↓ to control lines and busses low-Z	-	-	10	ns
29	RESETN ↓ to control lines and busses high-Z	-	-	10	ns
30	RESETN ↓ to DMAE ↑	-	-	10	ns
31	RESETN ↓ to RESETN ↑	3	-	-	CLK
32	RESETN ↑ setup to CLK ↓	10	-	-	ns
33	CLK ↓ to control lines and busses low-Z	-	-	10	ns
34	CLK ↓ to DMAE ↓	-	-	50	ns

Figure 32. Timing Parameters - PRELIMINARY INFORMATION ONLY

High performance MIL-STD-1750 Microprocessor

(Advance Data)

Preliminary Timing Parameters (continued)

NO.	Parameter	Min.	Typ.	Max.	Units
35	CLK ↓ to DMAE ↑ (following XIO DMAE)	-	10	-	ns
36	RESETN ↓ to NPU ↓	-	10	-	ns
37	CLK ↓ to NPU ↑ (following successful power-up)	-	10	-	ns
38	Interrupt setup to CLK ↑	10	-	-	ns
39	Interrupt hold after CLK ↑	0	-	-	ns
40	Interrupt pulse width (edge-sensitive)	10	-	-	ns
41	Fault setup to AS ↓	10	-	-	ns
42	Fault hold after AS ↓	0	-	-	ns
43	Discretes valid after AS ↑	-	10	-	ns
44	Discretes valid after AS ↓	-	10	-	ns
45	AS0-3, PS0-3, PB0-3 valid to AS ↑	-	10	-	ns
46	AS0-3, PS0-3, PB0-3 invalid after AS ↓	-	10	-	ns
47	LOCKN ↓ from CLK ↓	10	-	-	ns
48	LOCKN ↑ from CLK ↓	10	-	-	ns
49	AS ↑ to WRN ↓	-	25	-	ns
50	DPARN setup to RDN ↑	10	-	-	ns
51	DPARN hold after RDN ↑	0	-	10	ns
52	DTON setup to TCLK ↓	0	-	10	ns
53	DTON hold after TCLK ↓	0	-	10	ns
54	DTON to TGON	0	-	15	ns
55	TCLK ↓ to TGON ↓	0	-	15	ns

Figure 32 (continued). Timing Parameters - PRELIMINARY INFORMATION ONLY

NOTE: Timing parameters shown are preliminary and should be used as a guide only. Accurate timings will be available following full device characterisation.

9 Ratings and Characteristics

Parameter	Min.	Max.	Units
Supply voltage	-0.5	10	V
Input voltage	-0.3	V_{DD} + 0.3	V
Current through any pin	-20	20	mA
Operating temperature	-55	125	°C
Storage temperature	-65	150	°C

Figure 33: Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Symbol	Parameter	Conditions	Total dose radiation not exceeding $3x10^5$ Rad (Si)			Total dose ≤1 MRad (Si)		Units
			Min.	Typ.	Max.	Min.	Max.	
V_{DD}	Supply voltage	-	4.5	5.0	5.5	4.5	5.5	V
V_{IH1}	TTL input high voltage	-	2.0	-	-	2.0	-	V
V_{IL1}	TTL input low voltage	-	-	-	0.8	-	0.3	V
V_{CKH1}	CLK input high voltage	-	V_{DD}-0.5	-	V_{DD}	-	-	V
V_{CKL1}	CLK input low voltage	-	0.0	-	0.5	-	-	V
V_{OH1}	Output high voltage	I_{OH} = -0.8mA	2.4	-	-	2.4	-	V
V_{OL1}	Output low voltage	I_{OL} = 2.0mA	-	-	0.4	-	0.4	V
I_{IL}	Input low current	-	-	-	10	-	100	uA
I_{IH}	Input high current	-	-	-	10	-	100	uA
I_{DDYN}	Dynamic power supply current	-	-	-	100	-	100	mA

V_{DD} = 5V ± 10%, over full operating temperature range.

Figure 34: Operating DC Electrical Characteristics

Parameter	Min.	Max.	Units
Clock Frequency CLK	0	25	MHz
Clock Duty Cycle	45	55	%

Figure 35: Operating AC Electrical Characteristics

10 Pin Assignments and Outlines

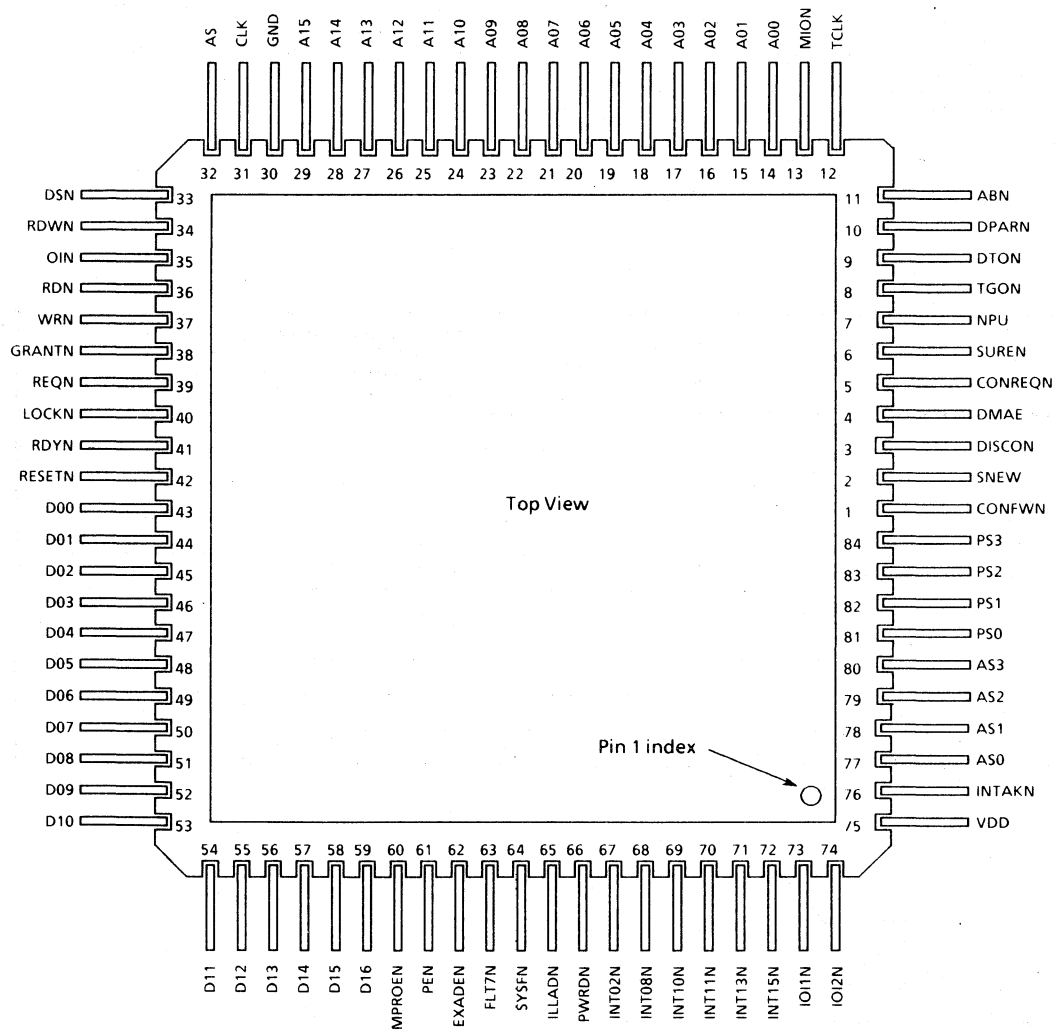
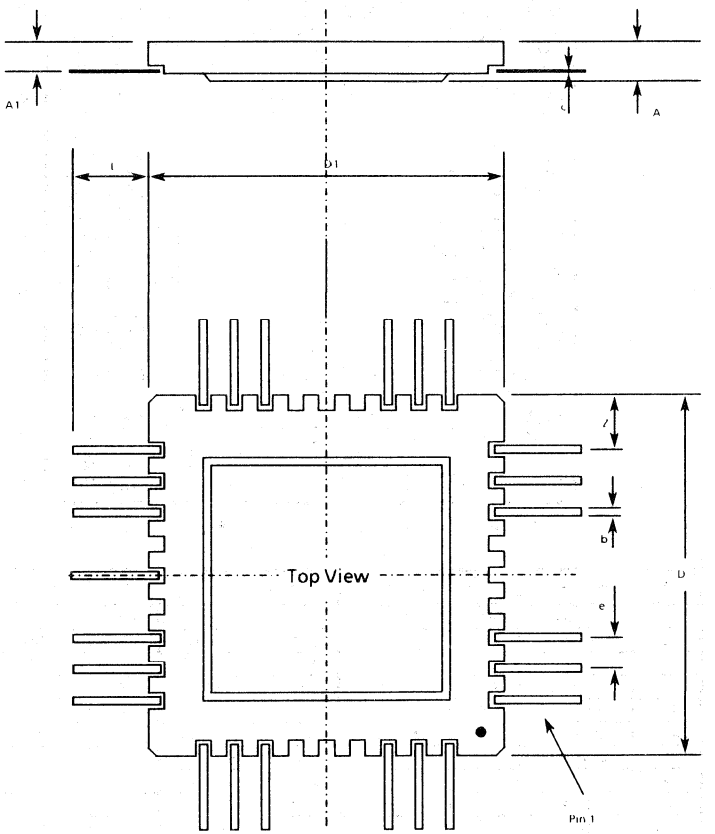


Figure 36: 84-Lead Flatpack Style F

MA31750

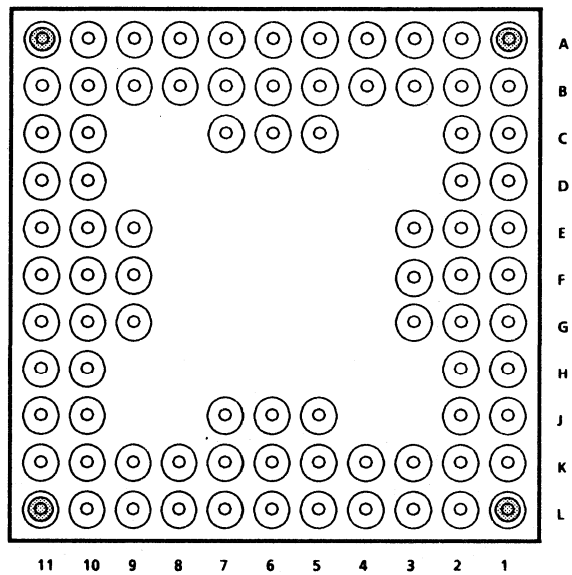
High performance MIL-STD-1750 Microprocessor

(Advance Data)



Ref.	Inches		
	Max.	Nom.	Min.
A	0.081	-	-
A1	0.044	-	0.036
b	0.020	-	0.017
c	0.012	-	0.009
D, D1	1.173	-	1.149
e	-	0.050	-
L	0.325	-	0.290

XG524



Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	IOI2N	B11	D08	F9	D00	K2	TCLK
A2	INT15N	C1	AS1	F10	RESETN	K3	MION
A3	INT13N	C2	INTAKN	F11	D04	K4	A02
A4	INT10N	C5	ILLADN	G1	DISCON	K5	A05
A5	PWRDN	C6	SYSFN	G2	DMAE	K6	A04
A6	INT08N	C7	MPROEN	G3	CONREQN	K7	A11
A7	EXADEN	C10	D09	G9	REQN	K8	A14
A8	D16	C11	D07	G10	LOCKN	K9	CLK
A9	D14	D1	AS3	G11	RDYN	K10	DSN
A10	D13	D2	AS2	H1	SUREN	K11	OIN
A11	D10	D10	D06	H2	NPU	L1	ABN
B1	AS0	D11	D05	H10	WRN	L2	A00
B2	VDD	E1	PS2	H11	GRANTN	L3	A01
B3	IOI1N	E2	PS1	J1	TGON	L4	A03
B4	INT11N	E3	PS3	J2	DPARN	L5	A06
B5	INT02N	E9	D01	J5	A07	L6	A09
B6	FLT7N	E10	D03	J6	A08	L7	A10
B7	PEN	E11	D02	J7	A12	L8	A13
B8	D15	F1	SNEW	J10	RDWN	L9	A15
B9	D12	F2	PS0	J11	RDN	L10	GND
B10	D11	F3	CONFWN	K1	DTON	L11	AS

XG640

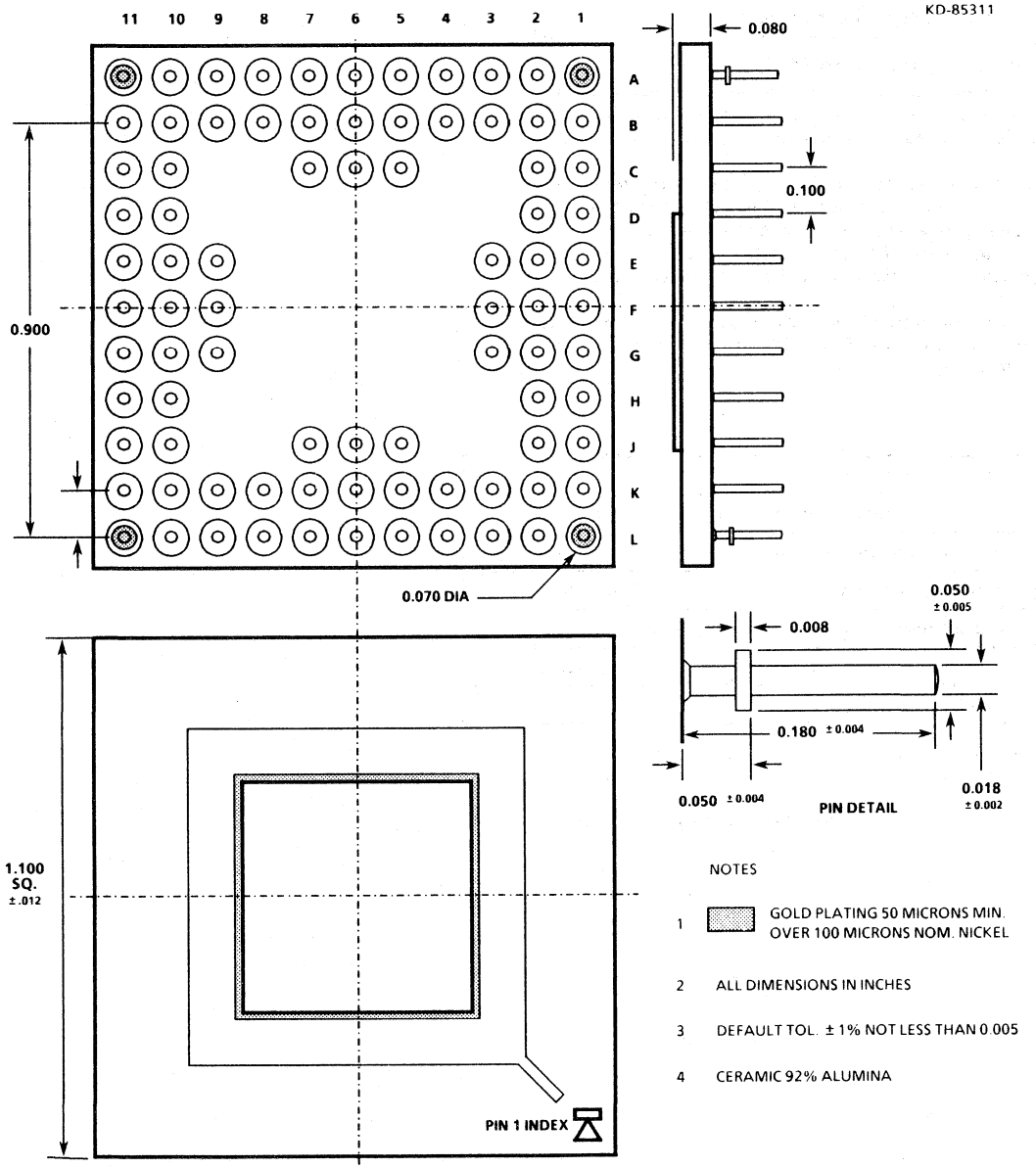
Figure 37: 84-Pin Grid Array Style A

MA31750

High performance MIL-STD-1750 Microprocessor

(Advance Data)

KD-85311



NOTES

1. GOLD PLATING 50 MICRONS MIN. OVER 100 MICRONS NOM. NICKEL
2. ALL DIMENSIONS IN INCHES
3. DEFAULT TOL. ± 1% NOT LESS THAN 0.005
4. CERAMIC 92% ALUMINA

11 Radiation Tolerance

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

Total Dose (Function to specification) - note 1	$1x10^6$ Rad(Si)
Total Dose (Function to specification) - note 2	$3x10^5$ Rad(Si)
Transient Upset (stored data loss)	$3x10^{10}$ Rad(Si)/sec
Transient Upset (survivability)	$>10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	10^{15}neutrons/cm^2
Single Event Upset (GSO 10% worst case)	$<10^{-10}$ errors/bitday
Latch-up	Not possible

Note 1: All CMOS inputs
Note 2: TTL inputs

Figure 40: Radiation Hardness Parameters

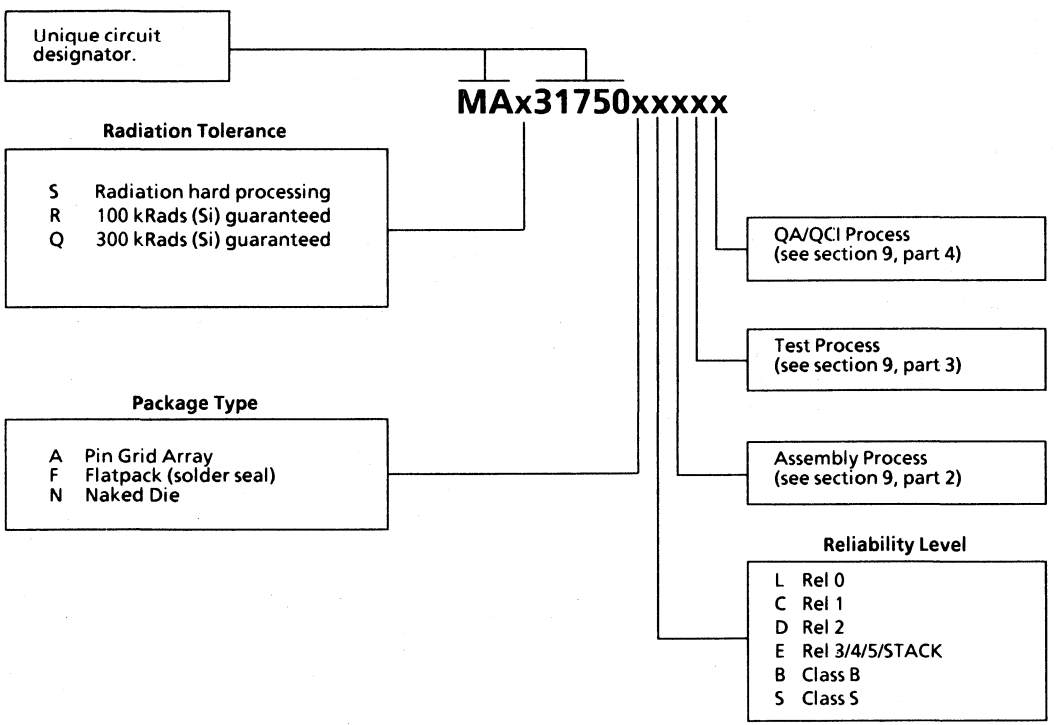
MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

12 Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



GEC PLESSEY

SEMICONDUCTORS

MAS281

MIL-STD-1750A Microprocessor

C465D Issue 1.3 May 1989

Features

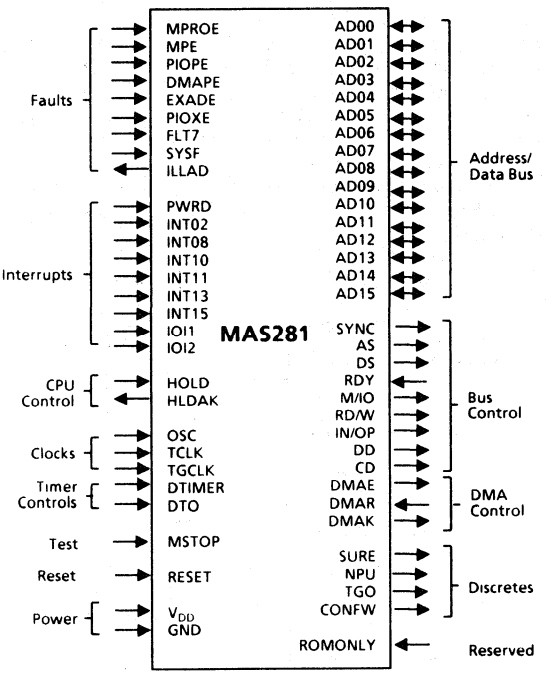
- MIL-STD-1750A 16-Bit Microprocessor
- Full Performance over Military Temperature Range (-55°C to +125°C)
- Radiation Hard CMOS/SOS Technology
- Performance Optimised Architecture
  - Parallel Multiplier/Accumulator
  - 32-bit Barrel Shifter
  - Instruction Pre-Fetch
  - Multi-Port Register File
- Implements MIL-STD-1750A Options
  - Timers A and B
  - Trigger-Go Counter
  - Start-Up ROM Interface
- 64 K-word Address Space Expandable to 1 M-word with Optional MMU

General Description

The Marconi MAS281 Microprocessor is a MIL-STD-1750A (Notice 1), 16-bit Central Processing Unit (CPU). It consists of three CMOS/SOS large-scale integration (LSI) chips: the MA17501 Execution Unit (EU), the MA17502 Control Unit (CU), and the MA17503 Interrupt Unit (IU). These three units are mounted on, and interconnected within a 64-pin ceramic substrate. The microprocessor is also available as a 3-chip set without the ceramic substrate (see ordering information on page 59).

The MAS281 is optimised for real-time I/O and arithmetic intensive operations. Key performance-enhancing features include a parallel multiplier/accumulator, 32-bit barrel shifter, instruction pre-fetch queue, and multi-port register file. Additional features include a comprehensive Built-In-Test (BIT), interval timers A and B, trigger-go counter, and Start-Up ROM interface.

Block Diagram



In accordance with MIL-STD-1750A, the MAS281 supports a 64K-word address space. An optional MA17504 Memory Management Unit/Block Protect Unit (MMU(BPU)) chip may be added externally to expand this address space to 1M-words or add a 1K-word memory block protection capability.

The MAS281 is offered in several screening grades which are described in this document. For availability of speed grades, please contact Marconi Electronic Devices.

Radiation Hard MIL-STD-1750A Microprocessor

1.0 Architecture

The Marconi MAS281 Microprocessor is a high performance implementation of the MIL-STD-1750A (Notice 1) instruction set architecture. It consists of three custom CMOS/SOS Large Scale Integration chips - referred to as the Execution Unit, Control Unit, and Interrupt Unit - mounted on, and interconnected within, a 64-pin, dual in-line ceramic substrate. Figure 1 depicts the interconnection of these chips via the substrate while Figure 2 depicts the architectural details within each chip.

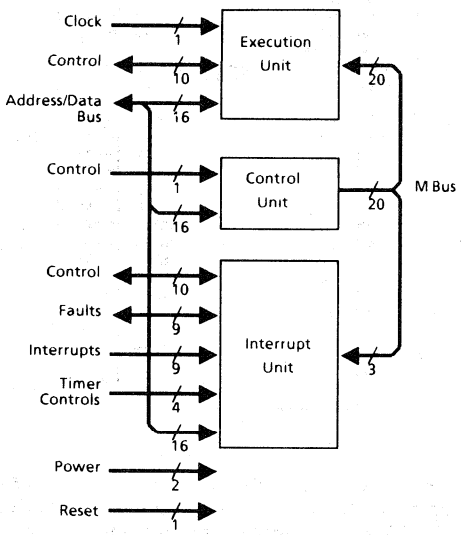


Figure 1: MAS281 Microprocessor Block Diagram.

The MAS281 architecture has been optimised for both real time I/O and arithmetic intensive operations. Two key features of this architecture which contribute to the overall high performance of the MAS281 are; a barrel shifter and a parallel multiplier/accumulator. These subsystems allow the MAS281 to perform multi-bit shifts, multiplications, divisions, and normalisations in a fraction of the clock cycles required on machines not having such resources. This is especially true of floating-point operations, in which the MAS281 excels. Such operations constitute 16% of the Digital Avionics Instruction Set (DAIS) mix and a generally much higher percentage of many signal processing algorithms, therefore having a significant impact on system performance.

In accordance with MIL-STD-1750A, the MAS281 can access a 64K-word address space. With the addition of an external Marconi MA17504 chip configured as a Memory Management Unit (MMU), this address space may be expanded to a full one megaword. Furthermore, this configuration provides write and access lock and key protection down to 4K-word blocks. By adding a second MA17504 configured as a Block Protect Unit (BPU), write protection may be extended down to 1K-word blocks. For those applications not requiring adherence to the address space requirements of MIL-STD-1750A, the MAS281 may be optionally configured with up to one megaword each of instruction and command space.

In addition to implementing all of the required features of MIL-STD-1750A, the MAS281 also incorporates a number of optional features. Interval timers A and B as well as a trigger-go counter are provided. Most specified XIO commands are decoded directly on the module and an additional set of commands, associated with MMU and BPU operations, are directly decoded on the MA17504 chip. Those commands not directly decoded are output for decoding by external logic in accordance with the XIO and VIO protocols of MIL-STD-1750A.

1.1 Execution Unit (EU)

The EU provides the computational resources for the MAS281. Key features include: (1) a three-bus (R, S, and Y) data path consisting of an arithmetic/logic unit (ALU), three-port register file, barrel shifter, parallel multiplier/accumulator, and status register; (2) instruction fetch registers IC, IA, and IB; (3) operand transfer registers A, DI, and DO; (4) a state sequencer; and (5) microinstruction decode logic. A brief description of these features follows:

1.1.1 Arithmetic/Logic Unit (ALU)

A full function 16-bit ALU is used to perform arithmetic and logic operations on one or two 16-bit operands in a single machine cycle. The ALU supports 16-bit fixed-point single-precision, 32-bit fixed-point double-precision, 32-bit floating-point, and 48-bit floating-point extended precision data in two's complement form. The ALU generates several machine flags which reflect the outcome of its operations. These flags are stored in the condition status (CS) field of the status register.

1.1.2 Three Port Register File

A 24-word by 16-bit wide register file is used to store operands, addresses, base pointers, stack pointers, indexes, and temporary values. Registers R0 through R15 are general purpose and user accessible in accordance with MIL-STD-1750A; remaining registers are accessible only by microcode. Wrap-around concatenation of R0 through R15 allows 32- and 48-bit operands to be stored. The three-port architecture allows two 16-bit operands to be read and a third 16-bit operand to be written simultaneously.

1.1.3 Parallel Multiplier/Accumulator

This multiplies a 24-bit multiplicand by a 4-bit multiplier and accumulates the product in a single machine cycle. Only four iterations through the multiplier are required to complete a 16-bit by 16-bit multiply.

1.1.4 Barrel Shifter

This shifter is a 32-bit input, 16-bit output right-shift network. The barrel shifter allows multibit shifts to be accomplished in a single machine cycle and is used by the microcode for all shift, rotate, and normalise operations.

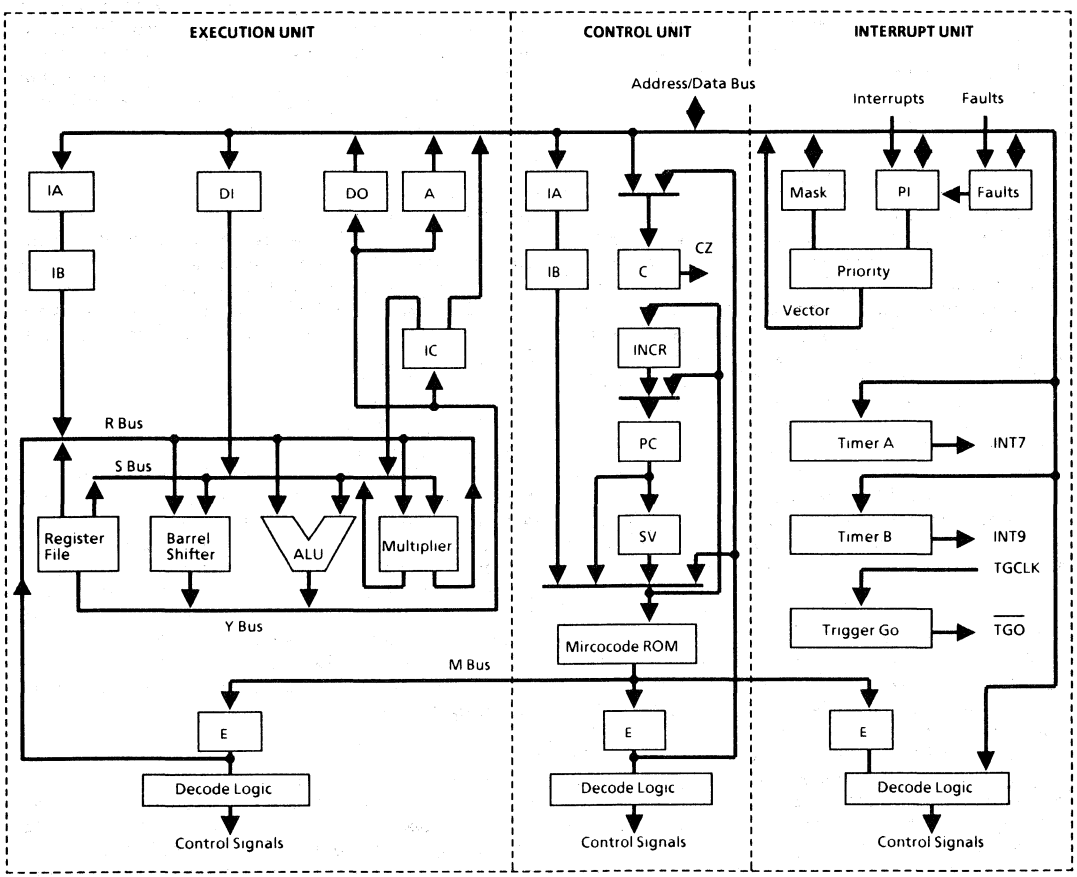
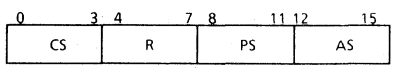


Figure 2: MAS281 Architecture



Field	Bits	Description
CS		CONDITION STATUS:
	0	C- Carry from an addition or no borrow from a subtraction
	1	P- Result >0
	2	Z- Result = 0
	3	N- Result<0
R	4 - 7	RESERVED
PS	8 - 11	PROCESSOR STATE: (a)- Memory access key code (b)- Privileged instruction enable
AS	12 - 15	ADDRESS STATE: Page register sets for expanded memory addressing

Figure 3: Status Word Format

1.1.5 Status Register
This 16-bit register holds the condition status (CS) bits C, P, Z, and N; the 4-bit address state (AS) field; and the 4-bit processor state (PS) field. The CS bits are updated after each logical, shift, and arithmetic operation performed by the ALU. The CU interrogates these bits during conditional operations to determine which course of action to follow. The AS field is used during expanded memory access to define the page register set to be used for instruction and operand memory references. The PS field is used during memory protect operations to define the access key used for memory accesses. The PS field is also used during execution of privileged instructions. PS must be zero for such operations to be legal. Figure 3 depicts the status register format.

1.1.6 State Sequencer
The EU utilises a state machine, clocked by the system oscillator, to generate processor timing and control signals. These signals constitute the lowest level of control available within the module, and provide the framework for basic operations, such as selecting the next microinstruction to be executed, sequencing bus control signals to effect a memory transfer, or performing an operation within the ALU. Each complete pass through the state machine corresponds to one such operation and constitutes a machine cycle.

A machine cycle requires five or more oscillator cycles to complete with the exact number determined by the type of operation being performed. Internal processor operations, excluding internally decoded XIO commands, require either five or six oscillator cycles, the former associated with sequential microcode execution and the latter with microcode branches. Internally decoded XIO commands require a minimum of six oscillator cycles to complete. External processor operations require a minimum of five oscillator cycles to complete.

The internal ready signal is generated by the IU whenever an internally decoded XIO command is detected. An external ready interface is provided which allows external machine cycles to be extended when interfacing with slow devices. The external ready signal is provided by external logic and must be asserted in order to conclude the machine cycle

1.1.7 Operand Transfer Registers
The Address (A), Data In (DI), and Data Out (DO) registers serve to buffer transfers between the data path and the Address/Data (AD) bus. These registers are used under microcode control and are not directly accessible by software. A description of the use of these registers during memory and I/O operations is provided in section 3.0.

1.1.8 Instruction Fetch Registers
The Instruction Counter (IC), Instruction A (IA), and Instruction B (IB) registers allow sequential instruction fetches to be performed without the assistance of the ALU. The IC register, which holds a 16-bit address and points to the next instruction to be fetched, is loaded indirectly via reset, jump, or branch operations. Once loaded, it uses a dedicated counter to sequence from one instruction to the next. IA and IB serve as an instruction pipeline with IA storing the next instruction to be executed. DI also plays a role by storing any immediate operands. Use of these registers during instruction fetches is described in section 3.0.

1.1.9 Microcode Control Logic
All EU operations are performed under microcode control. As depicted in Figure 2, microinstructions are provided by the CU over the M bus, buffered by the Execution (E) register, and decoded to generate various control signals.

1.2 Control Unit (CU)

The CU provides microprogrammed control of all MAS281 operations. It features a microsequencer, a microcode storage ROM, and an instruction mapping ROM. A brief description of these features follows:

1.2.1 Microsequencer

This 12-bit wide microcode address generator controls all microcode ROM accesses. The microsequencer features a program counter (PC) which points to the next sequential microinstruction, a program counter save register (SV) to save return addresses for microsubroutines, address increment logic (INCR), instruction pipeline registers (IA and IB), a next address multiplexer, a loop counter (C), and various miscellaneous systems.

The microsequencer controls the execution of each MIL-STD-1750A, or macro, instruction by stepping through its corresponding microcode sequence. If the macroinstruction is a conditional, the CS bits of the status word will be interrogated to determine the necessary course of action. At the completion of each macroinstruction, the microsequencer checks to see if a Hold request or an interrupt is pending. If so, the microsequencer will branch to the appropriate microinstruction sequence. If not, the microsequencer begins sequencing the next macroinstruction.

Note that the microsequencer is itself under the control of the EU state sequencer. Each processor machine cycle corresponds to the execution of a single microinstruction.

1.2.2 Microcode ROM

This is a 2k- (2048) word by 40-bits/word ROM which stores the microinstructions that implement the MIL-STD-1750A instruction set. The address of the next microinstruction to be accessed is generated by the microsequencer. The accessed microinstruction is output to the M-bus and broadcast to the EU and IU. In addition to the microinstruction sequences corresponding to the MIL-STD-1750A instructions, the microcode ROM also stores sequences for performing initialisation, interrupt response, Hold response, instruction prefetch, built-in-test (BIT), and BIFs.

1.2.3 Instruction Mapping ROM

This is a 512-word by 8-bits/word ROM which is used during microcode branches.

1.3 Interrupt Unit (IU)

The IU incorporates a pending interrupt register, a mask register, a priority encoder, a fault register, two interval timers (A and B), a trigger-go counter, XIO command decode logic, and microcode control logic. A brief description of these features follows:

1.3.1 Pending Interrupt Register (PI)

This 16-bit register is used to capture and hold interrupts until they can be processed by software. PI supports three dedicated external, six user-definable external, and seven dedicated internal interrupts. Interrupts are captured at the beginning of each machine cycle and are stored using a logic 1 to represent a pending interrupt. Anti-repeat logic is provided to prevent multiple captures of the same interrupt.

1.3.2 Mask Register (MK)

This 16-bit register is used to store the interrupt mask. Interrupts are masked by ANDing each mask bit with its corresponding PI register bit. Interrupts which are masked will be captured in the PI register but will not be acted on until unmasked. Interrupt level 0 can not be masked. A logic 0 in a given bit position indicates that the corresponding bit in the PI register will be masked.

1.3.3 Priority Encoder

This encoder generates an interrupt request to the CU whenever one or more unmasked interrupts are pending and enabled in the PI and encodes the highest priority unmasked pending interrupt as a 4-bit vector. This vector is read by the EU over the AD bus during interrupt servicing in order to create the interrupt Linkage and Service pointers.

1.3.4 Fault Register

This 16-bit register is used to capture and hold both internal and user implemented external faults. Faults are captured at the beginning of each machine cycle and are stored using positive logic, i.e., a logic "1" represents a fault. Setting any one or more faults in FT will cause a level 1 (machine error) interrupt request. Once a fault is set in FT, it may only be cleared via an XIO command.

1.3.5 Timers A and B

These are two 16-bit software controllable timers. Timer A is clocked by the TCLK input while Timer B is clocked by the internally generated TCLK/10. Timers A and B will generate interrupt levels 7 and 9, respectively, when their maximum counts of 65,536 are reached.

1.3.6 Trigger-Go Counter
This 16-bit counter is clocked by the TGCLK input, is enabled during system initialisation, and may be reset but not stopped by software action. It is stopped, however, upon overflow or by assertion of the DTIMERN input. Upon overflow, the TGON discrete output goes low and stays low until the counter is reset by software. This counter is typically used as a system "watchdog" timer.

1.3.7 XIO Command Decode Logic
This logic decodes all internally supported XIO commands and generates the control signals necessary to carry out the commanded action. An internal ready signal is generated upon command detection and is used by the EU state sequencer as previously discussed. Table 7b in Section 4.0 identifies the XIO commands which are internally supported by the MAS281.

1.3.8 Microcode Control Logic
Decode logic, which translates microcode received from the CU into control signals, is used both by the MAS281 and by the external system.

2.0 Interface Signals

2.1 Pin Assignments
Figure 4 defines the pin assignment for the MAS281 module. See section 10.0 for full packaging and pin assignment information.

All signals - with the exception of power, ground and ROMONLYN - are TTL compatible. In addition, each function is provided with Electrostatic Discharge (ESD) protection circuitry. Figure 5 depicts a typical system implementation using many of these signals. Throughout this data sheet, active low signals are denoted either by placing a bar over the signal name, or by following the signal name with an "N" suffix, e.g., DDN. If a signal has a dual function, both function names will be used separated by a "/". The function name to the left of the "/" will be active high while the function to the right will be active low, again with an "N" suffix, e.g., RD/WN.

2.2 Pin Functions
A description of each pin function follows. The function name is presented first, followed by its acronym and description. Function type is either input, output, high impedance (Hi-Z), or a combination thereof. Full timing characteristics of each of the functions are shown in section 6.0.

2.2.1 Power and Ground (VDD & GND)
The MAS281 utilizes a single VDD power supply. A single-point ground is provided for the three chips on the substrate and is brought out on two module pins.

2.2.2 Oscillator (OSC)
This input clocks the EU state sequencer which, in turn, generates timing and control signals for the rest of the module. To minimize skew between OSC edges and signals derived from OSC, and thereby optimize system performance, the OSC rise and fall times should be minimised. It is recommended that a clock driver with a high drive capability, such as a 54AS244, 54ALS244 or 54HST244, be used. In order to avoid double clocking due to line reflections, a 500- to 1000-ohm pull-up resistor placed close to the module is recommended.

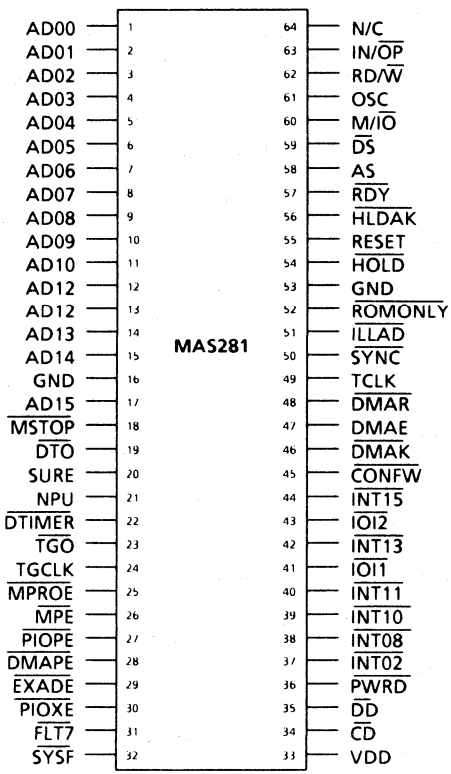


Figure 4: Pin Assignments

2.2.3 Synchronization Clock (SYNC)
This active low output transitions from high to low to signal the start of a new machine cycle. It should be used as a timing reference for those operations which must be synchronized to the basic machine cycle.

SYNCN cycles associated with external memory or I/O bus transactions are a minimum of five OSC periods in duration and may be extended by inserting wait states via the external ready interface. For such cycles, a SYNCN low indicates that either an address or XIO command is on the AD bus; a high indicates data is on the bus. Wait states extend the high state of SYNCN.

SYNCN cycles associated with internal CPU operations, are either five or six OSC periods in duration. Six OSC periods are required for machine cycles associated with microcode branches or with the execution of internally decoded XIO commands. Five OSC periods are required for all other internal operations.

[Note: For modules operating at high OSC frequencies, the internal ready logic provided on the IU may cause a wait state to be inserted during execution of internal XIO commands. This would result in a SYNCN cycle of seven OSC periods duration. Though unlikely, this condition must be taken into account in implementing an external ready interface. Refer to the description of the Ready (RDYN) signal below for further details.]

SYNCN continues to cycle during DMA and HOLD states. Such cycles are five OSC periods in duration.

2.2.4 Address Strobe (AS)
Output/Hi-Z. This active high signal indicates that an address has been placed on the AD bus. This address is guaranteed valid at the high to low transition of AS. AS should be used to strobe an address latch during AD bus demultiplexing. This latch should be a transparent type for optimum performance. AS is placed in the high impedance state during DMA and Hold cycles and is held low during internal (non-XIO) operations.

2.2.5 Data Strobe (DS)
Output/Hi-Z. This active low signal indicates that the AD bus is being used for data transfers.

During read operations, DSN should be used by the selected external device to enable data onto the AD bus. This data is guaranteed valid on the low to high transition of DSN. The selected external device should use the low to high edge of DSN to perform the write. DSN is placed in the high impedance state during DMA and Hold cycles and is held high during internal (non-XIO) operations.

2.2.6 Read/Write (RD/W)
Output/Hi-Z. This dual function signal indicates the direction of data flow on the AD bus. A high level indicates a read operation with data being input to the module. A low level indicates a write operation with data being output by the module. RD/WN may be combined with DSN to generate separate read and write strobes. This signal goes valid shortly after SYNCN goes low to indicate the start of a new machine cycle and remains valid until a new SYNCN cycle is begun RD/WN is placed in the high impedance state during DMA and Hold cycles.

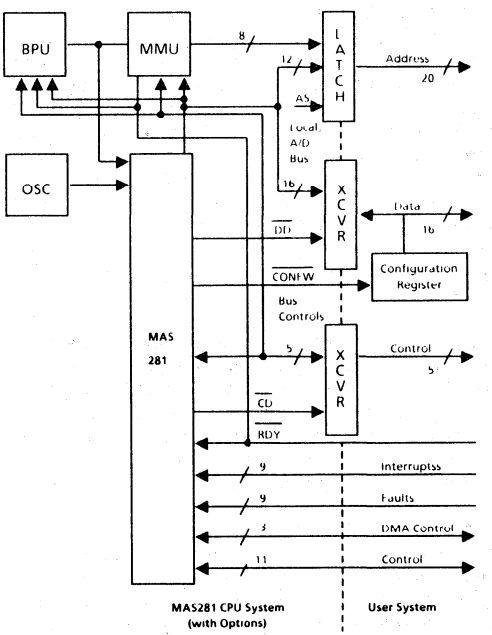


Figure 5: Typical MAS281/MA17504 System Interface

2.2.7 Memory/Input-Output (M/IO)
Output/Hi-Z. This dual function signal indicates the type of transfer of the AD bus that is occurring. A high state identifies memory transfers. A low state identifies I/O transfers. M/ION goes valid shortly after SYNCN goes low to indicate the start of a new machine cycle and remains valid until a new SYNCN cycle is begun. M/ION is placed in the high impedance state during DMA and Hold cycles and is held high during internal (non-XIO) operations.

2.2.8 Instruction/Operand (IN/OP)
Output/Hi-Z. This dual function signal indicates the type of data on the AD bus during the data portion of a SYNCN cycle. A high state identifies an instruction while a low state identifies an operand. IN/OPN goes valid shortly after SYNCN goes low to indicate the start of a new SYNCN cycle and remains valid until a new SYNCN cycle is begun. This signal is required during expanded memory accesses. IN/OPN is placed in the high impedance state during DMA and Hold cycles.

2.2.9 Address/Data Bus (AD00 - AD15)
Input/Output/Hi-Z. AD00 through AD15 comprise a bidirectional multiplexed address and data bus which serves both as the communication path between the external system and module as well as the communication path among the three chips on the module. It is important to note that the AD bus is shared between the external system and internal module resources. To avoid bus contention during internal operations, the AD bus must be isolated from the external system through the use of a bus transceiver. A data direction signal (DDN) is provided for transceiver control.

Addresses, data & commands appearing on the AD bus are represented in positive logic. A high level indicates a logic 1 and a low level indicates a logic 0. AD00 is the most significant bit position whilst AD15 is the least significant bit position. The AD bus is placed in the high impedance state during the data portion of a read SYNCN cycle as well as during DMA and Hold cycles.

2.2.10 Ready (RDY)
This asynchronous active low input is used by the EU state sequencer, in conjunction with the internal ready signal, to determine when the current machine cycle may be completed. By holding RDYN high, wait states may be inserted, stretching out the current machine cycle and allowing slower devices sufficient time to complete their operations.

Since the internal ready logic may request a wait state when the module is executing an internal XIO command, as discussed above under SYNCN, it is important that the external ready logic not override the internal ready logic. To this end, it is recommended that an external ready only be generated when an external device is specifically addressed.

[Note: If RDYN is held high during two consecutive TCLK high-to-low transitions (with DSN low), a bus timeout fault will occur and will be indicated in the appropriate bit in the fault register. The occurrence of this fault will cause the EU state sequencer to terminate the current machine cycle, drop SYNCN low, and begin a new machine cycle. Also, the presently executing macroinstruction will be aborted and execution will branch, unless masked, to the machine error interrupt (level 1) software routine. The DTON signal may be used to override this feature.]

2.2.11 Control Direction (CD)
This active low output goes high to indicate the module is driving the AS, DSN, M/ION, RD/WN and IN/OPN signals. During DMA and Hold cycles, this signal goes low to indicate the module has relinquished control of these signals and has placed them in the high impedance state. The DMA or Console controller, respectively, may then drive these signals. This signal should be used to control the transfer direction of the control signal transceiver.

2.2.12 Data Direction (DD)
This active low signal indicates the direction of data transfer on the AD bus. This signal goes high to indicate a write transfer from the module to the external system. It also goes high during all internal module operations. DDN goes low to indicate a read transfer from the external system to the module. It also goes low during DMA and Hold cycles as well as during configuration register reads.

[Note: In addition to going high during the execution of internally implemented XIO commands, DDN also goes high during execution of XIO commands which are implemented in the MA17504 MMU(BPU) chip.

If an MA17504 is used with the MAS281, it must reside on the MAS281 local AD bus rather than the system buses (see Figure 5). Table 7b in Section 4.0 identifies those XIO commands which are implemented in the MA17504].

2.2.13 Direct Memory Access Enable (DMAE)
This active high output goes high in responce to the DMAE XIO command. A high state indicates DMA requests will be acknowledged; a low state indicates a DMA request will be ignored.

2.2.14 Direct Memory Access Request (DMAR)
A low on this asynchronous active low input will cause the processor to suspend internal operations at the end of the current machine cycle. This request will only be acknowledged by the module when DMAE is high.

2.2.15 Direct Memory Access Acknowledge (DMAK)
This active low signal goes low in response to a DMA request if DMAE is high. A low state grants use of the system busses to the requesting DMA device by placing the module's AD bus, AS, DSN,RD/WN, M/ION and IN/OPN drivers into the high impedance state and by pulling CDN and DDN low. The high-to-low transition is synchronized to the falling edge of SYNCN to ensure that the current machine cycle is completed before the DMA device is granted the bus. DMAKN will remain low until the requesting device raises DMARN.

2.2.16 Hold Request (HOLD)
A low on this asynchronous active low input will cause the module to suspend internal processor functions at the end of the currently executing MIL-STD-1750A instruction. A Hold state is also entered if the processor encounters a breakpoint (BPT) instruction and the configuration word indicates the presence of a Console (bit 15 = 0).

2.2.17 Hold Acknowledge (HLDAK)
This active low output goes low either upon completion of the MIL-STD-1750A instruction during which HOLDN went low or if the processor encounters a breakpoint (BPT) instruction with Console present indicated in the configuration word register. A low on this signal indicates to the requesting device that that the module AD bus, AS, DSN, M/ION, RD/WN, and IN/OPN drivers have been placed in the high impedance state. The Hold state is terminated either by raising HOLDN high or, in the case of a BPT caused Hold, by pulsing HOLDN low and high again (see Section 6.0).

2.2.18 System Reset (RESET)
This asynchronous active high input should be raised high to reset the module. The high-to-low transition of this input will start the module's initialization.

2.2.19 Start-Up ROM Enable (SURE)
This active high output goes high during initialization and may also be asserted by software with the ESUR XIO command. This signal remains high until removed by software via the DSUR XIO command. When a Start-Up ROM is present, This signal should be used to qualify its chip select or output enable input such that the ROM may be accessed only when SURE is high.

[NOTE: Instruction pipelining must be considered in transitioning from Start-Up ROM to RAM when using the DSUR XIO command. If a system overlays RAM with the Start-Up ROM and transitions to execution from RAM by simply executing DSUR from the ROM, then IA will contain the value stored in the ROM location immediately following DSUR. This value will be treated as an instruction and the module will attempt to execute it. In such cases, it is recommended that DSUR be followed by an unconditional branch instruction with offset, i.e., the BR instruction. An alternative approach is simply to jump to a portion of RAM not overlaid by the Start-Up ROM and execute DSUR from RAM.]

2.2.20 Configuration Word (CONFW)
This active low output goes low when the module reads the external configuration register and should be used as that register's output enable strobe (see Section 6.0). Table 1 defines the required format of the configuration register. A zero in a given bit position indicates the specified device is present. Bits 0 through 11 are not used by the module.

The configuration register is read during initialization to determine the system configuration. It is also read whenever a (BPT) instruction is executed to determine the presence of a Console. If a console is not present, a BPT will be interpreted as a NOP. DDN goes low during a

Bit	Device
15	Console
14	MMU
13	BPU
12	Output Discrete Register
11-0	Unused

Table 1: Configuration Register Bit Assignment

configuration register read. Thus, the configuration register must reside on the system AD bus rather than the local AD bus (see Figure 5).

2.2.21 Normal Power Up (NPU)
This active high output is dropped low during module initialization as the first step of BIT. If BIT is successful, NPU goes high and remains high until reset by software via the RNS XIO command. NPU cannot be set high by software.

2.2.22 Timer Clock (TCLK)
This clock input is used by interval timers A and B as well as the interface fault timer. Timer A is clocked at the TCLK frequency while timer B is clocked at a frequency of TCLK/10. MIL-STD-1750A requires that this input be a 100kHz pulse train.

2.2.23 Trigger-Go Clock (TGCLK)
This clock input is used by the internal 16-bit trigger-go counter. The trigger-go counter counts at the same frequency as TGCLK.

2.2.24 Trigger-Go Discrete (TGO)
This active low output goes low whenever the trigger-go counter overflows, i.e., the counter rolls over to 0000. It returns to the high state when the trigger-go counter is reset by software via the GO XIO command.

2.2.25 Disable Timer (DTIMER)
A low on this active low input disables timers A and B as well as the trigger-go counter. A low also disables DMA access by forcing DMAE low and DMAKN high. Raising DTIMERN allows timers A and B and the trigger-go counter to resume counting from the value at which they were stopped. A high also allows normal DMA operation.

2.2.26 Disable Timeout (DTO)
A low on this active low input will reset and disable the bus fault timeout circuitry.

2.2.27 Power Down Interrupt (PWRD)
A low on this active low input is captured in the PI register by a SYNCN high-to-low transition. This sets pending interrupt 0. This is the highest priority interrupt and cannot be masked or disabled.

2.2.28 User Interrupts (INT02, 08, 10, 11, 13 and 15)
A low on any of these active low inputs will be captured in the PI register by a SYNCN high-to-low transition and will set pending interrupt levels 2, 8, 10, 11, 13, and 15, respectively. Level 2 is the highest priority user level while level 15 is the lowest priority. These interrupts are maskable and can be disabled. Unused inputs should be pulled up to VDD.

2.2.29 I/O dedicated Interrupts (IOI1 & IOI2)
A low on either IOI1N or IOI2N will be captured in the PI register by a SYNCN high-to-low transition and will set pending interrupt levels 12 and 14, respectively. Unused inputs should be pulled up to VDD.

[NOTE: Interrupt levels 1, 3, 4, 5, 6, 7, and 9 are dedicated to internal machine interrupts.]

2.2.30 Memory Protect Error (MPROE)
A low on this active low input, captured by the SYNCN high-to-low transition, is used to inform the module that an access fault, execute protect, or write protect violation has been detected. Bit 0 of the module Fault Register (FT) is set if this signal goes low during a memory cycle; bit 1 is set if it goes low during a DMA cycle. Either condition immediately sets pending interrupt level 1 and in the case of a memory cycle error, causes the currently executing MIL-STD-1750A instruction to be aborted.

Although the MAS281 aborts the macroinstruction, system memory management, and / or block protect hardware is responsible for preventing the erroneous bus cycle from accessing memory. To effectively use this feature, MPROEN should be pulled low prior to the high-to-low SYNCN transition of the next machine cycle. This can easily be accomplished by injecting wait states to hold off the DSN rising edge (write cycle) and the SYNCN falling edge (read cycle) until the system protection circuitry can decide whether or not to allow the transaction.

2.2.31 Memory Parity Error (MPE)
A low on this active low input, captured by the SYNCN high-to-low transition, is used to inform the module that a parity error has been detected during a memory transfer. Bit 2 of the module Fault Register (FT) is set when this signal goes low. This, in turn, causes pending interrupt level 1 to be set.

2.2.32 Programmed I/O Parity Error (PIOPE)
A low on this active low input, captured by the SYNCN high-to-low transition, is used to inform the module that a parity error has been detected during an external I/O transfer. Bit 3 of the module Fault Register (FT) is set when this signal goes low. This, in turn, causes pending interrupt level 1 to be set.

2.2.33 DMA Parity Error (DMAPE)
A low on this active low input, captured by the SYNCN high-to-low transition, is used to inform the module that a parity error has been detected during a DMA data transfer. Bit 4 of the module Fault Register (FT) is set when this signal goes low. This, in turn, causes pending interrupt level 1 to be set.

2.2.34 External Address Error (EXADE)
A low on this active low input, captured by the SYNCN high-to-low transition ,is used to inform the module that a system address error has been detected. Bit 8 of the module Fault Register (FT) is set when this signal goes low during a memory fault; bit 5 is set if it goes low during an I/O fault. As with MPROEN, either condition immediately sets pending interrupt level 1 and causes the currently executing MIL-STD-1750A instruction to be aborted.

2.2.35 Programmed I/O Transfer Error (PIOXE)
A low on this active low input, captured by the SYNCN high-to-low transition, is used to inform the module that a programmed I/O data transfer error has been detected. Bit 6 of the module Fault Register (FT) is set when this signal goes low. This, in turn, causes pending interrupt level 1 to be set.

2.2.36 Fault #7 (FLT7)
A low on this active low input, captured by the SYNCN high-to-low transition, sets bit 7 of the Fault Register (FT). This is a user definable fault.

2.2.37 System Fault (SYSF)
A low on this active low input, captured by the SYNCN high-to-low transition, sets bits 13 and 15 of the Fault Register (FT). This is a user definable fault.

2.2.38 Illegal Address (ILLAD)
This active low output drops low if the EXADEN input drops low or if the bus fault timeout circuit causes an interface timeout. When extended memory is implemented, the MA17504 MMU uses ILLADN to trigger the Memory Fault Status Register (MFSR).

2.2.39 Microcode Stop (MSTOP)
MSTOPN allows microcode to be single-stepped and is reserved for use by Marconi Electronic Devices. MSTOPN must be pulled up to V_{DD} in customer applications.

2.2.40 ROM Only (ROMONLY)
ROMONLYN is used for testing by Marconi Electronic Devices and must be pulled up to V_{DD} in customer applications.

3.0 Operating Modes

MAS281 operating modes include: (1) initialisation, (2) instruction execution, (3) interrupt servicing, (4) fault servicing, (5) DMA support, (6) Hold support, and (7) timer operations.

3.1 Initialisation

The module executes a microcoded initialisation routine in response to a hardware reset. This routine clears module registers, disables and masks interrupts, reads the configuration register, resets the output discrete register (if implemented), initialises the MMU and BPU (if implemented), performs Built-In-Test (BIT), raises the Start-Up ROM enable discrete, clears and starts timers A and B, resets the trigger-go counter, and loads the instruction pipeline. Table 2 summarises the resulting initialisation state, and Table 3 provides a detailed breakdown of the initialisation sequence.

BIT consists of five subroutines, as outlined in table 4, and begins by pulling NPU low. This is the first time after reset that NPU is guaranteed low. If all five subroutines execute successfully, NPU is raised high. If any part of BIT fails, an error code identifying the failed subroutine is loaded into the Fault Register (FT), BIT is aborted, and NPU is left in the low state. Table 4 defines the coding of BIT results in FT. In the event of such a failure, the resulting module reset state will be dependent on where in BIT the error occurred and may not be the same as that shown in Table 2. A BIT failure indication in FT will set the level 1 interrupt request bit of the Pending Interrupt (PI) register. Since initialisation disables and masks interrupts, this interrupt request will not be asserted.

The last action performed by the initialisation routine is to load the instruction pipeline. Instruction fetches start at memory location zero and will be from the Start-Up ROM if implemented. Whether BIT passes or not, the processor will begin instruction execution at this point.The system start-up code may include a routine to enable and unmask interrupts in order to detect and respond to a BIT failure.

[NOTE: To complete initialisation and pass BIT, interrupt and fault inputs must be high for the duration of the initialisation routine. Also, timers A and B must be clocked during this interval, i.e., TCLK must be applied.]

MAS281	
Instruction Counter (IC)	Zeroed
Status Word (EU and MMU) (SW)	Zeroed
Fault (FT)	Zeroed
Pending Interrupt (PI)	Zeroed
Mask (MK)	Zeroed
General Register File (R0 - R15)	Zeroed
Interrupts	Disabled
DMA Access	Disabled
Timer A	Reset and Started
Timer B	Reset and Started
Trigger-Go Timer	Reset and Started
MMU	
Page Registers	Group 0 Enabled
AL, W, E Fields	Zeroed
PPA Field	Logical to Physical Map
BPU	
Write Protect	Zeroed
Global Memory Protect	Enabled

Table 2: Initialisation State

3.2 Instruction Execution

Once initialisation has been completed, the module will begin instruction execution. Instruction execution is characterised by a variety of operations, each one or more machine cycles in duration. Depending on the instruction being executed at the time, these operations include: (1) internal CPU cycles, (2) instruction fetches, (3) operand transfers, and (4) input/output transfers. Instruction execution may be interrupted at the end of any individual machine cycle by DMA operations and at the conclusion of any given instruction by an interrupt or Hold request.

Label	Cycle	
MAIN	B1	1. Enable Control of DMAE Output signal
	P	2. -
	B1	3. Clear MAS281 Execution Unit Status Word (SW) Clear Interrupt Mask (MK) (Internal I/O command, SKM, 2000H)
	B1	4. Clear Pending Interrupt Register (PI) and Fault Register (FT) (Internal I/O Command, CLIR, 2001H) Clear Instruction Counter (IC)
	P	5. -
	B1	6. Disable Interrupts (Internal I/O Command, DSBL, 2003H)
	P	7. -
	B1	8. Clear MMU Status Word (Internal I/O Command, WSW, 200EH) (Note 1)
	P	9. -
	B1	10. Disable DMA Access (Internal I/O Command, DMAD, 4007H)
	P	11. -
	B1	12. Read Configuration Register (Internal I/O Command,RCW, 8400H, CONFWN Drops low per Figure 25, Section 5.0)
	P	13. -
	P	14. -
	B2	15. - (If Output Discrete Register Present, then Continue; Else, Skip to 18.)
	p	(16). -
	I/O	(17). Clear Output Discrete Register (External I/O Command)
	P	18. -
	B2	19. - (If BPU present, then Branch to BPU; else, continue)
	P	20. -
	B2	21. - (If MMU present, then Branch to MMU; Else, Continue)
	p	22. -(Setup Temporary Register to indicate No MMU Present)
	B2	23. -(Branch to MAS281 BIT)
	P	24. -
	B1	25. Enable Start-Up ROM (Internal I/O Command, ESUR, 4004H; SURE Raises High per Figure 25, Section 5.0)
	P	26. -
	B1	27. Clear and Start Timer A (Internal I/O Command, OTA, 400AH)
	B1	28. Reset the Trigger-Go timer (Internal I/O Command, GO, 400BH)
	P	29. -
	B1	30. Clear and Start Timer B (Internal I/O Command, OTB, 400EH)
	B2	31. -(Branch to Load Instruction Pipeline Routine)
	M	32. Load data-In register (DI) and instruction Register A (IA) from [IC], Increment IC
	M	33. Load Data-In Register (DI) and Instruction Register a (IA) from [IC] ([IA] Moves to IB), Increment IC, Map Instruction Register B (IB) into Microcode Routine
BPU	P	(1). -
	P	(2). -(Set Loop to Clear Memory Protect RAM)
	I/O	(3). Clear a Location in MPRAM (Internal I/O Command, LMP, 50XXH), Increment Address; Do 128 Times
		(4). -(Branch Back to 20.)
MMU	P	(1). -
	P	(2). -
	P	(3). -(Setup Loop to Load Instruction Page Registers (IPR) and Operand Page Registers (OPR) with Sequential Values of 0 to 255)
	P	(4). -
	P	(5). -
	I/O	(6). Load a Location in the IPR with the value of the Location Address (Internal I/O Command, WIPR, 51XYH)
	I/O	(7). Load a Location in the OPR Increment Loaded Value with the Value of the Location Address (Internal I/O Command, WOPR,52XYH)
	P	(8). -(Increment IPR Address)
	P	(9). -(Increment OPR Address; Repeat Loop [4. - 9.] 256 Times)
	B2	(10). -(Setup Temporary Register to Indicate MMU Present; Branch back to 23)

Notes:
1. This operation is performed whether or not an MMU is present.
2. "-" indicates internal CPU operation.
3. Sequence numbers in "()" are performed only under the stated conditions.
4. Each step enumerated above represents a single machine (SYNC) cycle of the type shown in the "Cycle" column.
   "P" indicates a 5 OSC cycle, 60% duty cycle, machine cycle.
   "I/O" and "M" indicate a 5 OSC cycle, 50% duty cycle, machine cycle
   "B1" indicates a 6 OSC cycle, 50% duty cycle, machine cycle.
   "B2" indicates a 6 OSC cycle, 66% duty cycle, machine cycle.

Table 3. MAS281 Initialisation Sequence

3.2.1 Internal CPU Cycles

Internal CPU cycles are used to perform all CPU data manipulation and housekeeping operations. Internal CPU cycles are either five or six oscillator periods in duration and are characterised by AS low and DSN, DDN and M/ION high. Section 6.0 provides timing characteristics for internal CPU cycles. Tables 7a and 7b in Section 4.0 provide machine cycle counts (both the five and the six OSC cycle variety) associated with each MIL-STD-1750A instruction.

3.2.2 Instruction Fetches

Instruction Fetches are used to keep the instruction pipeline full. This ensures that the next instruction is always ready for execution when the preceding instruction is completed. During jump and branch instruction execution, the pipeline is flushed, and then it is refilled via two consecutive instruction fetches starting at the new instruction location. The pipeline is also refilled as part of interrupt and hold request processing.

Instruction fetches are characterised by IN/OPN high but are otherwise identical to an operand read transfer. For a detailed explanation of the function of various bus control signals during instruction fetches, refer to the discussion of operand transfers below. Section 6.0 provides timing characteristics for instruction fetches. Machine cycles associated with instruction fetches are a minimum of five oscillator periods in duration. The RDYN signal may be used to insert wait states to accommodate slow memory. Machine cycle counts included in Table 7a of Section 4.0 include instruction fetches.

Instruction fetches use instruction pipeline registers IA and IB, the instruction counter (IC), and the data input register (DI) and proceed as follows: assuming an empty instruction pipeline (occurring as a result of a reset, jump, or branch), the contents of IC are placed on the AD bus as an address. The returned value, which will be an instruction, is stored in the IA register.

The value in IC is incremented (via its dedicated counter) and the next fetch is performed. This second returned value, which may be either an instruction or an immediate operand, is stored in both the IA and DI registers. The instruction previously stored in IA is advanced to IB to be executed.

The instruction in IB is checked to determine if an immediate operand is required. If so, that operand has already been pre-fetched and resides in both IA and DI. If not, then the value currently in IA is an instruction. If IA contains an operand, another instruction fetch is performed and the returned value is stored only in IA (the contents of IB and DI are preserved). If IA contains an instruction, however, the next fetch is deferred until the contents of IB are no longer needed. At that time, the deferred fetch is performed, IA is advanced to IB for execution, and the newly returned value is stored in both IA and DI.

This sequence repeats until the instruction pipeline is again emptied at which time the whole process is repeated.

3.2.3 Operand Transfers

Operand transfers are used to obtain (read in) operands to be used by an instruction and to save (write out) any results of an instruction's execution. Section 6.0 provides timing characteristics for operand transfers. Machine cycles associated with operand transfers are a minimum of five oscillator periods in duration. The RDYN signal may be used to insert wait states to accommodate slow memory. Machine cycle counts in Table 7a of Section 4.0 include operand transfers.

Operand transfers use the address register (A), the data input register (DI), and data output register (DO). Before the operand transfer begins, the processor calculates the effective operand address and stores this value in A. For write transfers, the processor loads the operand into the DO register.

All operand transfers between the module and memory are referenced to the AS and DSN bus control signals and are characterised by IN/OPN low and, by M/ION and CDN high. The transfer begins by placing the contents of A (the address register) on the AD bus immediately following the SYNCN high-to-low transition. The AS strobe then goes high to enable the system's transparent address latch. The address is assured valid on the high-to-low transition of AS. The DDN signal is high during the address portion of the transfer; its subsequent action depends on whether the

transfer is a read or write.The RD/WN signal indicates the direction of the transfer. If the operand is a write, the address from A is replaced by the operand in DO when SYNCN transitions from low-to-high. Next, the DSN signal goes low and can be used by the memory system to generate a write enable. Data is guaranteed valid at the low-to-high transition of DSN. DDN stays high for the duration of a write transfer. The memory system must pull RDYN low to conclude the transfer.

If the operand transfer is a read, the AD bus drivers are placed in a high impedance state at the low-to-high transition of SYNCN to give the memory system access to the bus. Next, the DSN signal goes low and can be used by the memory system to generate an output enable. Shortly after DSN goes low, DDN also goes low. This should be used by the system to reverse the direction of the system's AD bus transceivers. The memory system must pull RDYN low to conclude the transfer. Data will be read into the DI register on the SYNCN high-to-low transition.

3.2.4 Input/Output Transfers

Input/Output transfers utilize the MIL-STD-1750A XIO and VIO protocols and are characterized by M/ION and IN/OPN low and CDN high. RD/WN defines the direction of the transfer. AS and DSN cycle as with operand transfer operations. The procedure followed depends on whether the transfer is associated with one of the internally implemented XIO commands or an externally implemented capability. An exception is the Read Configuration Word (RCW) command which is decoded by the MAS281 but is treated, in some ways, like an externally implemented XIO command. This exception is discussed below.

Internal I/O transfers involve all XIO commands which are decoded internally either by the MAS281 or by the MA17504 MMU/BPU chip (with the exception noted above). Table 7b identifies these commands. The A, DI and DO registers are used as in operand transfers. Internal I/O transfers are characterised by DDN staying high for the duration of the transfer in order to prevent bus contention between the module AD bus and the

BIT	Test Coverage	BIT Fail Codes (FT $_{13,14,15}$)	Cycles
1	Microcode Sequencer IB Register Control Barrel Shifter Byte Operations and Flags	100	220
2	Temporary Registers (T0 - T7) Microcode Flags Multiply Divide	101	165
3	Interrupt Unit - MK, PI, FT Enable/Disable Interrupts	111	216
4	Status Word Control User Flags General Registers (R0 - R15)	110	155
5	Timer A Timer B	111	775
-	BIT Pass/Fail Overhead	-	25

Note: BIT pass is indicated by all zeros in FT bits 13, 14, and 15.

Table 4. Built-in Test Coverage and Timing

system bus. Machine cycle associated with internal I/O commands are normally six oscillator cycles in duration but might be extended to seven OSC cycles by the internal ready interface if the module is run at high frequencies. Internal I/O transfers may be subdivided into writes, reads and commands as follows:

I/O writes consist of a command phase followed by the value to be written. The command is placed on the AD bus from the A register at the SYNCN high-to-low transition and is assured valid on the high-to-low transition of AS. The value to be written is placed on the AD bus from the DO register at the SYNCN low-to-high transition and is written to the internal I/O device by the subsequent SYNCN high-to-low transition. An example of an internal I/O write is loading timer A.

I/O reads consist of a command phase followed by the value returned by the internal device. The command is placed on the AD bus from the A register at the SYNCN high-to-low transition and is assured valid on the high-to-low transition of AS. The internal I/O device places the value to be read on the AD bus at the SYNCN low-to-high transition. This value is captured by the DI register on the subsequent SYNCN high-to-low transition. An example of such an operation is reading the interrupt mask register.

I/O commands consist of a command phase alone. The command is placed on the AD bus from the A register at the SYNCN high-to-low transition and is executed at the following SYNCN high-to-low transition. An example of an I/O command is raising the DMAE discrete.

External I/O transfers are similar to internal I/O transfers with the following exceptions: (1) DDN goes low, as with operand transfers, during an I/O read; and (2) external I/O machine cycles are normally five OSC cycles in duration and may be extended via the RDYN signal as with operand transfers.

As discussed earlier, the Read Configuration Word command is a special case. It is decoded internally to generate a read strobe (CONFWN) and therefore uses both the standard internal I/O six OSC period machine cycle as well as the internal ready interface to extend its cycle. It relies on an externally implemented configuration register, however, and therefore cycles DDN as with external I/O cycles. Therefore, the configuration word register must reside on the system side of the data bus transceivers as opposed to residing directly on the local AD bus (as shown in Figure 5).

3.3 Interrupt Servicing

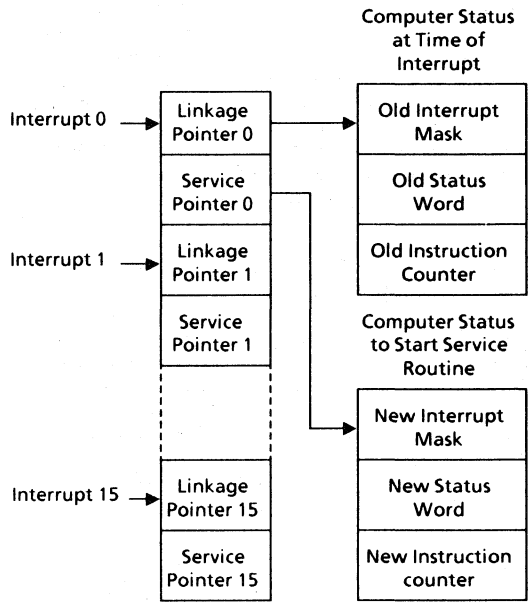


Figure 6. Interrupt Vectoring

Nine user interrupt request inputs are provided for programmed response to asynchronous system events. A low on any of these inputs will be detected at the high-to-low transition of SYNCN and latched into the Pending Interrupt (PI) register on the following SYNC high-to-low transition (with the exception of INT02N which is latched into PI when INT02N is first detected). This sequence occurs whether interrupts are enabled or disabled or whether the specific interrupt is masked or unmasked.

Each external PI register input is buffered by a falling edge detector to prevent repeat latching of requests held low beyond the first SYNCN high-to-low transition. An interrupt request input must transition to the high state before a subsequent request on that input will be detected.

When an interrupt request is latched into PI, it is ANDed with its corresponding mask bit in the mask register (MK). Interrupt level 0 is not maskable. Any unmasked pending interrupts are output to the priority encoder where the highest priority is encoded as a 4-bit vector. If interrupts are enabled, and an unmasked interrupt is pending, the priority encoder will assert an interrupt request to the CU.

Upon completing execution of a given MIL-STD-1750A instruction, the CU's microsequencer checks the state of the priority encoder's interrupt request. If an interrupt request is asserted, the microsequencer branches to the microcode interrupt service routine. This routine performs a read of the priority encoder's 4-bit pending interrupt vector, stores the value in the EU DI register, and then uses this value to calculate the appropriate interrupt linkage and service pointers. The pointers serve as addresses to data structures used in servicing interrupts. Figure 6 depicts this relationship. Table 5 defines pointer values.

Using the linkage and service pointers, the microcode interrupt service routine performs the following: (1) the current contents of the status word, mask register, and instruction counter are saved; (2) a write status word I/O command is executed with an all zero data word; (3) the new mask is loaded into MK and interrupts are disabled; (4) the new status word is read and checked for a valid AS field - If AS is non-zero and an MMU is not present, AS is set to zero and fault 11 (address state error) is set in the fault register FT; (5) a write status word command using the new status word is performed; and (6) the new IC value is loaded into IC, the instruction pipeline is filled starting at the new address, and instruction execution begins.

[NOTE: The steps listed above represent a summary of actions performed during interrupt servicing and do not necessarily reflect the actual order in which these events take place.]

If an interrupt is latched during the interrupt service routine, it will not be processed until interrupts are re-enabled. If an AS fault occurs during the service routine, interrupt level 1 will be set. This interrupt will be serviced when interrupts are re-enabled unless it is masked by the new value in MK.

3.4 Fault Servicing

Eight user fault inputs are provided. A low on any of these inputs will be latched into the Fault Register (FT) at the high-to-low transition of SYNCN.

	Interrupt	LP Address	SP Address
PWRD	0	20	21
	1	22	23
INT02	2	24	25
	3	26	27
	4	28	29
	5	2A	2B
	6	2C	2D
	7	2E	2F
INT08	8	30	31
	9	32	33
INT10	10	34	35
INT11	11	36	37
IOI1	12	38	39
INT13	13	3A	3B
IO12	14	3C	3D
INT15	15	3E	3F

Table 5. Interrupt Pointer Definitions

No falling edge detectors are provided to prevent repeat latching of faults held low beyond the first SYNCN high-to-low transition. However, all FT bits are ORed together and input to the PI bit 1 through an edge detector to prevent the fault register from causing multiple level 1 interrupts.

The sequence of events following a fault capture depends on the type of fault as follows:

3.4.1 MPEN, PIOPEN, DMAPEN, PIOXEN, FLT7N, and SYSFN

The capture of one or more of these faults immediately sets pending interrupt level 1 (machine error) of the Pending Interrupt (PI) register. Anti-repeat logic between the FT and PI prevents latching more than a single interrupt into the PI before the user interrupt service routine has cleared the FT. The microcoded interrupt service routine reads the interrupt priority vector from the Interrupt Unit and clears the serviced interrupt from the PI. At this point the PI is ready to latch another interrupt into this bit.

When this microcoded service routine acts on a level 1 interrupt, it clears the PI bit 1, but the FT maintains the interrupting bit(s). Therefore, a level 1 interrupt would be latched again if there was no anti-repeat logic to prevent a never-ending loop of interrupts.

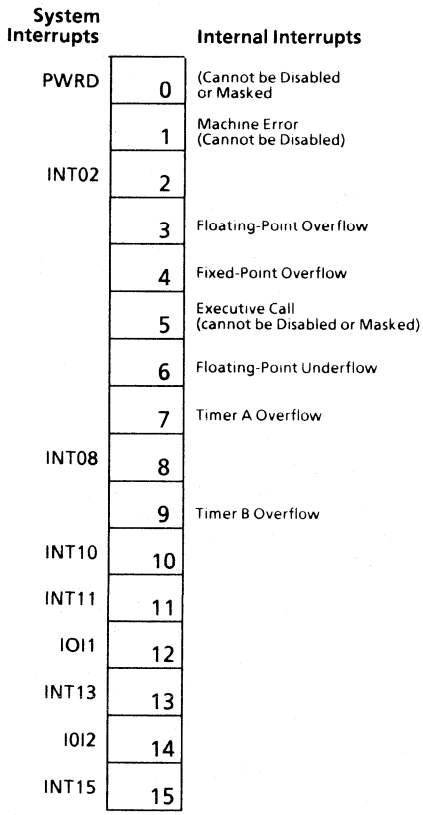


Figure 7. Pending Interrupt Register Bit Assignments

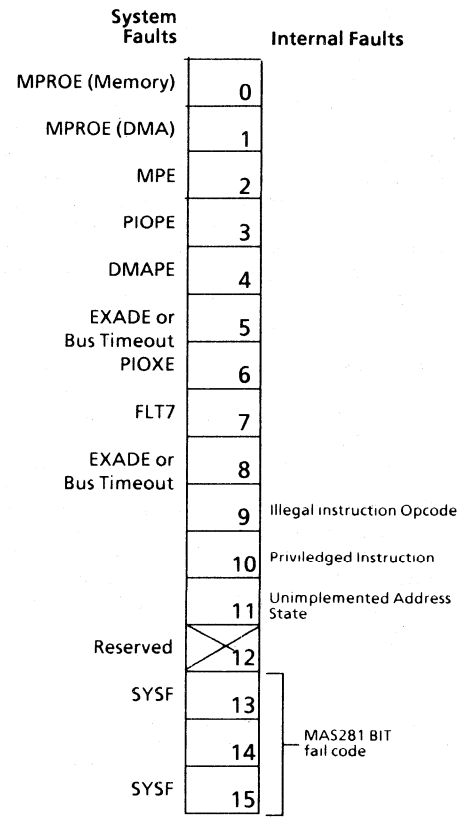


Figure 8. Fault Register Bit Assignments

During the SYNCN cycles between fault capture and the beginning of the microcode interrupt handling routine, AS and DSN are forced to their inactive states. In the case of MPROEN, which may reflect an attempted write violation, it is required that system hardware provide the additional protection necessary to inhibit memory write strobe.

Interrupts are serviced at the end of the currently executing instruction if not masked and if interrupts are enabled. System software servicing level 1 interrupts must clear the FT via the RCFR internal I/O command at some point in the routine to allow subsequent faults to latch a level 1 interrupt request. A non-destructive read of the FT is provided by the internal I/O command RFR, but this command should be used carefully.

3.4.2 MPROEN, EXADEN, and Bus Fault Time-Out

The capture of one or more of these faults immediately sets pending interrupt level 1 (machine error) of the Pending Interrupt (PI) register. Furthermore, the instruction currently executing is aborted at the SYNCN high-to-low transition following the SYNCN high-to-low transition that latched the fault. The IC value saved in the interrupt linkage table for the level 1 interrupt always points to the instruction which was in instruction pipeline register IA at the time of the abort. Anti-repeat logic between the FT and PI prevents latching more than a single interrupt into the PI before the user interrupt service routine has cleared the FT.

The microcoded interrupt service routine reads the interrupt priority vector from the Interrupt Unit and clears the serviced interrupt from the PI. At this point the PI is ready to latch another interrupt into this bit. When this microcoded service routine acts on a level 1 interrupt, it clears the PI bit 1, but the FT maintains the interrupting fault bit(s). Therefore, a level 1 interrupt would be latched again if there were no anti-repeat logic to prevent a never-ending loop of interrupts from occurring.

3.5 DMA Support

DMA data transfers are performed under the control of a system DMA controller over the system AD bus. The user signals that DMA requests will be honored by setting the DMAE output high via the DMAE internal XIO command. The DMA controller may request use of the AD bus by pulling the module's DMARN input low.

Unless the DMAE output is high, all such requests will be ignored. If DMAE is high, DMARN will be acknowledged by DMAKN dropping low. This occurs at the first SYNCN high-to-low transition after DMARN goes low.

DMAKN low indicates that the module has relinquished control of the AD bus by placing its AD bus, AS, DSN, M/ION, RD/WN and IN/OPN drivers in their high impedance state. DDN is dropped low to direct the system data bus transceivers to drive the local AD bus and CDN is dropped low to disable the control signal buffers. The DMA controller relinquishes control of the AD bus by raising DMARN high. The module responds by raising DMAKN high at the next SYNCN high-to-low transition and continuing with program execution.

3.6 Hold Support

The Hold state is provided to facilitate debugging of user software by allowing the user to disable the MAS281 and access system resources. Hold state timings is defined in Section 6.0. The Hold state can be entered either by pulling HOLDN low or by executing a BPT instruction with the Console present and indicated in the Configuration Word. These two approaches, as well as methods for using the Hold state to single step through software, are discussed below:

3.6.1 Using HOLDN

At the completion of the currently executing instruction, the microsequencer checks the state of the HOLDN input. If low, the microsequencer branches to the microcode Hold service routine. This routine decrements IC twice, enables the Hold termination sequence, drops HLDAKN low, and enters the Hold state. HLDAKN drops low three SYNCN cycles after the final SYNCN cycle of the currently executing instruction. A low on HLDAKN indicates that the module has relinquished the AD bus by placing its AD bus, AS, DSN, M/ION, RD/WN and IN/OPN drivers into the high impedance state and, DDN and CDN drop low.

When HOLDN is returned high, the Hold state will end on the subsequent high-to-low transition of SYNCN. This is signified by raising HLDAKN, at which point the module resumes control of the AD bus, AS, DSN, M/ION, RD/WN and IN/OPN signals. CDN and DDN raise high.The instruction pipeline is then refilled and instruction execution resumes with the first instruction loaded into the pipeline.

3.6.2 Using BPT

The Hold state may also be entered by executing a BPT instruction with Console present indicated in the Configuration Word. On encountering a BPT instruction, the processor reads the Configuration Word to check for the presence of a Console. If a Console is indicated, the microsequencer branches to the microcode BPT Hold service routine. This routine decrements IC once, drops HLDAKN low, and enters the Hold state.

To release the MAS281 from a BPT initiated Hold state, the HOLDN input must be pulsed low in accordance with the timing diagrams in Section 6.0. When HOLDN returns high, the Hold state will be released on the following SYNCN high-to-low transition. The instruction pipeline is then refilled and instruction execution resumes with the first instruction loaded into the pipeline.

3.6.3 Single-Stepping

Software can be single-stepped through the proper use of the HOLDN input and the BPT instruction. Use the BPT instruction to mark the beginning of the section of code which will be stepped through. Pulse HOLDN low to release the BPT initiated Hold state and then pull HOLDN low again during the two subsequent SYNCN cycles that refill the instruction pipeline. When the first instruction following Hold release completes execution, the module will once again enter the Hold state. Again pulling HOLDN will cause the next instruction to execute. This process may be repeated as long as required. Raising HOLDN high will resume normal operation.

3.7 Timer Operations

The MAS281 implements interval timers A and B, a trigger-go counter, and a bus fault timer. A discussion of each follows:

3.7.1 Timers A and B

Timer A is clocked by the TCLK input; timer B is clocked by an internally generated TCLK/10. MIL-STD-1750A requires TCLK to be a 100-kHz pulse train. If allowed to overflow, timers A and B will set level 7 and level 9 interrupt requests, respectively. Timing characteristics of each timer are defined in Section 5.0. Either timer can be read, loaded, started, and stopped through the use of internally decoded XIO commands.

These commands are identified in Table 7b in Section 4.0. By asserting the DTIMERN input, both timers will halt and all internally decoded XIO commands which would change their state are disabled (asserting DTIMERN also disables DMA accesses by driving DMAE low and DMAKN high). Raising DTIMERN allows the timers to resume counting from their suspended state and allows timer commands to function normally (DMA control lines are again allowed to change).

A feature of the MAS281 timers is the choice of disabling, or not disabling, the interval timers A and B upon execution of a BPT software instruction when a Console is connected. If full compliance with MIL-STD-1750A (Notice 1) is desired, the halting of timers A and B can be accomplished by pulling DTIMERN low upon execution of a BPT instruction with a Console connected. Two suggested ways to do this are: (1) connect HLDAKN to DTIMERN through an AND gate; or (2) allow the system Console to pull DTIMERN low upon receiving HLDAKN low. The first option provides a faster response and is a less complicated method, whereas the second choice allows the option of halting timers A and B, or not halting them.

[NOTE: As described in Section 2.2, DTIMERN low suspends the trigger-go timer and disables DMA access (forces DMAE low and DMAKN high) in addition to halting timers A and B].

3.7.2 Trigger-Go Counter

The trigger-go counter is clocked by the TGCLK input. Timing characteristics for trigger-go counter operation are defined in Section 6.0. DTIMERN disables and enables operation in the same manner as with timers A and B. Whenever the trigger-go counter overflows, TGON drops low and remains low until the counter is reset via the GO internal XIO command.

3.7.3 Bus Fault Timer

All bus operations are monitored to ensure timely completion. A hardware timeout circuit is enabled at the start of each memory and I/O transfer (DSN high-to-low transition) and is reset upon receipt of the external ready (RDYN) signal.

If this circuit fails to reset within a minimum of one TCLK period or a maximum of two TCLK periods, either bit 8 (if the transaction is with memory) or bit 5 (if the transaction is with I/O) of the Fault Register (FT) is set. This sets pending interrupt level 1 and causes the current bus cycle to be terminated by forcing SYNCN low. The MIL-STD-1750A instruction is aborted, and control passes to the level 1 interrupt service routine (if the level 1 interrupt is unmasked). This feature is disabled by pulling DTON low.

4.0 Software Considerations

The MAS281 implements the full MIL-STD-1750A instruction set. Table 7a lists the instruction set and provides performance data for each instruction. Table 7b provides a summary of the XIO commands which are internally decoded on the module. Resources available to the software programmer are depicted in Figure 9. A discussion of data types, addressing modes and benchmarking considerations follows.

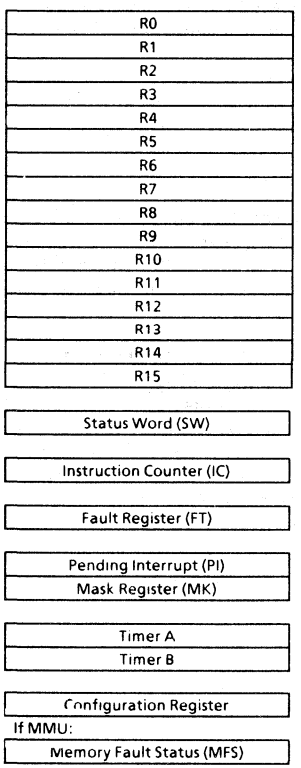


Figure 9. Register Set Model

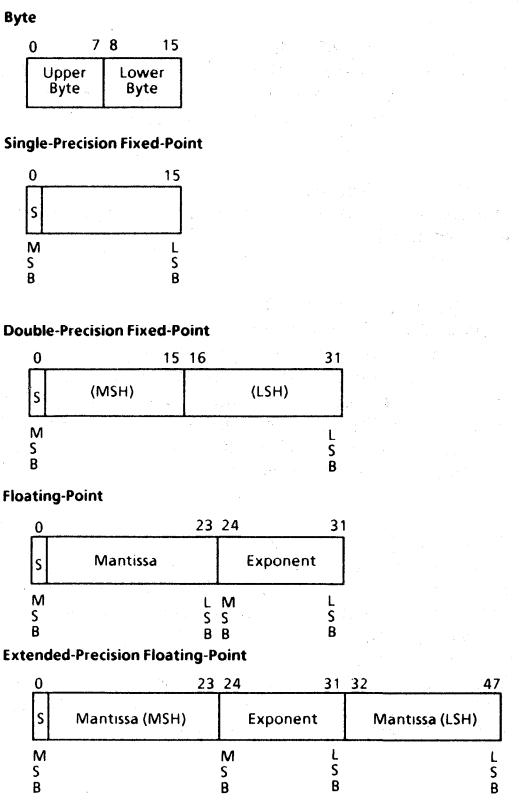


Figure 10. Data Formats

4.1 Data Types

The MAS281 fully supports 16-bit fixed-point single-precision, 32-bit fixed-point double-precision, 32-bit floating-point, and 48-bit extended precision floating-point data types. Figure 10 depicts the formats of these data types.

All numerical data is represented in two's complement form. Floating-point numbers are represented by a fractional two's complement mantissa with an 8-bit two's complement exponent. All floating-point operands are expected to be normalized. If not normalized, the results from an instruction are not defined.

4.2 Addressing Modes

The MAS281 supports the eight addressing modes specified in MIL-STD-1750A. These addressing modes are depicted in Figure 11 and are defined below.

4.2.1 Register Direct (R)

The register specified by the instruction contains the required operand.

4.2.2 Memory direct (D,DX)

Memory Direct (without indexing) is an addressing mode in which the instruction contains the memory address of the required operand. In Memory Direct-Indexed (DX), the memory address of the required operand is specified by the sum of the contents of an index register (RX) and the instruction address field (A). Register R1 through R15 may be specified for indexing.

4.2.3 Memory Indirect (I, IX)

Memory Indirect (without indexing) is an addressing mode in which the memory address specified by the instruction contains the address of the required operand. In Memory Indirect with Pre-Indexing (IX), the sum of the contents of a specified index register and the instruction address field in the address that contains the address of the required operand. Registers R1 through R15 may be specified for pre-indexing.

4.2.4 Immediate Long (IM, IMX)

There are two formats which implement Immediate Long Addressing; one allows indexing and one does not. For the indexable form, if the specified index register, RX, is not equal to zero, the contents of RX are added to the immediate field to form the required operand; otherwise, the immediate field contains the required operand.

4.2.5 Immediate Short (IS)

In this mode the required 4-bit operand is contained within the 16-bit instruction. The Immediate Short addressing mode accommodates two formats; one which interprets the contents of the immediate field as positive data and the other which interprets the contents of the immediate field as a negative data.

4.2.5.1 Immediate Short Positive (ISP)

The immediate operand is treated as a positive integer between 1 and 16.

4.2.5.2 Immediate Short Negative (ISN)

The immediate operand is treated as a negative integer between -1 and -16. Its internal form is a two's complement, sign-extended 16-bit number.

4.2.6 Instruction Counter Relative (ICR)

This addressing mode is used for 16-bit branch instructions. The contents of the instruction counter minus two (the address of the current instruction) is added to the sign-extended 8-bit displacement field within the instruction. This sum then points to the memory address to which control will be transferred if the branch is taken.

4.2.7 Base Relative (B)
There are two formats which implement Base Relative Addressing; one allows indexing and one does not. For the non-indexable form, the contents of the instruction specified base register (BR = BR' + 12) is added to the 8-bit displacement field (DU) of the 16-bit instruction. For the indexable form, the sum of the contents of a specified index register and a specified base register is the address of the required operand. Registers R1 through R15 may be specified for indexing. Registers R12 through R15 may be specified as the base register.

4.2.8 Special
This addressing mode is applicable to instructions that do not follow the above formats. The instructions that use this special mode are indicated in Table 7a.

4.3 Benchmarking

Table 7a defines the number and type of machine cycles associated with each MIL-STD-1750A instruction. This information may be used when benchmarking MAS281 performance. The Digital Avionics Instruction Set (DAIS) mix, which defines a typical frequency of occurrence for MIL-STD-1750A instructions, is used here for this purpose.

One problem with the DAIS mix, however, is that it does not reflect the impact of data dependencies on system performance. For example, a multiplication in which operand is zero may be performed much faster than one with two non-zero operands. Also, the DAIS mix does not specify such time consuming operations as normalization and alignment.

Realistic benchmarks must therefore take both the instruction mix and data dependencies into account. To this end, machine cycle counts in Table 7a which have data dependencies, are annotated with either an "a" or "wa" suffix.

An "a" suffix reflects an average number of machine cycles (where each of several possibilities is equally likely) and a "wa" suffix reflects a weighted average number of machine cycles (where some data possibilities are more likely than others).

Weighted averages are only applicable to floating-point operations. Weighted averages provided in Table 7a are based on the Sweeney (IBM) guidelines. These guidelines take a wide range of data dependencies into consideration. Normalization and alignment operations are also represented. Table 6 defines MAS281 throughput, at various frequencies and wait states, for the DAIS mix using Sweeney data dependencies.

It should be noted that using the Sweeney guidelines is a conservative approach to benchmarking. If best case assumptions are made and such operations as normalization and alignment are not considered, MAS281 performance figures are approximately 50% higher than those indicated in Table 6.

f_{osc} MHz	0	1	2	3
25	743.4	698.3	658.4	622.8
20	594.7	558.7	526.7	498.2
15	446.0	419.0	395.0	373.7
10	297.4	279.3	263.4	249.1

Number of Wait States in Memory Access Cycle

Table 6. Throughput (KIPS)

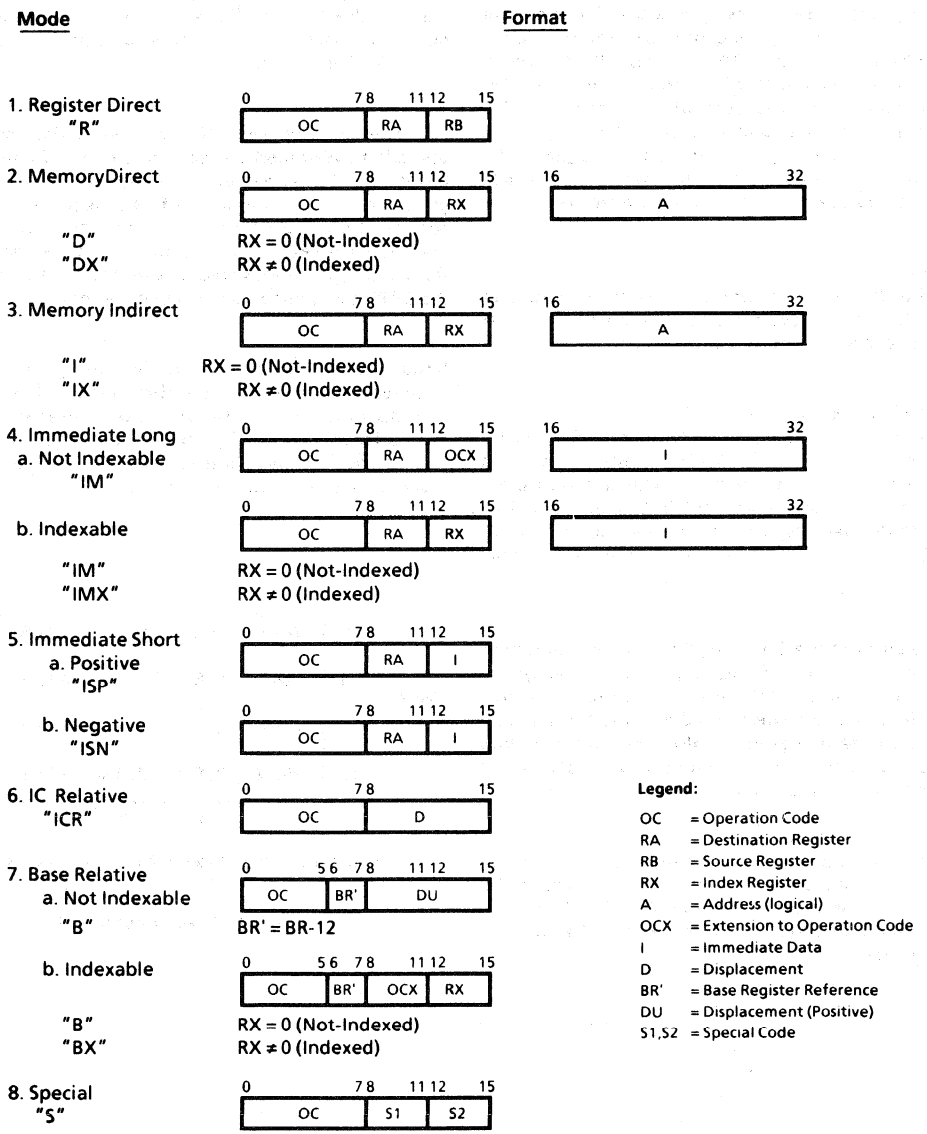


Figure 11. Addressing Modes

4.4 Instruction Summary

Operation	Op Code/Ext	Mnemonic	Format	Cycles *		
				M	P	B
LOAD/STORE						
Single Precision Load	81	LR	R	1	0	0
	0X	LB	B	2	1	0
	4X 0	LBX	BX	2	1	0
	82	LISP	ISP	1	0	0
	83	LISN	ISN	1	0	0
	80	L	D,DX	3	0	0
	85	LIM	IM,IMX	2	0	0
	84	LI	I,IX	4	1	0
Double-Precision Load	87	DLR	R	1	2	0
	0X	DLB	B	3	1	0
	4X 1	DLBX	BX	3	2	0
	86	DL	D,DX	4	0	0
	88	DLI	I,IX	5	1	0
Single-Precision Store	0X	STB	B	2	2	0
	4X 2	STBX	BX	2	2	0
	90	ST	D,DX	3	1	0
	94	STI	I,IX	4	1	0
Store a Non-Negative Constant	91	STC	D,DX	3	1	0
	92	STCI	I,IX	4	1	0
Double-Precision Store	0X	DSTB	B	3	2	0
	4X 3	DSTX	BX	3	2	0
	96	DST	D,DX	4	0	0
	98	DSTI	I,IX	5	1	0
Load Multiple Registers	89	LM	D,DX	3 + n	1	1
Store Multiple Registers	99	STM	D,DX	3 + n	1	1
INTEGER ARITHMETIC						
Single-Precision Integer Add	A1	AR	R	1	1	0
	1X	AB	B	2	2	0
	4X 4	ABX	BX	2	2	0
	A2	AISP	ISP	1	1	0
	A0	A	D,DX	3	1	0
	4A 1	AIM	IM	2	1	0
Increment Memory by a Positive Integer	A3	INCM	D,DX	4	1	0
Single-Precision Absolute Value of Register	A4	ABS	R	1	1.5	1a
Double-Precision Absolute Value of Register	A5	DABS	R	1	2.5	1a

*M = memory, P = processor (5 OSC cycles), B = processor (b OSC cycles),

a = average if more than one alternative exists

Table 7a. Instruction Summary

Operation	Op Code/Ext	Mnemonic	Format	Cycles *		
				M	P	B
Double-Precision Integer Add	A7 A6	DAR DA	R D,DX	1 4	3 1	0 0
Single Precision Integer Subtract	B1 1X 4X 5 B2 B0 4A 2	SR SBB SBBX SISP S SIM	R B BX ISP D,DX IM	1 2 2 1 3 2	1 2 2 1 1 1	0 0 0 0 0 0
Decrement Memory by a Positive Integer	B3	DECM	D,DX	4	1	0
Single Precision Negate Register	B4	NEG	R	1	1	0
Double-Precision Negate Register	B5	DNEG	R	1	3	0
Double-Precision Integer Subtract	B7 B6	DSR DS	R D,DX	1 4	3 1	0 0
Single Precision Integer Multiply with 16-Bit Product	C1 C2 C3 C0 4A 4	MSR MISP MISN MS MSIM	R ISP ISN D,DX IM	1 1 1 3 2	6.5 7.5 7.5 6.5 6.5	4a 4a 4a 4a 4a
Single Precision Integer Multiply with 32-Bit Product	C5 1X 4X 6 C4 4A 3	MR MB MBX M MIM	R B BX D,DX IM	1 2 2 3 2	5 7 7 5 5	3 3 3 3 3
Double-Precision Integer Multiply	C7 C6	DMR DM	R D,DX	1 4	41 40	4.5a 4.5a
Single Precision Integer Divide with 16-Bit Dividend	D1 D2 D3 D0 4A 6	DVR DISP DISN DV DVIM	R ISP ISN D,DX IM	1 1 1 3 2	20.25 20 20.5 20.25 20.25	5.5a 5.5a 5.5a 5.5a 5.5a
Single Precision Integer Divide with 32-Bit Dividend	D5 1X 4X 7 D4 4A 5	DR DB DBX D DIM	R R BX D,DX IM	1 2 2 3 2	21.75 22.75 22.75 21.75 22.75	6.5a 6.5a 6.5a 6.5a 6.5a
Double-Precision Integer Divide	D7 D6	DDR DD	R D,DX	1 4	79.5 77.5	5.5a 5.5a

*M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles).

a = average if more than one alternative exists

Table 7a (continued). Instruction Summary

Operation	Op Code/Ext	Mnemonic	Format	Cycles *		
				M	P	B
LOGICAL						
Inclusive Logical OR	E1	ORR	R	1	0	0
	3X	ORB	B	2	1	0
	4X F	ORBX	BX	2	1	0
	E0	OR	D,DX	3	0	0
	4A 8	ORIM	IM	2	0	0
Logical AND	E3	ANDR	R	1	0	0
	3X	ANDB	B	2	1	0
	4X E	ANDX	BX	2	1	0
	E2	AND	D,DX	3	0	0
	4A 7	ANDM	IM	2	0	0
Exclusive Logical OR	E5	XORR	R	1	0	0
	E4	XOR	D,DX	3	0	0
	4A 9	XORM	IM	2	0	0
Logical NAND	E7	NR	R	1	1	0
	E6	N	D,DX	3	1	0
	4A B	NIM	IM	2	1	0
Set Bit	51	SBR	R	1	0	0
	50	SB	D,DX	4	1	0
	52	SBI	I,IX	5	2	0
Reset Bit	54	RBR	R	1	1	0
	53	RB	D,DX	4	1	0
	55	RBI	I,IX	5	2	0
Test Bit	57	TBR	R	1	0	0
	56	TB	D,DX	3	0	0
	58	TBI	I,IX	4	1	0
Test and Set Bit	59	TSB	D,DX	4	0	2
Set Variable Bit in Register	5A	SVBR	R	1	0	1
Reset Variable Bit in Register	5C	RVBR	R	1	1	1
Test Variable Bit in Register	5E	TVBR	R	1	0	1
Store Register Through Mask	97	SRM	D,DX	4	3	0
BYTE						
Load From Upper Byte	8B	LUB	D,DX	3	0	0
	8D	LUBI	I,IX	4	1	0
Load From Lower Byte	8C	LLB	D,DX	3	1	0
	8E	LLBI	I,IX	4	2	0
Store Into Upper Byte	9B	STUB	D,DX	4	1	0
	9D	SUBI	I,IX	5	3	0
Store Into Lower Byte	9C	STLB	D,DX	4	1	0
	9E	SLBI	I,IX	5	2	0
Exchange Bytes in Register	EC	XBR	S	1	0	1

*M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles).

Table 7a (continued). Instruction Summary

Operation	Op Code/Ext	Mnemonic	Format	Cycles *		
				M	P	B
COMPARE						
Single-Precision Compare	F1	CR	R	1	0	0
	3X	CB	B	2	1	0
	4X C	CBX	BX	2	1	0
	F2	CISP	ISP	1	0	0
	F3	CISN	ISN	1	0	0
	F0	C	D,DX	3	0	0
	4A A	CIM	IM	2	0	0
Compare Between Limits	F4	CBL	D,DX	4	2.75	1.75a
Double-Precision Compare	F7	DCR	R	1	2	0
	F6	DC	D,DX	4	0	0
JUMP/BRANCH						
Jump on Condition	70	JC	D,DX	2	0.5	1a
	71	JCI	I,IX	3	0.5	1a
Jump to Subroutine	72	JS	D,DX	2	2	0
Subtract One and Jump	73	SOJ	D,DX	2	2.5	1a
Branch Unconditionally	74	BR	ICR	2	2	0
Branch if Equal to (Zero)	75	BEZ	ICR	1.5	1	1a
Branch if Less than (Zero)	76	BLT	ICR	1.5	1	1a
Branch to Executive	77	BEX	S	16	12	3a
Branch if Less than or Equal to (Zero)	78	BLE	ICR	1.5	1	1a
Branch if Greater than (Zero)	79	BGT	ICR	1.5	1	1a
Branch if Not Equal to (Zero)	7A	BNZ	ICR	1.5	1	1a
Branch if Greater than or Equal to (Zero)	7B	BGE	ICR	1.5	1	1a
SHIFT						
Shift Left Logical	60	SLL	R	1	1	0
Shift Right Logical	61	SRL	R	1	1	0
Shift Right Arithmetic	62	SRA	R	1	1	0
Shift Left Cyclic	63	SLC	R	1	1	0
Double Shift Left Logical	65	DSLL	R	1	3	0
Douible Shift Right Logical	66	DSRL	R	1	2	0
Double Shift Right Arithmetic	67	DSRA	R	1	2	0
Double Shift Left Cyclic	68	DSLC	R	1	3	0
Shift Logical, Count in Register	6A	SLR	R	1	1	3
Shift Arithmetic, Count in Register	6B	SAR	R	1	1.5	3.50a
Shift Cyclic, Count in Register	6C	SCR	R	1	1	3.25a
Double Shift Logical, Count in Register	6D	DSLR	R	1	2.25	4a
Double Shift Arithmetic, Count in Register	6E	DSAR	R	1	3.19	4.94a
Double Shift Cyclic, Count in Register	6F	DSCR	R	1	3.5	3a

*M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles),
a = average if more than one alternative exists

Table 7a (Continued). Instruction Summary

Operation	Op Code/Ext	Mnemonic	Format	Cycles *		
				M	P	B
CONVERT						
Convert Floating-Point to 16-Bit Integer	E8	FIX	R	1	4.25	4.5a
Convert 16-Bit Integer to Floating-Point	E9	FLT	R	1	3	2a
Convert Extended-Precision Floating-Point to 32-Bit Integer	EA	EFIX	R	1	12.25	6.25a
Convert 32-Bit Integer to Extended-Precision Floating-Point	EB	EFLT	R	1	7.5	3.5a
STACK						
Stack IC and Jump to Subroutine	7E	SJS	D,DX	4	3	0
Unstack IC and return from Subroutine	7F	URS	S	3	1	1
Pop Multiple registers off the Stack	8F	POPM	S	2.5 + n (n = 0 to 15)	2.25 + n (n = 0 to 15)	4.25a
Push Multiple Registers onto the Stack	9F	PSHM	S	1 + n (n = 0 to 15)	4.5 + n (n = 0 to 15)	2a
I/O (See I/O Command Summary)						
Execute I/O	48	XIO**	IM,IMX	3	3.583	6.277a
Vectored I/O	49	VIO**	D,DX	-	-	-
SPECIAL						
Built-In Function Call	4F	BIF	S			
Move Multiple Words, Memory-to-Memory	93	MOV	S	1 + 4n	1 + 3n	1 + 2na
Exchange Words in Registers	ED	XWR	R	1	2	0
Load Status	7D	LST**	D,DX	8	2	3
	7C	LSTI**	I,IX	9	2	4
No Operation	FF	NOP	S	1	2	2
Break Point	FF	BPT	S	3	4	4

*M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles).
a = average if more than one alternative exists
** Privileged instruction.

Table 7a (Continued). Instruction Summary

Operation	Op Code/Ext	Mnemonic	Format	Cycles *		
				M	P	B
FLOATING-POINT						
Extended-Precision Floating-Point Load	8A	EFL	D,DX	5	0	1
Extended-Precision Floating-Point Store	9A	EFST	D,DX	5	0	1
Floating-Point Absolute Value of Register	AC	FABS	R	1	1.75	3.25a
Floating-Point Negate Register	BC	FNEG	R	1	3.25	3.75a
Floating-Point Compare	F9	FCR	R	1	2.75	2.875wa
	3X	FCB	B	2	2.75	2.875wa
	4X D	FCBX	BX	2	2.75	2.875wa
	F8	FC	D,DX	3	1.75	2.875wa
Extended-Precision Floating-Point Compare	FB	EFCR	R	1	3.25	2.875wa
	FA	EFC	D,DX	4.25a	2.75	2.875wa
Floating-Point Add	A9	FAR	R	1	7.625	8.25wa
	2X	FAB	B	3	6.625	8.25wa
	4X 8	FABX	BX	3	6.625	8.25wa
	A8	FA	D,DX	4	5.625	8.25wa
Extended-Precision Floating-Point Add	AB	EFAR	R	1	21.3125	10.5625wa
	AA	EFA	D,DX	5	19.3125	10.5625wa
Floating-Point Subtract	B9	FSR	R	1	8.625	8.625wa
	2X	FSB	B	3	7.625	8.625wa
	4X 9	FSBX	BX	3	7.625	8.625wa
	B8	FS	D,DX	4	6.625	8.625wa
Extended-Precision Floating-Point Subtract	BB	EFSR	R	1	23.0625	11.8125wa
	BA	EFS	D,DX	5	21.0625	11.8125wa
Floating-Point Multiply	C9	FMR	R	1	12.75a	6.25wa
	2X	FMB	B	3	12.75a	6.25wa
	4X A	FMBX	BX	3	12.75a	6.25wa
	C8	FM	D,DX	4	11.75a	6.25wa
Extended-Precision Floating-point Multiply	CB	EFMR	R	1	59.75	6.25wa
	CA	EFM	D,DX	5	57.75	6.25wa
Floating-Point Divide	D9	FDR	R	1	31.5	32.75wa
	2X	FDB	B	3	30.5	32.75wa
	4X B	FDBX	BX	3	30.5	32.75wa
	D8	FD	D,DX	4	29.5	32.75wa
Extended-Precision Floating-Point Divide	DB	EFDR	R	1	102.625	47.875wa
	DA	EFD	D,DX	5	100.625	47.875wa

*M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles),
a = average if more than one alternative exists
wa = weighted average favouring one or more possible alternatives.

Table 7a (Continued). Instruction Summary

4.5 Internal I/O Command Summary

Operation	Command Code (Hex)	Mnemonic	Cycles *		
			M	P	B
Implemented in MAS281					
Set Fault Register	0401	SFR	2	3	9
Set Interrupt Mask	2000	SMK	2	3	9
Clear Interrupt request	2001	CLIR	2	3	9
Enable Interrupts	2002	ENBL	2	3	9
Disable Interrupts	2003	DSBL	2	3	9
Reset Pending Interrupt	2004	RPI	2	3	9
Set Pending Interrupt Register	2005	SPI	2	3	9
Reset Normal Power Up Discrete	200A	RNS	2	3	9
Write Status Word	200E	WSW	2	3a	8.5a
Enable Start-Up ROM	4004	ESUR	2	3	9
Disable Start-Up ROM	4005	DSUR	2	3	9
Direct Memory Access Enable	4006	DMAE	2	3	9
Direct Memory Access Disable	4007	DMAD	2	3	9
Timer A Start	4008	TAS	2	3	9
Timer A Halt	4009	TAH	2	3	9
Output Timer A	400A	OTA	2	3	9
Reset Trigger-Go	400B	GO	2	3	9
Timer B Start	400C	TBS	2	3	9
Timer B Halt	400D	TBH	2	3	9
Output Timer B	400E	OTB	2	3	9
Read Configuration Word	8400	RCW	2	2	4
Read Fault Register Without Clear	8401	RFR	2	2	4
Read Interrupt Mask	A000	RMK	2	2	4
Read Pending Interrupt Register	A004	RPIR	2	2	4
Read Status Word	A00E	RSW	2	1	4
Read and Clear Fault Register	A00F	RCFR	2	2	4
Input Timer A	C00A	ITA	2	2	4
input Timer B	C00E	ITB	2	2	4
Implemented in BPU					
Memory Protect Enable	4003	MPEN	2	4	8
Load Memory Protect RAM	50XX	LMP	2	4	8
Read Memory Protect RAM	D0XX	RMP	2	3	3
Implemented in MMU					
Write Instruction Page Register	51XY	WIPR	2	4	8
Write Operand Page Register	52XY	WOPR	2	4	8
Read Memory Fault Status	A00D	RMFS	2	3	3
Read Instruction Page Register	D1XY	RIPR	2	3	3
Read Operand Page Register	D2XY	ROPR	2	3	3

*M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles),
a = average if more than one alternative exists

Table 7b. Internal I/O Command Summary

5.0 Timing Diagrams

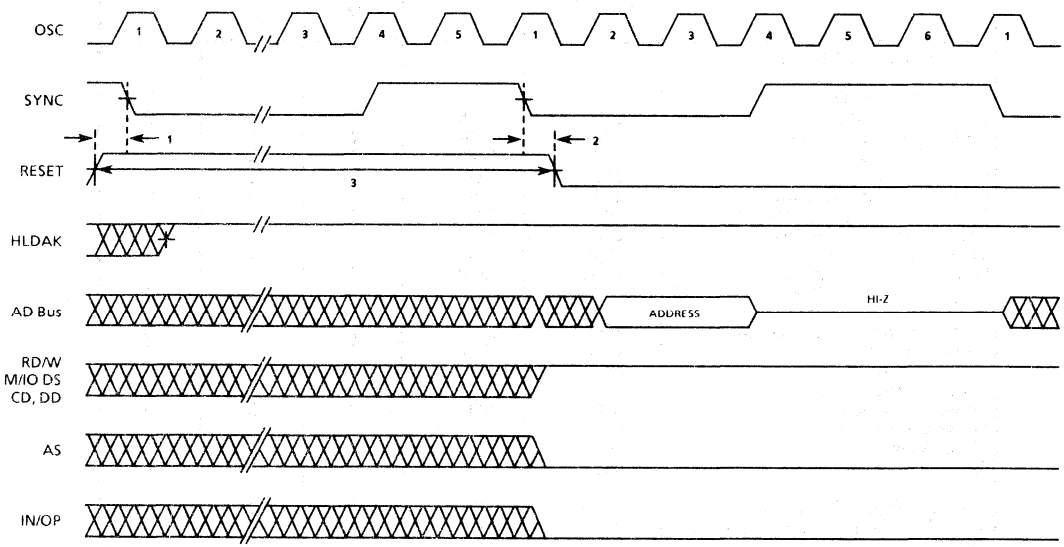


Figure 12. RESET timing

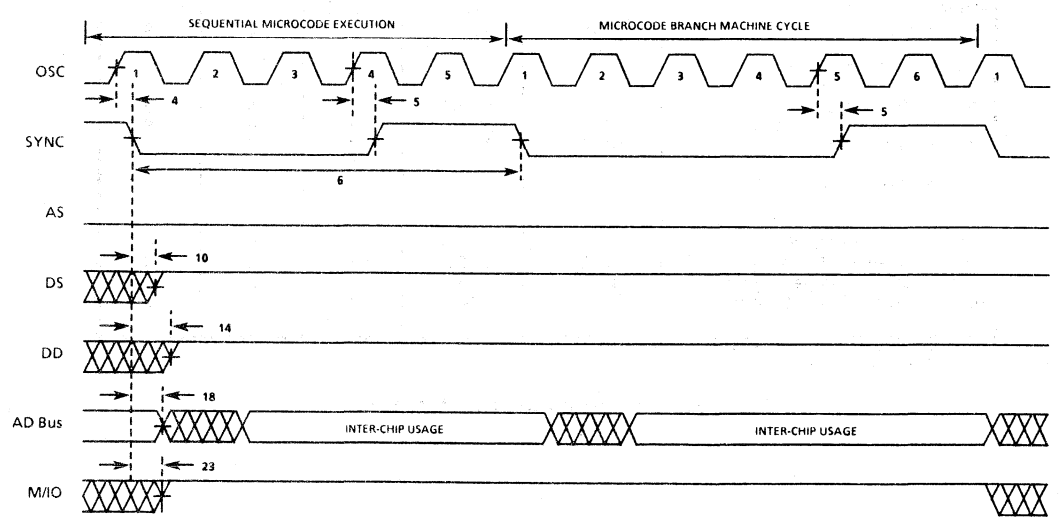
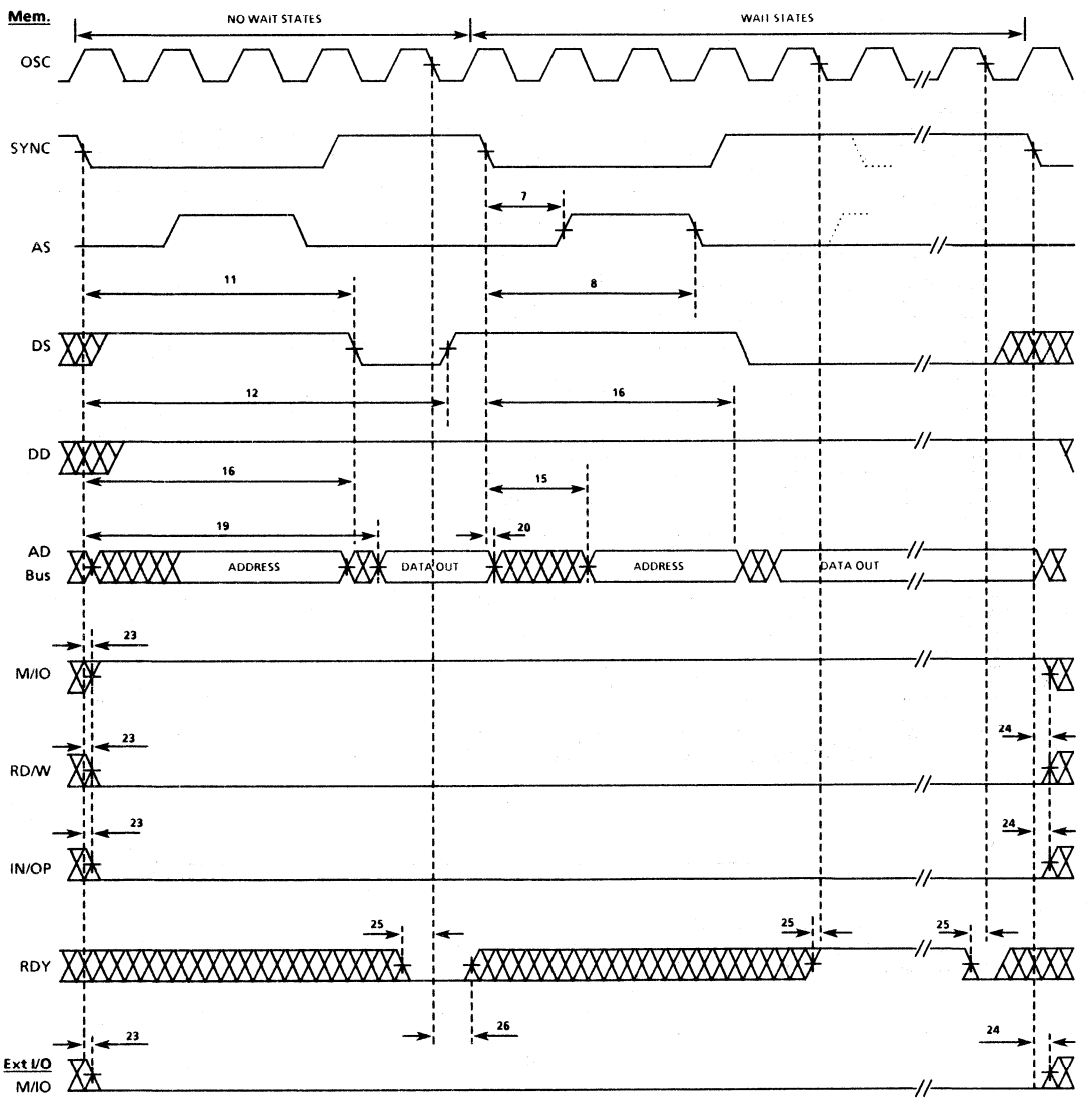
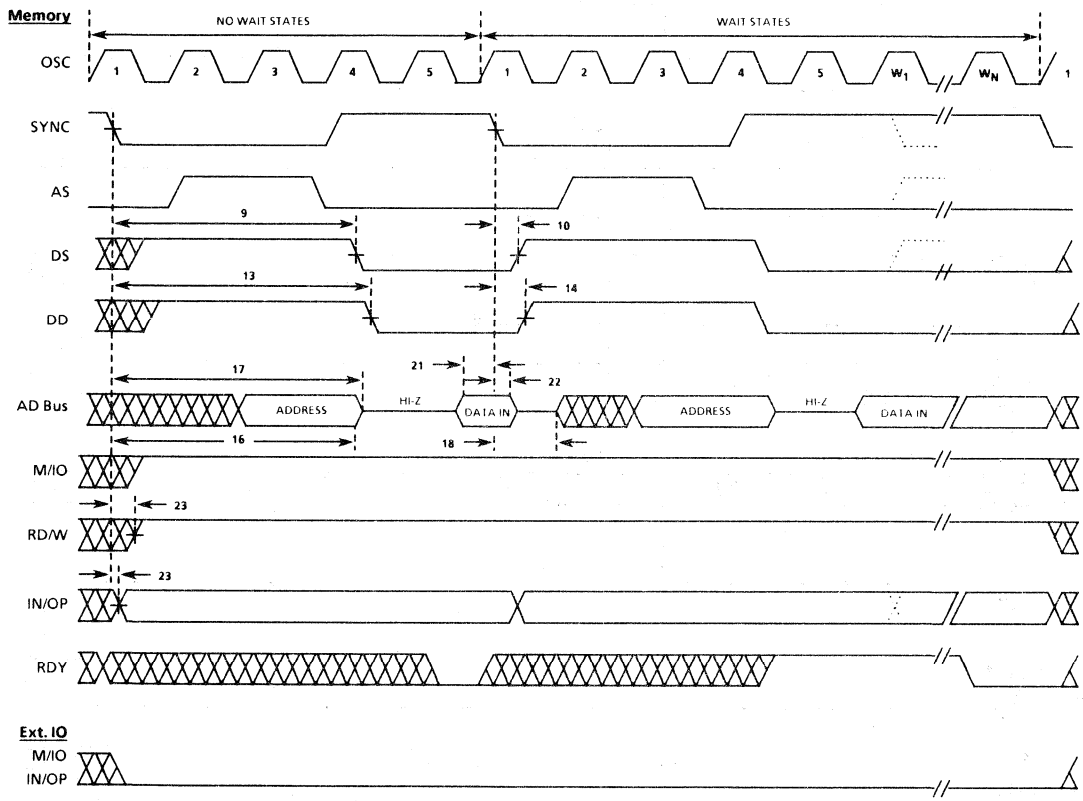


Figure 13. Internal CPU operations



NOTES:
1. Dashed timing lines indicate no-wait cycle timing.
2. Other output states : CD = HIGH, HLDAK = HIGH and DMAK = HIGH
3. Other required input states: HOLD = HIGH, DMAR = HIGH and RESET = LOW

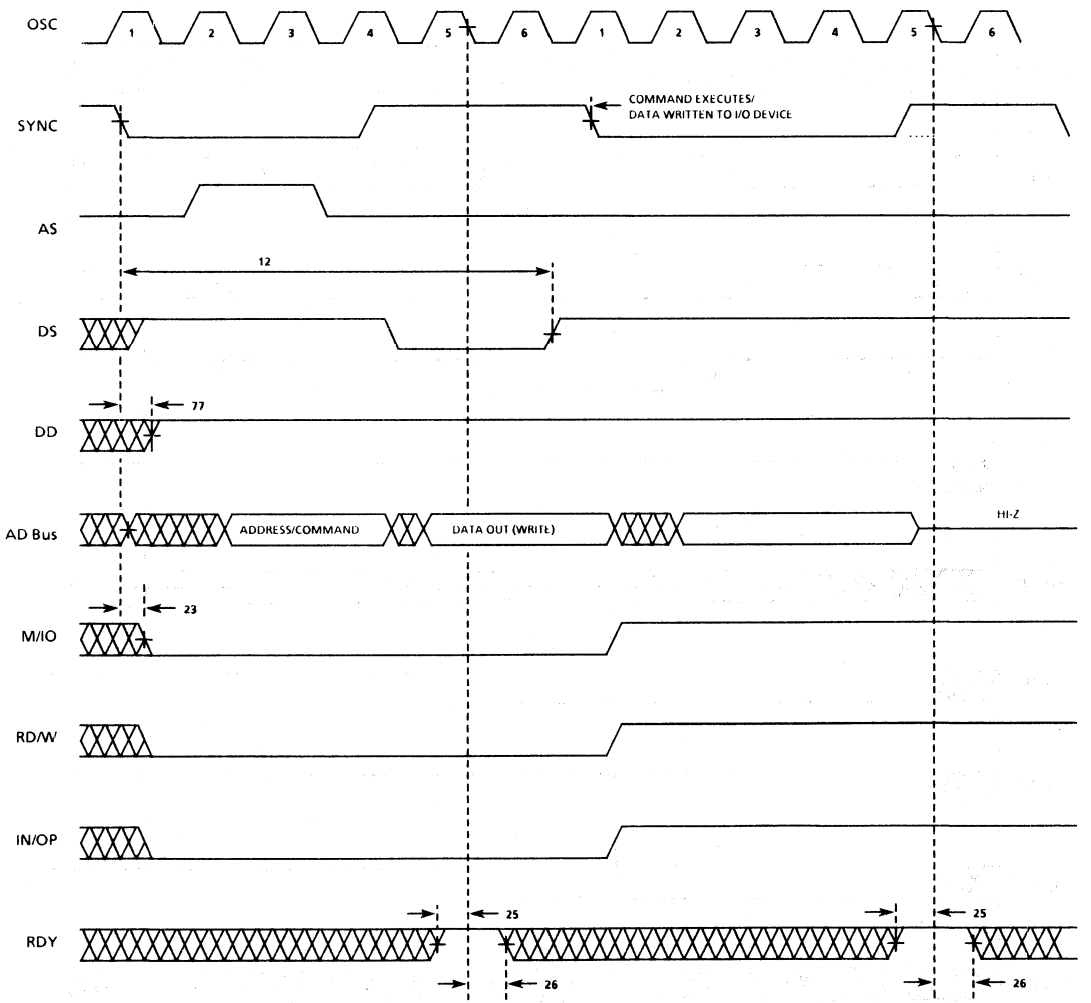
Figure 14. Write transfer timing



NOTES:

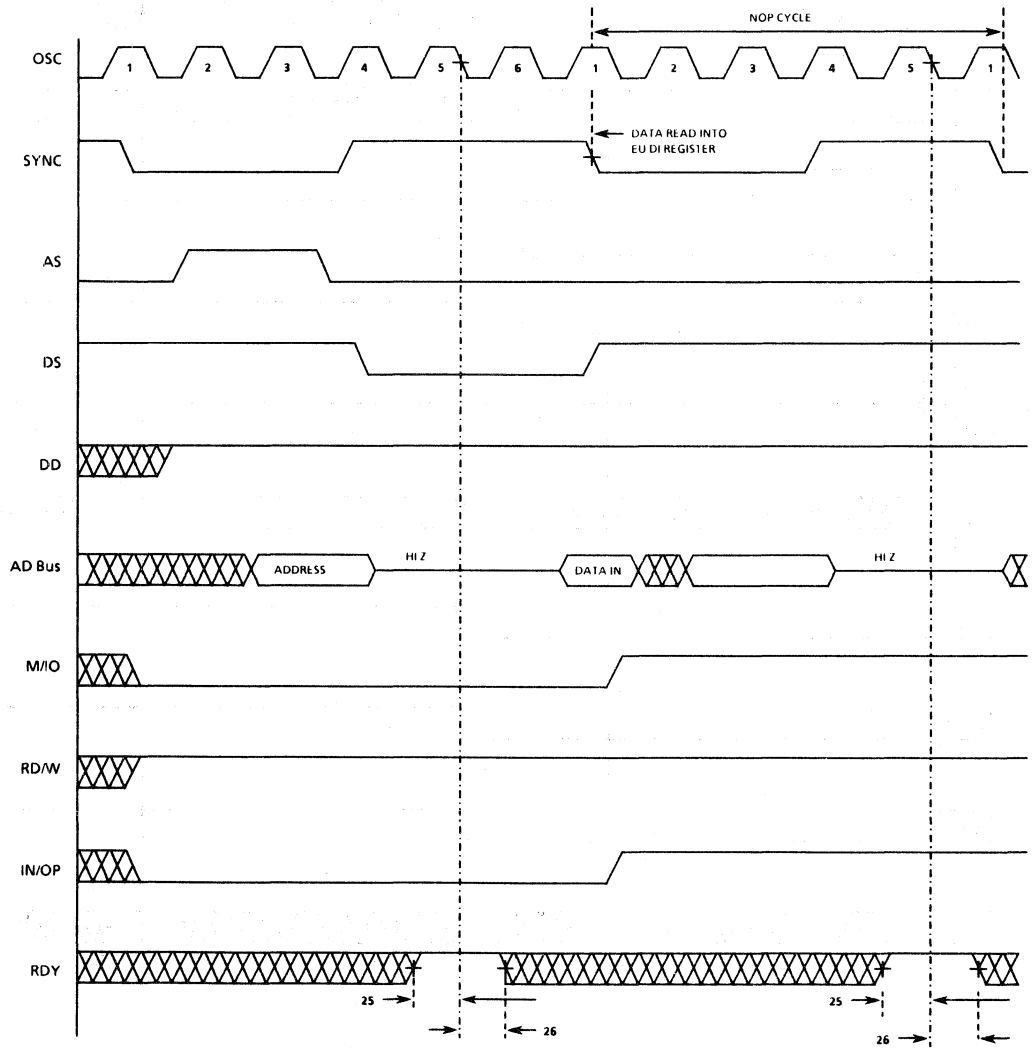
1. Dashed timing lines indicate no-wait cycle timing.
2. Other output states : CD = HIGH, HLDAK = HIGH and DMAK = HIGH
3. Other required input states: HOLD = HIGH, DMAR = HIGH and RESET = LOW

Figure 15. Read transfer timing



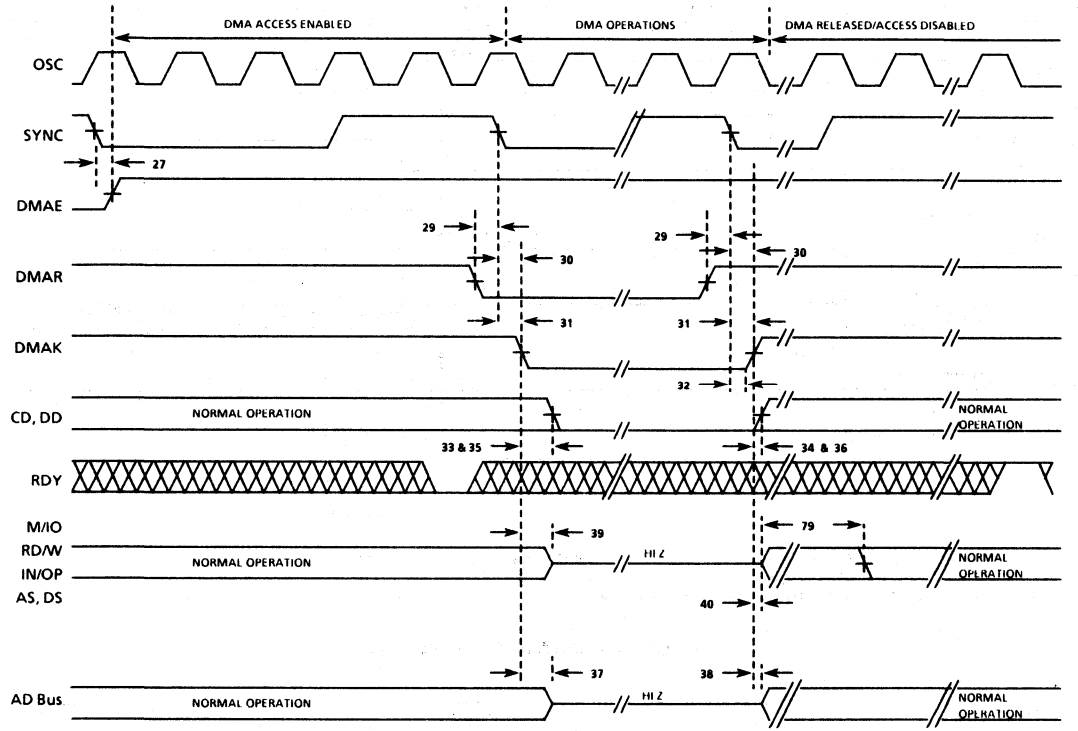
NOTES:
1. Dashed timing lines indicate no-wait cycle timing.
2. Other output states : CD = HIGH, HLDAK = HIGH and DMAK HIGH
3. Other required input states: HOLD = HIGH, DMAR = HIGH and RESET = LOW

Figure 16. Internal I/O write/command



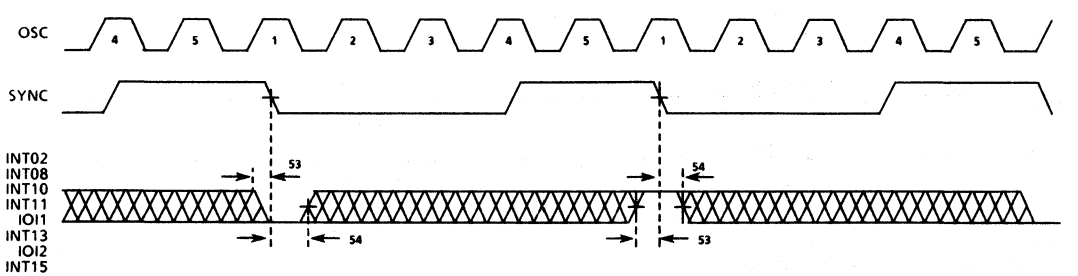
NOTES:
1. Dashed timing lines indicate no-wait cycle timing.
2. Other output states : CD = HIGH, HLDAK = HIGH and DMAK HIGH
3. Other required input states: HOLD = HIGH, DMAR = HIGH and RESET = LOW

Figure 17. Internal I/O read timing



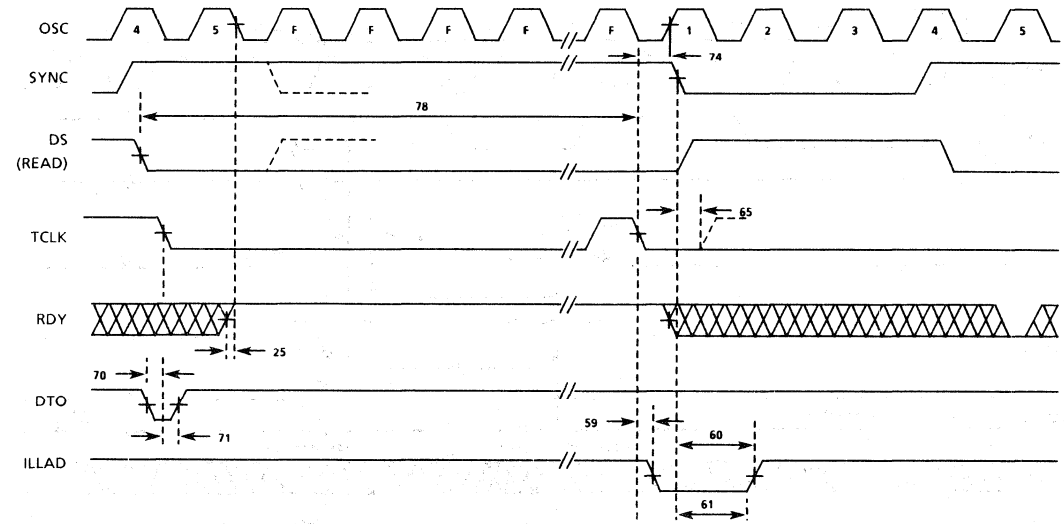
NOTE:
Other required input states: DTIMER = HIGH and RESET = LOW

Figure 18. DMA Access/Release Timing



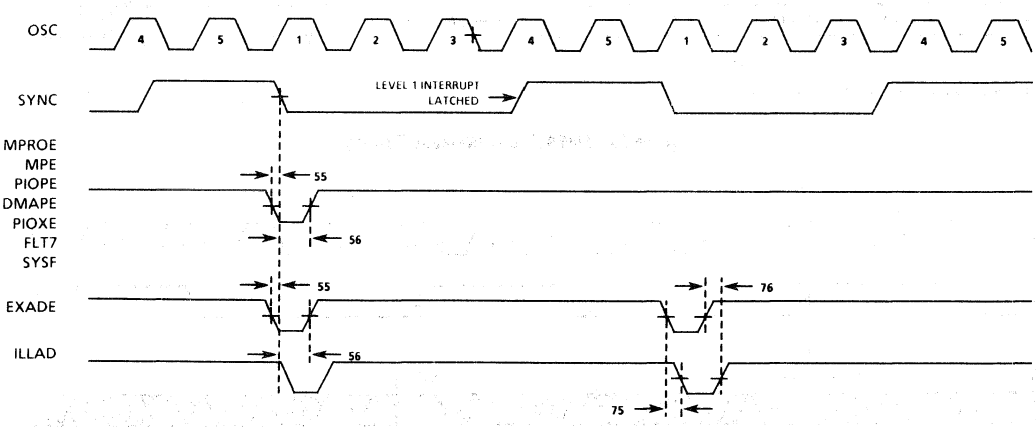
NOTES:
Other required input: RESET = LOW

Figure 19. Interrupt request timing



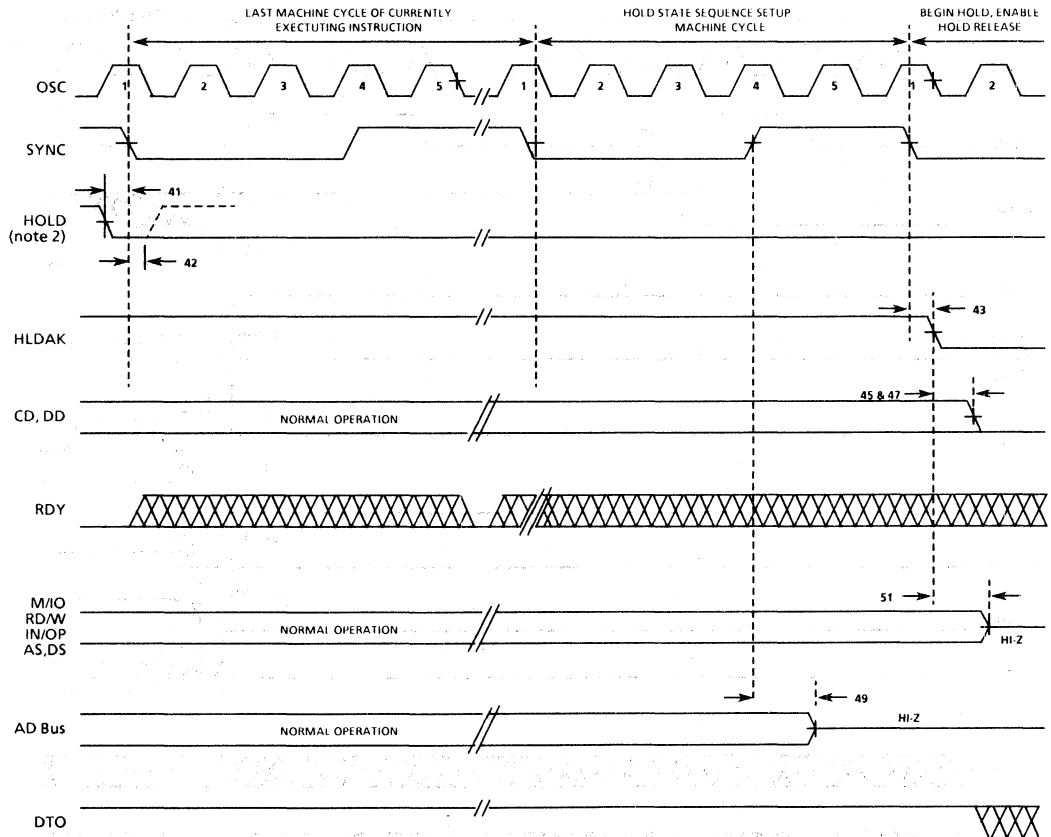
NOTES:
1. 2 TCLK falling edges during a continuous DS = low are necessary to cause a bus fault timeout.
2. Other output states : HLDAK = HIGH
3. Other required input states: DTO = HIGH and RESET = LOW

Figure 20. Bus fault timeout timing



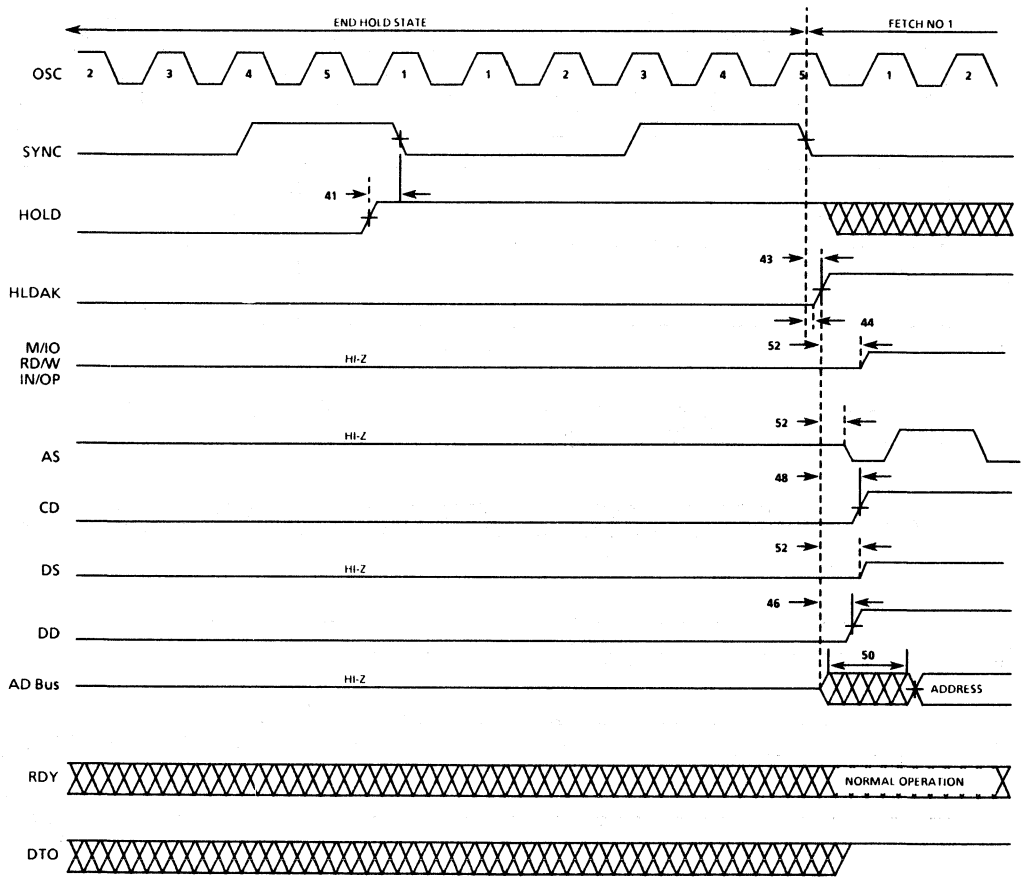
NOTES:
1. Assumes only one fault active at a time.
2. Buffered EXADE.
3. Other required input state: RESET = LOW

Figure 21. Fault capture timing



NOTES:
1. The "don7t care" state will continue to exist until HLDAK = HIGH, RDY will then resume normal operation.
2. HOLD falling may occur at any time during software execution. The diagram shows the last possible time it can occur and be assured of entering the Hold state after the current instruction completes execution.
3. Other required input states: RESET = LOW

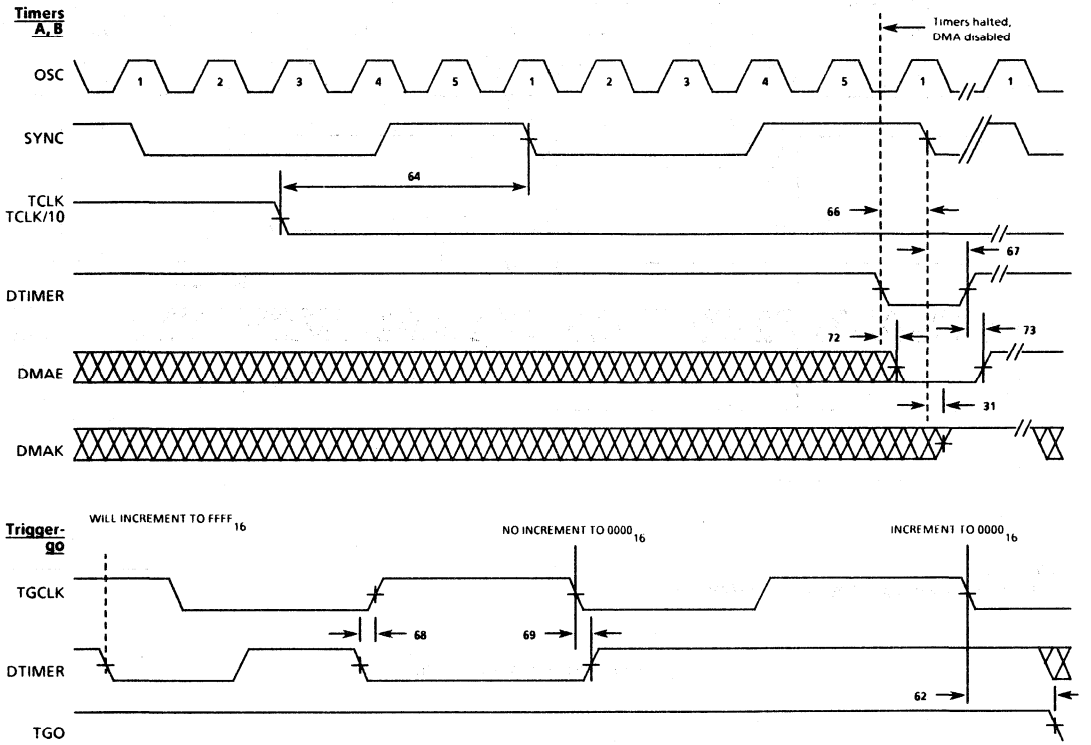
Figure 22. Hold state generation timing



NOTES:

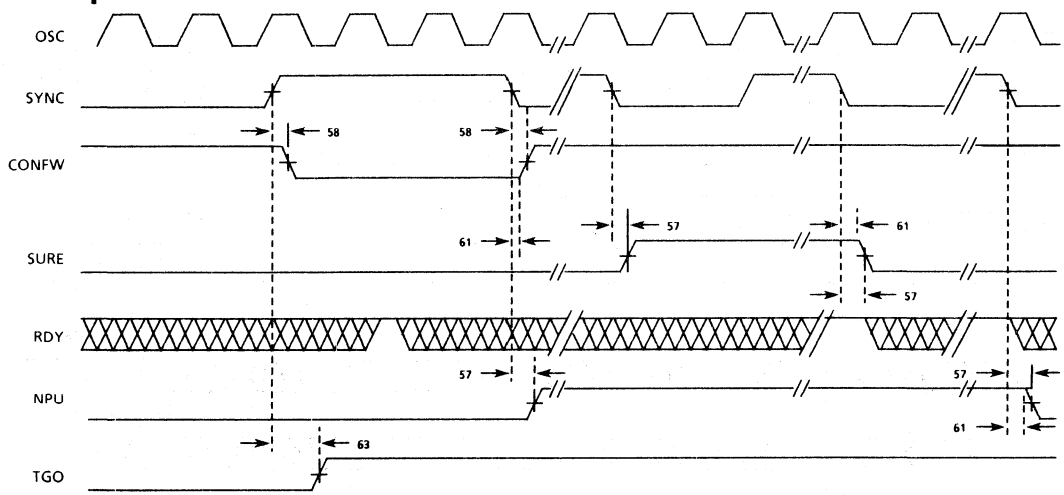
1. ADDRESS = IC(BPT) - 1, if BPT initiated the Hold state.
   ADDRESS = IC(Hold) - 2, if HOLD = LOW initiated the Hold state (unless changed by the monitor system).
2. Other output states : DMAK HIGH
3. Other required input states: DMAR = HIGH and RESET = LOW

Figure 23. Hold State Termination Timing



NOTES:
1. Other required input: RESET = LOW
2. TCLK/10 is the internally derived Timer B clock.
3. Timers A and B are clocked on the second SYNC falling edge after TCLK setup time is satisfied.

Figure 24. Timer Operations



NOTES:
1. Other required input states: RESET = LOW

Figure 25. Discrete outputs timing

6.0 Timing Parameters

NO.	Parameter	Test Condition (notes 1 & 9)	Min. (note 2)	Typ. (note 2)	Max. (note 2)	Units
1	RESET setup to SYNC lo (note 3)		-	-	30	ns
2	RESET hold after SYNC lo (note 3)		-	-	15	ns
3	RESET hi to RESET lo (note 3)		2	-	-	SYNC
4	OSC hi to SYNC lo	Load 1	10	25	40	ns
5	OSC hi to SYNC hi	Load 1	10	25	40	ns
6	SYNC lo to SYNC lo (notes 4 & 5)	Load 1	5_T - 2	5_T	5_T + 2	ns
7	SYNC lo to AS hi (note 6)	Load 2	1_T - 10	1_T - 3	1_T + 5	ns
8	SYNC lo to AS lo	Load 2	2.5_T - 10	2.5_T	2.5_T + 15	ns
9	SYNC lo to DS lo (read)	Load 2	3_T - 5	3_T + 1	3_T + 20	ns
10	SYNC lo to DS hi (read)	Load 2	0	9	30	ns
11	SYNC lo to DS lo (write)	Load 2	3_T - 5	3_T + 1	3_T + 20	ns
12	SYNC lo to DS hi (write) (note 5)	Load 2	4.5_T-5	4.5_T + 6	4.5_T + 30	ns
13	SYNC lo to DD lo	Load 1	3_T + 20	3_T + 32	3_T + 60	ns
14	SYNC lo to DD hi	Load 1	20	40	60	ns
15	SYNC lo to Address valid	Load 3	-	27	65	ns
16	Address valid after SYNC lo	Load 3	3_T - 5	3_T + 12	-	ns
17	SYNC lo to AD Bus Hi-Z (read) (note 7)	Load 3	-	-	3_T + 50	ns
18	SYNC lo to AD Bus active (read)	Load 3	5	-	-	ns
19	SYNC lo to Data valid (write)	Load 3	-	3_T + 29	3_T + 43	ns
20	Data valid after SYNC lo (write)	Load 3	8	-	-	ns
21	Data setup to SYNC lo (read)		30	22	-	ns
22	Data hold after SYNC lo (read) (note 8)	Load 3	0	-	-	ns
23	SYNC lo to M/IO, RD/W, IN/OP valid	Load 2	-	33	70	ns
24	M/IO, RD/W, IN/OP valid after SYNC lo	Load 2	5	-	-	ns
25	RDY setup to OSC lo		12	4	-	ns
26	RDY hold after OSC lo		10	-	-	ns
27	SYNC lo to DMAE valid	Load 1	-	50	85	ns
28	DMAE valid after SYNC lo	Load 1	5	-	-	ns
29	DMAR setup to SYNC lo		30	-	-	ns
30	DMAR hold after SYNC lo		10	-	-	ns

Notes:

1. Unless otherwise noted, test conditions are as follows: VIL = 0.5V, VIH = 3.0V, VIH_{OSC} = 4.0V, OSC duty cycle = 50%, input rise and fall time < 5ns, timing measured from 50% of VDD points.
2. τ = 1 OSC period. 0.5τ implies a 50% OSC duty cycle; fractional τ's may be adjusted to reflect actual OSC duty cycle.
3. Data obtained by characterisation or analysis, is not routinely mearsured.
4. Add 1τ for potential branch cycle
5. Add 1τ for internal XIO cycle; nτ for n memory wait states.
6. Excluding DMA or HOLD conditions
7. Measured to pre-Hi-Z steady state ± 10% of VDD.
8. Measurement minus $1x10^{-7}$ ln [1-(VIL-0.5/VDD-0.5)] nsecs.
9. Output references SYNC, DMAK, and HLDAK drive into load 1.

Table 8. Timing Parameters

NO.	Parameter	Test Condition (notes 1 & 9)	Min. (note 2)	Ttp. (note 2)	Max. (note 2)	Units
31	SYNC lo to DMAK valid	Load 1	-	35	45	ns
32	DMAK valid after SYNC lo	Load 1	5	-	-	ns
33	DMAK lo to DD lo	Load 1	-	-	50	ns
34	DMAK hi to DD hi	Load 1	-	-	80	ns
35	DMAK lo to CD lo	Load 1	-	-	50	ns
36	DMAK hi to CD hi	Load 1	-	-	50	ns
37	DMAK lo to AD Bus Hi-Z (note 7)	Load 3	-	-	70	ns
38	DMAK hi to AD Bus valid	Load 3	-	-	60	ns
39	DMAK lo to AS, DS, M/IO, RD/W, IN/OP Hi-Z (note 7)	Load 3 (AS), Load 4 (All else)	-	-	50	ns
40	DMAK hi to AS, DS M/IO, RD/W, IN/OP valid	Load 3 (AS), Load 4 (All else)	-	-	59	ns
41	HOLD setup to SYNC lo		40	-	-	ns
42	HOLD hold after SYNC lo		15	-	-	SYNC
43	SYNC lo to HLDAK valid	Load 1	-	2	20	ns
44	HLDAK valid after SYNC lo	Load 1	-7	-2	-	ns
45	HLDAK lo to DD lo	Load 1	-	-	50	ns
46	HLDAK hi to DD hi	Load 1	-	-	50	ns
47	HLDAK lo to CD lo	Load 1	-	-	50	ns
48	HLDAK hi to CD hi	Load 1	-	-	50	ns
49	HLDAK lo to AD Bus Hi-Z (Hold) (note 7)	Load 3	-	-	60	ns
50	HLDAK hi to AD bus valid	Load 3	-	-	50	ns
51	HLDAK to AS, DS M/IO, RD/W, IN/OP Hi-Z (note 7)	Load 3 (AS), Load 4 (All else)	-	-	50	ns
52	HLDAK to AS, DS M/IO, RD/W, IN/OP valid	Load 1	-	-	50	ns
53	Interrupts setup to SYNC lo		30	-	-	ns
54	Interrupts hold after SYNC lo		10	-	-	ns
55	Faults setup to SYNC lo		30	-	-	ns
56	Faults hold after SYNC lo		10	-	-	ns
57	SYNC lo to SURE, NPU valid	Load 1	-	-	85	ns
58	SYNC lo to CONFW valid	Load 1	-	-	85	ns
59	TCLK lo to ILLAD lo (Bus timeout)	Load 1	-	-	85	ns
60	SYNC lo to ILLAD hi (Bus timeout)	Load 1	-	-	85	ns

Notes:

1. Unless otherwise noted, test conditions are as follows: VIL = 0.5V, VIH = 3.0V, VIH_{OSC} = 4.0V, OSC duty cycle = 50%, input rise and fall time < 5ns, timing measured from 50% of VDD points.
2. τ = 1 OSC period. 0.5τ implies a 50% OSC duty cycle; fractional τ's may be adjusted to reflect actual OSC duty cycle.
7. Measured to pre-Hi-Z steady state ± 10% of VDD.
9. Output references SYNC, DMAK, and HLDAK drive into load 1.

Table 8 (continued). Timing Parameters

NO.	Parameter	Test Condition (notes 1 & 9)	Min. (note 2)	Typ. (note 2)	Max. (note 2)	Units
61	SURE, NPU, ILLAD, CONFW valid after SYNC lo	Load 1	5	-	-	ns
62	TGCLK lo to TGO lo (Timer clocking)	Load 1	-	-	150	ns
63	SYNC hi to TGO hi (Reset Trigger-Go XIO)	Load 1	-	-	100	ns
64	TCLK setup to SYNC lo		30	-	-	ns
65	TCLK hold after SYNC lo		10	-	-	ns
66	DTIMER setup to SYNC lo		60	-	-	ns
67	DTIMER hold after SYNC lo		10	-	-	ns
68	DTIMER setup to TGCLK hi		60	-	-	ns
69	DTIMER hold after TGCLK lo		20	-	-	ns
70	DTO setup to TCLK lo		60	-	-	ns
71	DTO hold after TCLK lo		10	-	-	ns
72	DTIMER lo to DMAE lo	Load 1	-	-	70	ns
73	DTIMER hi to DMAE normal operation	Load 1	-	-	70	ns
74	TCLK lo to Normal operation after bus timeout		-	-	100	ns
75	EXADE lo to ILLAD lo	Load 1	-	-	70	ns
76	EXADE hi to ILLAD hi	Load 1	-	-	70	ns
77	SYNC lo to DD hi (Internal to XIO) (note 3)	Load 1	-	-	60	ns
78	Bus fault timeout interval (note 3)		1	-	2	TCLK
79	DD hi to AS lo (DMA) (note 3)	Load 1 (DD), Load 2 (AS)	20	-	-	ns
80	DS hi to Data valid	Load 2 (DS), Load 3 (Data)	15	-	-	ns

Notes:

1. Unless otherwise noted, test conditions are as follows: VIL = 0.5V, VIH = 3.0V, VIH_{OSC} = 4.0V, OSC duty cycle = 50%, input rise and fall time < 5ns, timing measured from 50% of VDD points.
2. τ = 1 OSC period. 0.5τ implies a 50% OSC duty cycle; fractional τ's may be adjusted to reflect actual OSC duty cycle.
3. Data obtained by characterisation or analysis, is not routinely measured.
9. Output references SYNC, DMAK, and HLDAK drive into load 1.

Table 8 (continued). Timing Parameters

7.0 Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply voltage	-0.5	9	V
Input voltage	-0.3	V_{DD} + 0.3	V
Current through any pin	-20	20	mA
Operating temperature	-55	125	°C
Storage temperature	-65	150	°C

Table 9. Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8.0 DC Electrical Characteristics

Symbol	Parameter	Condition	Total Dose Radiation Not Exceeding $3x10^5$ RAD (Si)			Units
			Min.	Typ.	Max.	
V_{DD}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	TTL Input High Voltage		2.0			V
V_{IL}	TTL Input Low Voltage				0.8	V
V_{CH}	OSC Input High Voltage		4.0			V
V_{CL}	OSC Input Low Voltage				1.0	V
V_{OH}	TTL Output High Voltage	I_{OH} = -1.4mA	2.4			V
V_{OL}	TTL Output low Voltage	I_{OL} = 2.0mA			0.4	V
I_{IZ}	Input Leakage Current	V_{DD} = 5.5V			± 10	uA
I_{OZ}	Output Leakage Current	V_{DD} = 5.5V			± 20	uA
I_{DD}	Power Supply Current	f = 20MHz		70	150	mA

V_{DD} = 5V ± 10%, over full operating temperature range

Table 10. Operating DC Electrical Characteristics

MAS281
Radiation Hard MIL-STD-1750A Microprocessor

9.0 Chip Set Interconnection

To form the MAS281 processor from the individual chips MA17501, MA17502 and MA17503, connects should be made as shown below.

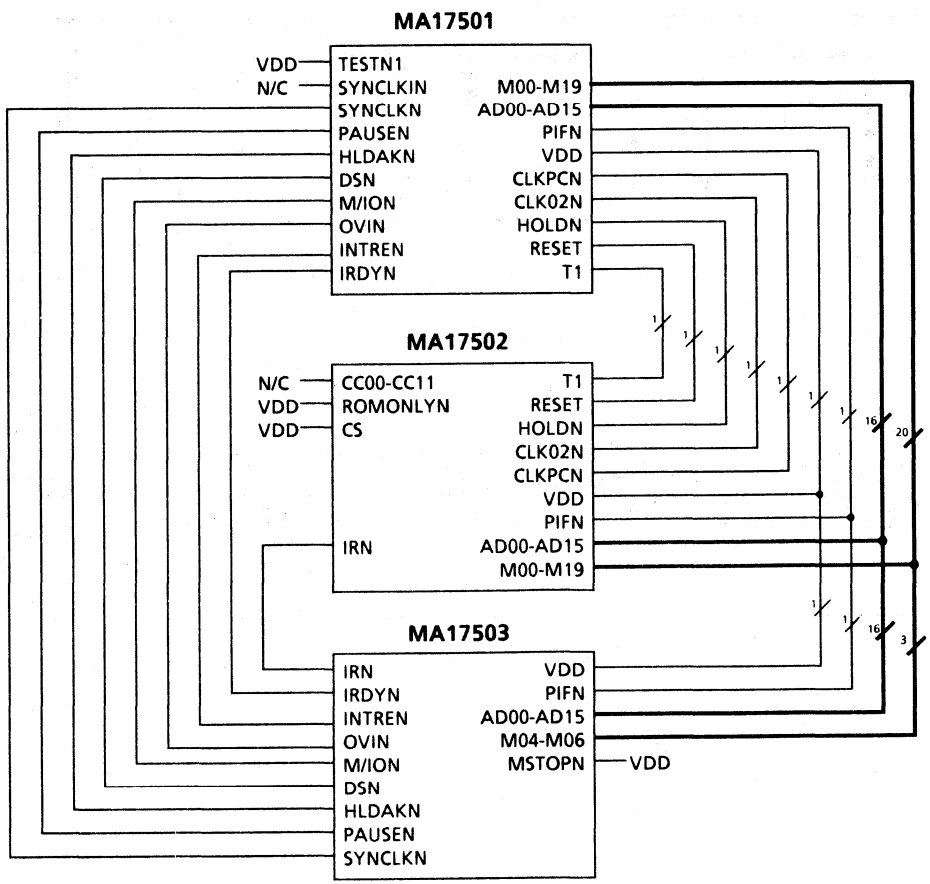
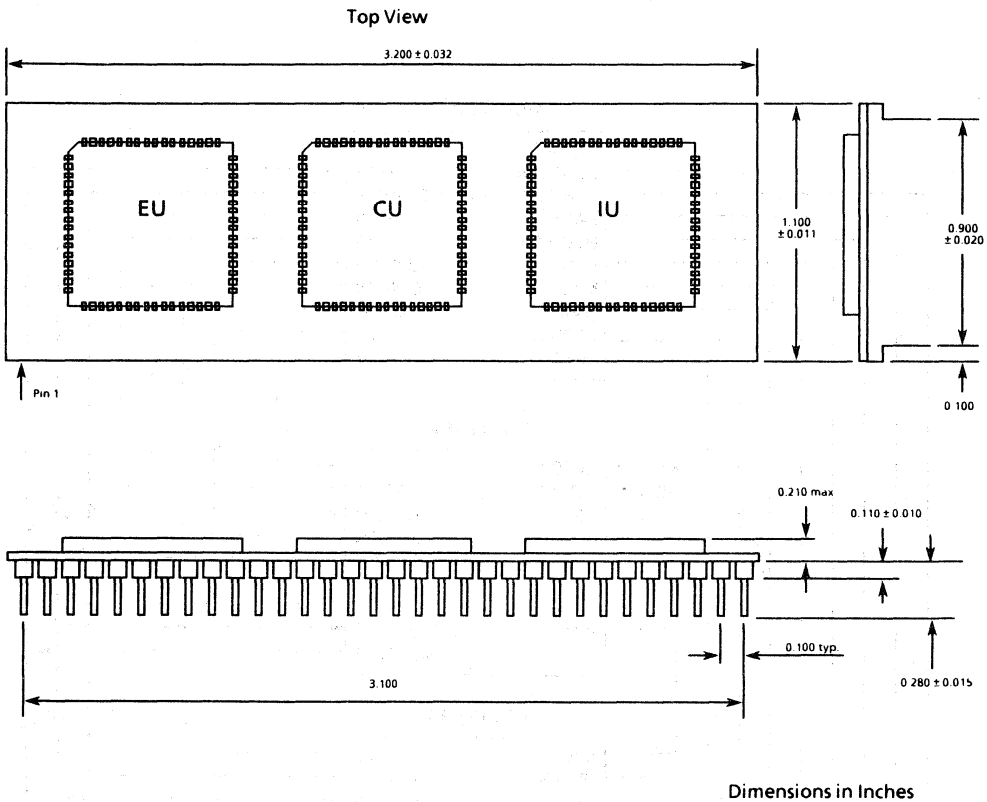


Figure 26. Chip Set Interconnection Diagram

GEC PLESSEY
SEMICONDUCTORS

10.0 Packaging Infomation

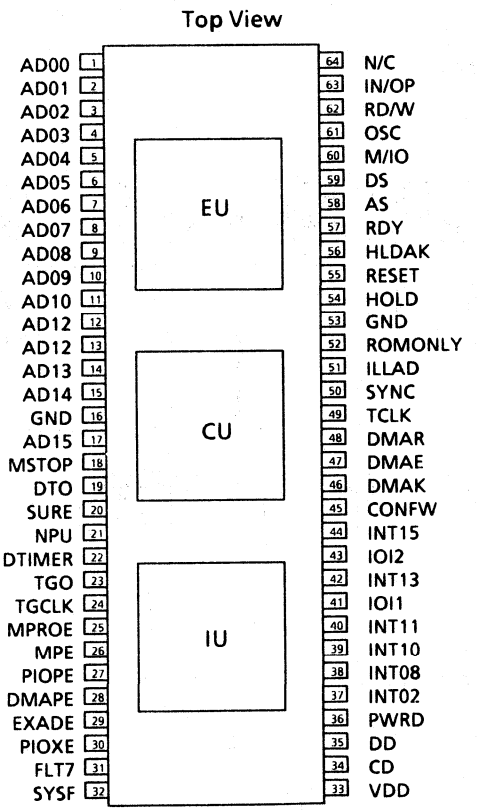
Dual-in-line Ceramic Module
(MAS281 - Package type C)



Dimensions in Inches

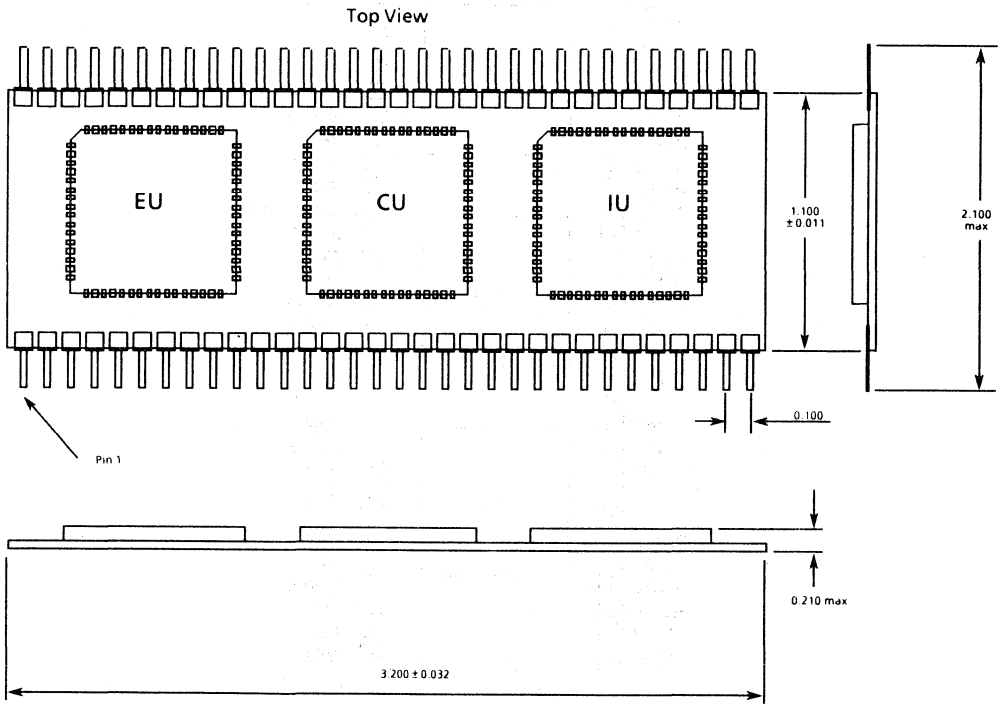
Figures 27a. Dimensioned Drawing

MAS281
Radiation Hard MIL-STD-1750A Microprocessor



Figures 27b. Pin Assignment

Flatpack Ceramic Module
(MAS281 - Package type F)



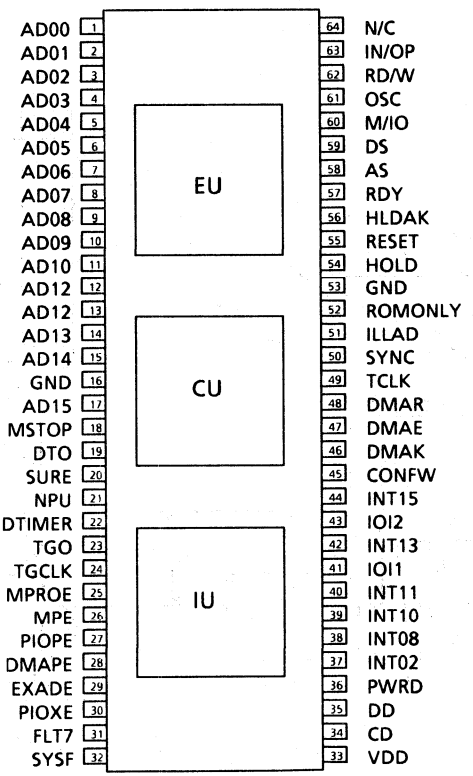
Dimensions in Inches

Figures 28a. Dimensioned Drawing

MAS281

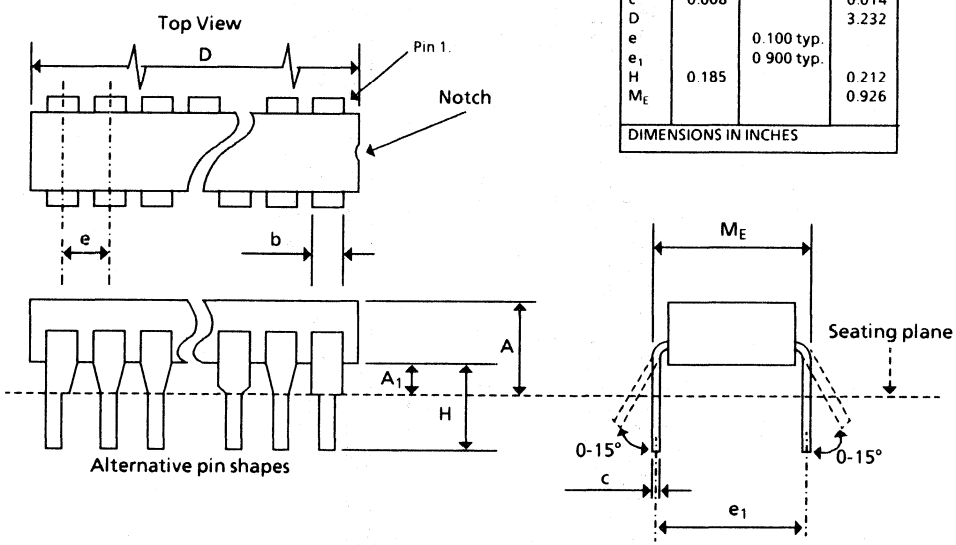
Radiation Hard MIL-STD-1750A Microprocessor

Top View



Figures 28b. Pin Assignment

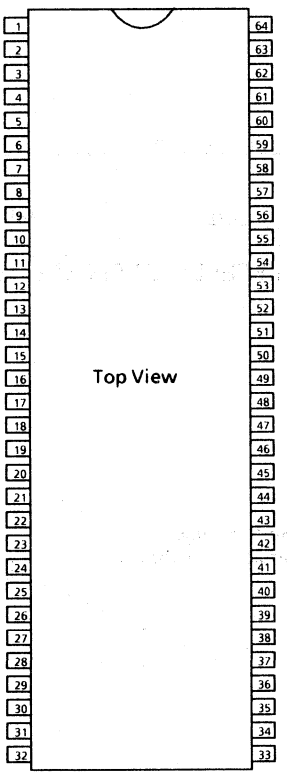
Ceramic Dual-in-line
(MA17501 to MA17503 - Package type C)



Ref.	Min.	Nom.	Max.
A			0.220
A_1	0.015		0.060
b	0.014		0.023
c	0.008		0.014
D			3.232
e		0.100 typ.	
e_1		0 900 typ.	
H	0.185		0.212
M_E			0.926
DIMENSIONS IN INCHES			

Figures 29a. Dimensioned Drawing

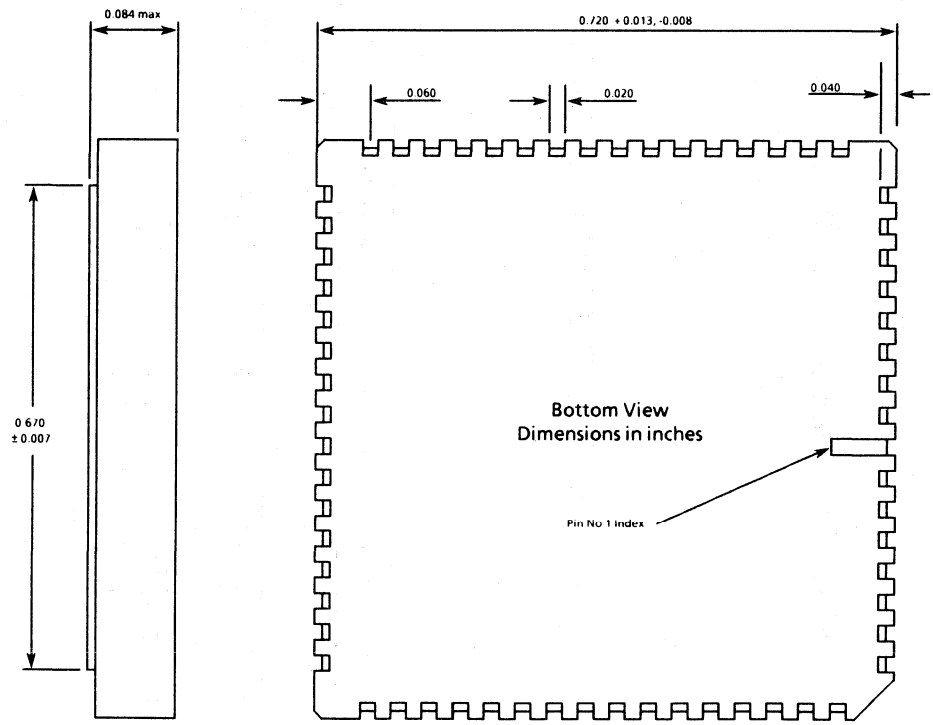
MAS281
Radiation Hard MIL-STD-1750A Microprocessor



Pin No.	17501	17502	17503
1	OSC	IRN	ILLADN
2	NC	VDD	DTON
3	SYSCLKIN	PIFN	SYNCLKN
4	SYNCLKN	AD00	DSN
5	CLKPCN	AD01	INTREN
6	CLK02N	AD02	CONFWN
7	AS	AD03	IRDYN
8	DSN	AD04	M/ION
9	GND	AD05	DMAKN
10	M/ION	AD06	DMAE
11	RD/WN	AD07	DMARN
12	GND	AD08	M04
13	IN/OPN	AD09	M05
14	INTREN	AD10	M06
15	PIFN	AD11	TCLK
16	M19	AD12	AD00
17	M18	AD13	AD01
18	M17	AD14	AD02
19	M16	AD15	AD03
20	M15	CLK02N	AD04
21	M14	CLKPCN	AD05
22	M13	M19	AD06
23	M12	M18	AD07
24	M11	M17	AD08
25	M10	M16	AD09
26	M09	M15	AD10
27	M08	M14	AD11
28	M07	M13	AD12
29	M06	M12	AD13
30	M05	M11	AD14
31	M04	M10	AD15
32	M03	M09	GND
33	M02	M08	MSTOPN
34	M01	NC	SURE
35	M00	M07	NPU
36	TESTN	M06	DDN
37	AD15	M05	DTIMERN
38	AD14	M04	TGON
39	AD13	M03	TGCLK
40	AD12	M02	CDN
41	NC	M01	PIFN
42	VDD	GND	MPROEN
43	AD11	CS	MPEN
44	AD10	M00	PIOPEN
45	AD09	CC00	DMAPEN
46	AD08	CC01	EXADEN
47	AD07	CC02	PIOXEN
48	AD06	CC03	FLT7N
49	AD05	CC04	SYSFN
50	AD04	CC05	VDD
51	AD03	CC06	IRN
52	GND	CC07	PAUSEN
53	AD02	CC08	OVI
54	AD01	CC09	PWRDN
55	AD00	CC10	INT02N
56	HOLDN	CC11	INT08N
57	RESET	ROMONLYN	INT10N
58	HLDAKN	NC	INT11N
59	PAUSEN	GND	IOI1N
60	T1	NC	INT13N
61	OVIN	NC	IOI2N
62	IRDYN	T1	INT15N
63	RDYN	RESET	HLDAKN
64	SYNCN	HOLDN	NC

Figures 29b. Pin Assignments

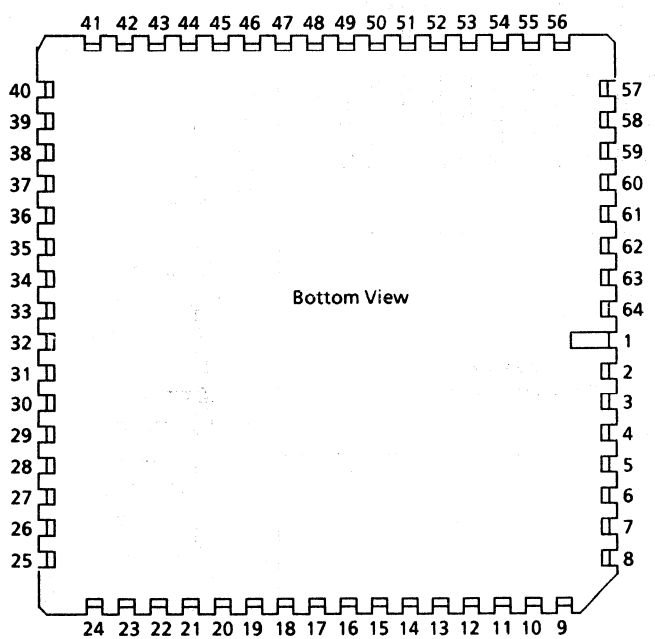
Leadless Chip Carrier
(MA17501 to 3 - Package type L)



Figures 30a. Dimensioned Drawing

MAS281

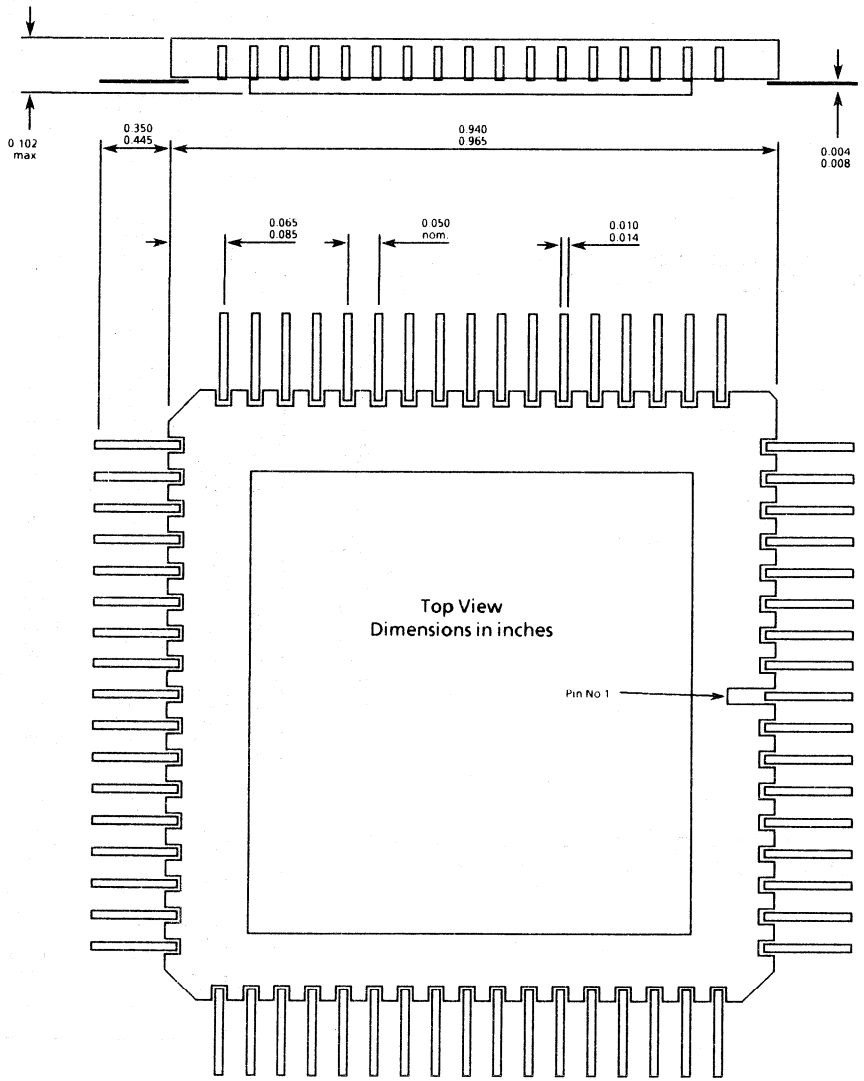
Radiation Hard MIL-STD-1750A Microprocessor



Pin No.	17501	17502	17503
1	OSC	IRN	ILLADN
2	NC	VDD	DTON
3	SYSCLK1N	PIFN	SYNCLKN
4	SYNCLKN	AD00	DSN
5	CLKPCN	AD01	INTREN
6	CLK02N	AD02	CONFWN
7	AS	AD03	IRDYN
8	DSN	AD04	M/ION
9	GND	AD05	DMAKN
10	M/ION	AD06	DMAE
11	RD/WN	AD07	DMARN
12	GND	AD08	M04
13	IN/OPN	AD09	M05
14	INTREN	AD10	M06
15	PIFN	AD11	TCLK
16	M19	AD12	AD00
17	M18	AD13	AD01
18	M17	AD14	AD02
19	M16	AD15	AD03
20	M15	CLK02N	AD04
21	M14	CLKPCN	AD05
22	M13	M19	AD06
23	M12	M18	AD07
24	M11	M17	AD08
25	M10	M16	AD09
26	M09	M15	AD10
27	M08	M14	AD11
28	M07	M13	AD12
29	M06	M12	AD13
30	M05	M11	AD14
31	M04	M10	AD15
32	M03	M09	GND
33	M02	M08	MSTOPN
34	M01	NC	SURE
35	M00	M07	NPU
36	TESTN	M06	DDN
37	AD15	M05	DTIMERN
38	AD14	M04	IGON
39	AD13	M03	IGCLK
40	AD12	M02	CDN
41	NC	M01	PIFN
42	VDD	GND	MPROLN
43	AD11	CS	MPEN
44	AD10	M00	PIOPEN
45	AD09	CC00	DMAPEN
46	AD08	CC01	EXADEN
47	AD07	CC02	PIOXEN
48	AD06	CC03	FLT2N
49	AD05	CC04	SYSFN
50	AD04	CC05	VDD
51	AD03	CC06	IRN
52	GND	CC07	PAUSEN
53	AD02	CC08	OVI
54	AD01	CC09	PWRDN
55	AD00	CC10	INT02N
56	HOLDN	CC11	INT08N
57	RESET	ROMONLYN	INT10N
58	HLDAKN	NC	INT11N
59	PAUSEN	GND	IOI1N
60	I1	NC	INT13N
61	OVIN	NC	IOI2N
62	IRDYN	I1	INT15N
63	RDYN	RESET	HLDAKN
64	SYNCN	HOLDN	NC

Figures 30b. Pin Assignments

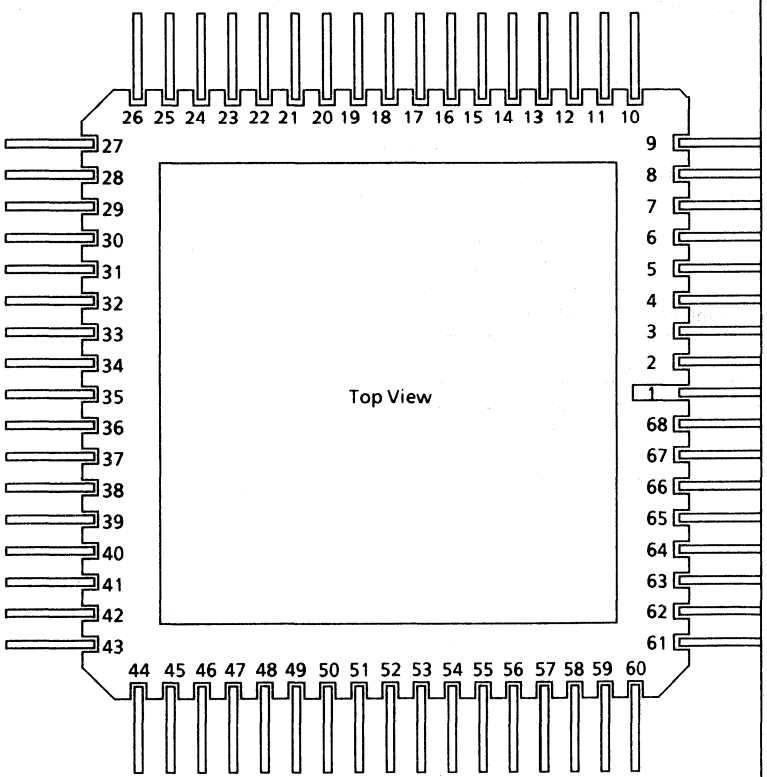
Topbraze Flatpack
(MA17501 to 3 - Package type F)



Figures 31a. Dimensioned Drawing

MAS281

Radiation Hard MIL-STD-1750A Microprocessor



Pin No.	17501	17502	17503
1	OSC	IRN	NC
2	NC	NC	ILLADN
3	NC	VDD	DTON
4	SYSCLK1N	PIFN	SYNCLKN
5	SYNCLKN	AD00	DSN
6	CLKPCN	AD01	INTREN
7	CLK02N	AD02	CONFWN
8	AS	AD03	IRDYN
9	DSN	AD04	M/ION
10	NC	AD05	DMAKN
11	GND	AD06	DMAL
12	M/ION	AD07	DMARN
13	RD/WN	AD08	M04
14	GND	AD09	M05
15	NC	AD10	M06
16	IN/OPN	AD11	TCLK
17	INTREN	AD12	AD00
18	PIFN	AD13	AD01
19	M19	AD14	AD02
20	M18	AD15	AD03
21	M17	CLK02N	AD04
22	M16	CLKPCN	AD05
23	M15	M19	AD06
24	M14	M18	AD07
25	M13	M17	AD08
26	M12	M16	NC
27	M11	M15	AD09
28	M10	M14	AD10
29	M09	M13	AD11
30	M08	M12	AD12
31	M07	M11	AD13
32	M06	M10	AD14
33	M05	M09	AD15
34	M04	M08	NC
35	M03	NC	GND
36	M02	NC	MSTOPN
37	M01	M07	SURE
38	M00	M06	NPU
39	TESTN	M05	DDN
40	AD15	M04	DTIMERN
41	AD14	M03	TGON
42	AD13	M02	TGCLK
43	AD12	M01	CDN
44	NC	NC	PIFN
45	NC	GND	MPROEN
46	VDD	CS	MPEN
47	AD11	M00	PIOPEN
48	AD10	CC00	DMAPEN
49	AD09	CC01	EXADEN
50	AD08	CC02	PIOXEN
51	AD07	CC03	FLT/N
52	AD06	CC04	SYSFN
53	AD05	CC05	VDD
54	AD04	CC06	NC
55	AD03	CC07	IRN
56	GND	CC08	PAUSEN
57	AD02	CC09	OVI
58	AD01	CC10	PWRDN
59	AD00	CC11	INT02N
60	HOLDN	ROMONLYN	INT0BN
61	RESET	NC	INT10N
62	HLDAKN	GND	INT11N
63	PAUSEN	NC	IOI1N
64	T1	NC	INT13N
65	OVIN	NC	IOI2N
66	IRDYN	T1	INT15N
67	RDYN	RESET	HLDAKN
68	SYNCN	HOLDN	NC

Figures 31b. Pin Assignments

Radiation Hard MIL-STD-1750A Microprocessor

11.0 Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Total Dose (Function to specification, note 1)	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$1x10^{10}$ Rad(Si)/s
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/s
Neutron Hardness (Function to specification)	$1x10^{15}$ neutrons/cm2
Latch-up	Not possible
Single Event Upset (note 2)	$<10^{-10}$ errors/bit day

Note 1. Typical performance only, for guaranteed levels see ordering information
2. GSO 10% Worst Case

MAS281

Radiation Hard MIL-STD-1750A Microprocessor

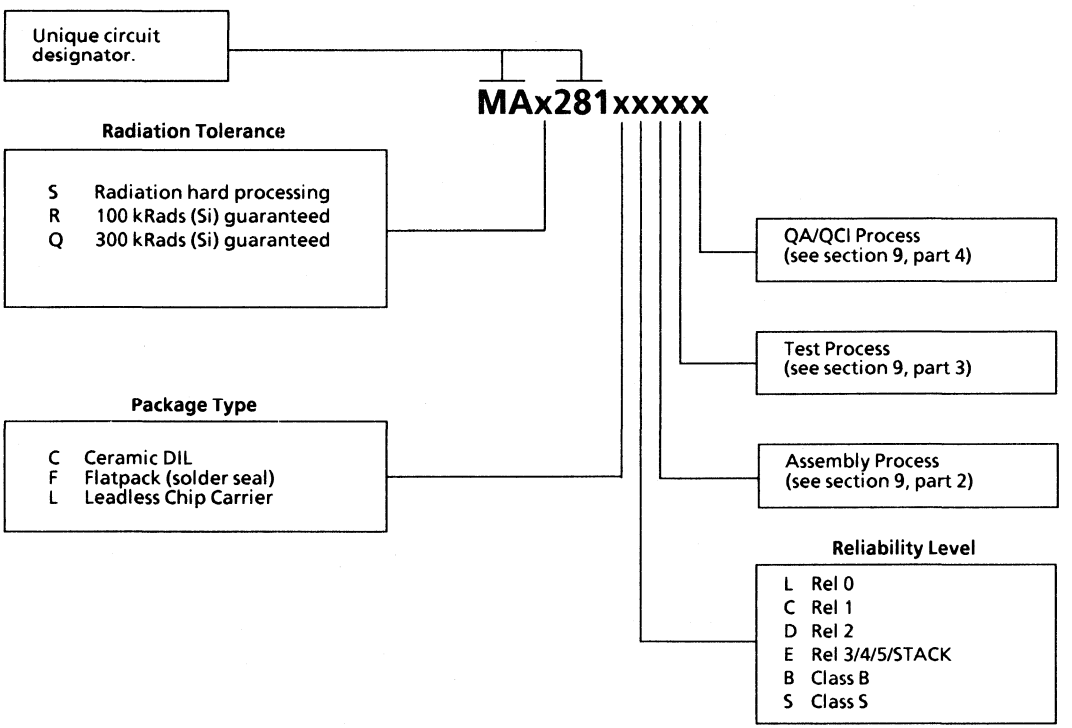
12.0 Ordering Information

The processor can be ordered in the form of a module, consisting of three chips in leadless chip carriers, mounted on a ceramic tile. The module can be supplied with dual-inlline (C) or flatpack (F) lead configurations.

Module - MAx281xxx

The three chips which form the processor can be packaged as separate devices. They are available in leadless chip carrier (L), flatpack (F), or ceramic dual-in-line packages (C).

Chip Set - MAx17501xxx
- MAx17502xxx
- MAx17503xxx



For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.

GEC PLESSEY

SEMICONDUCTORS

MA17501

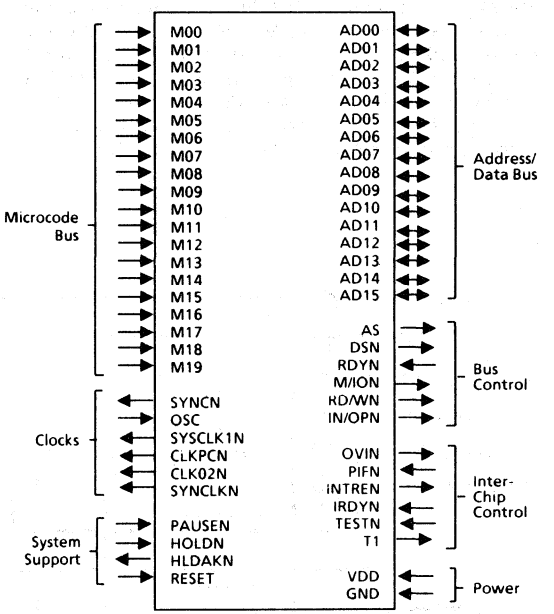
MIL-STD-1750A Execution Unit

S10211FDS Issue1 September 1990

Features

- MIL-STD-1750A Instruction Set Architecture
- Full Performance over Military Temperature Range (-55°C to + 125°C)
- Radiation Hard CMOS/SOS Technology
- 16-Bit Bidirectional Address/Data Bus
- 16-Bit Full Function Registered ALU
- 32-Bit Barrel Shifter
- 24 x 16-Bit Dual-Port RAM File
  - 16 User Accessible General Purpose Registers
  - 8 Microcode Accessible Registers
- 4 x 24-Bit Parallel Multiplier
  - 48-Bit Accumulator
  - 16-Bit x 16-Bit Multiply in 4 Machine Cycles
- Instruction Pre-Fetch
- MAS281 Integrated Built-in Self Test
- TTL Compatible System Interface

Block Diagram



General Description

The MA17501 Execution Unit is a component of the Marconi Electronic Devices MAS281 chip set. Other chips in the set include the MA17502 Control Unit and the MA17503 Interrupt Unit. Also available is the peripheral MA17504 Memory Management Unit/Block Protection Unit. These chips in conjunction implement the full MIL-STD-1750A Instruction Set.

The MA17501 - consisting of a full function 16-bit ALU, 24 x 16-bit dual-port RAM register file, 32-bit barrel shifter, 4 x 24-bit parallel multiplier, synchronisation clock generation logic, and microcode decode logic - provides all computational, logical, and synchronisation functions for the chip set. Table 1 provides brief signal definitions.

The MA17501 is offered in several package styles including; dual-in-line, flatpack and leadless chip carrier. Full packaging information is given at the end of the document.

1.0 System Considerations

The MA17501 Execution Unit (EU) is a component of the Marconi Electronic Devices MAS281 chip set. This chip set implements the full MIL-STD-1750A instruction set architecture. The other chips in the set are the MA17502 Control Unit (CU) and the MA17503 Interrupt Unit (IU). Also available is the peripheral MA17504 Memory Management Unit/Block Protection Unit (MMU(BPU)).

Figure 1 depicts the relationship between the chip set components.The EU provides the arithmetic and logical computation resources for the chip set. The EU also provides program sequencing logic in support of branching and subroutine functions. The IU provides interrupt and fault handling resources, DMA interface control signals, and the three MIL-STD-1750A timers. The EU and IU are each controlled by microcode from the CU. The MMU(BPU) may be configured to provide either 1M-word memory management (MMU) or 1K-word memory block write protection (BPU) functions.

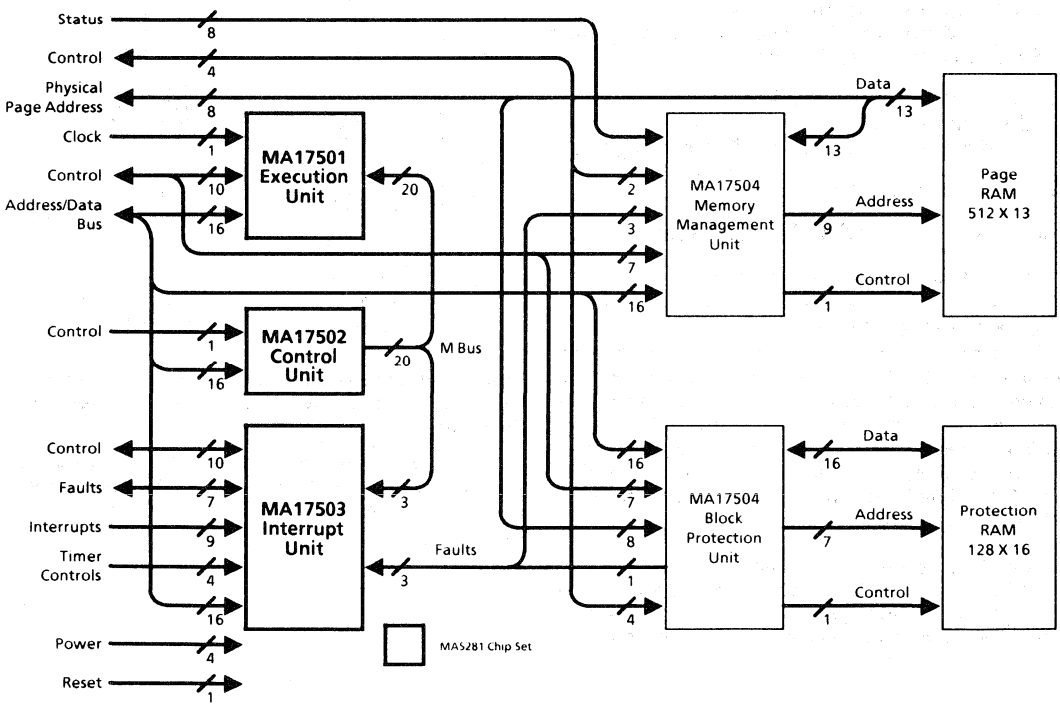


Figure 1. MAS281 Chip Set with optional MA17504 & Support RAMs

Signal	I/O	Definition
AD00 - AD15	I/O	External 16-Bit Address/Data Bus
$\overline{AS}$	O/Z	Address Strobe Indicates Address Information on A/D Bus
$\overline{CLKPC}$	0	Precharge Clock
$\overline{CLK02}$	0	Phase 2 Clock
$\overline{PAUSE}$	I	DMA Acknowledge (A/D Bus to be used for DMA)
$\overline{DS}$	O/Z	Data Strobe Indicates Data Information on A/D Bus
$\overline{HLDAK}$	0	Hold Acknowledge
$\overline{HOLD}$	I	Hold Request Suspends Internal Processor Functions
$\overline{IN/OP}$	O/Z	Instruction/Operand Indicates Type of Memory Access
$\overline{INTRE}$	0	Interrupt Enable
$\overline{IRDY}$	I	Interrupt Unit Ready Signal
M/$\overline{IO}$	O/Z	Memory or Input/Output Indicates Transaction on A/D Bus
M00 - M19	I	20-Bit Microcode Bus
$\overline{OSC}$	I	External Oscillator Clock
$\overline{OVI}$	0	Overflow Indicator
$\overline{PIF}$	I	Privileged Instruction Fault
RD/$\overline{W}$	O/Z	Read/Write Indicates Data Direction on A/D Bus
$\overline{RDY}$	I	Ready Informs CPU of the Conclusion of External Bus Cycle
$\overline{RESET}$	I	Reset Indicates Device Initialization
$\overline{SYNCLK}$	0	Interrupt Unit's Sync Clock
$\overline{SYNC}$	0	System Clock - CPU Sync Clock (External)
$\overline{SYSCLK1}$	0	System Clock (Internal)
$\overline{TEST}$	I	Test Enable
T1	0	Branch or Jump Control
VDD		Power (External), 5 Volts
GND		Ground

Table 1. Signal Definitions

As shown in Figure 1, the MAS281 is the minimum processor configuration consisting of an Execution Unit, a Control Unit, and an Interrupt Unit. This configuration is capable of accessing a 64K-word address space. Addition of a MMU configured MA17504 allows access to a 1M-word address space. Addition of a BPU configured MA17504 provides hardware support for 1K-word memory block write protection.

The EU, as with all components of the MAS281 chip set, is fabricated with Marconi Electronic Devices CMOS/SOS process technology. Input and output buffers associated with signals external to the MAS281 are TTL compatible.

Detailed descriptions of the EU's companion chips are provided in separate data sheets. Additional discussions on chip set system considerations, interconnection details, and DAIS mix benchmarking analysis are provided in separate applications notes.

2.0 Architecture

The Execution Unit consists of a full function 16-bit ALU, 32-bit barrel shifter, 4 x 24-bit parallel multiplier, 24 x 16-bit dual-port RAM register file, processor status word register, three operand transfer registers, three instruction fetch registers, various interconnect buses, synchronization clock generation logic, and microcode decode logic. Details of these components are depicted in Figure 2 and are discussed below:

2.1 ALU

The ALU is a full function 16-bit arithmetic/logic unit capable of performing arithmetic and logic operations on either one or two 16-bit operands in a single machine cycle. In addition to operand manipulation, the ALU is used to compute memory addresses.

The ALU supports 16-bit fixed-point single-precision, 32-bit fixed-point double-precision, 32-bit floating-point, and 48-bit floating-point extended-precision data in two's complement representation. Double-precision and extended-precision operands are passed through the ALU 16 bits at a time on consecutive machine cycles. Machine flags provide an indication of ALU results and are used to set condition status (CS) bits C, P, Z, and N in the Status Word Register. Condition status bits and the Status Word register are discussed below.

2.2 Barrel Shifter

The Barrel Shifter is a 32-bit input, 16-bit output right shift network. A 32-bit operand may be shifted right arithmetically, logically, or cyclically up to 31 bit positions in a single machine cycle. While not directly accessible or visible to user programs, the Barrel Shifter is utilized by microcode to effect all shift, rotate, and normalize instructions with minimum execution time.

2.3 Parallel Multiplier

The Parallel Multiplier performs a 4-bit multiplier by 24-bit multiplicand multiplication plus accumulation in a single machine cycle. Only four machine cycles are required to complete a 16-bit by 16-bit multiplication. Contained within the multiplier is a 48-bit product accumulation register with the lower 24 bits serving as a source operand register.

On each multiply machine cycle, the lower four bits of the accumulator are multiplied by 24 bits from the two ALU operand source buses (R and S). The lower 24 bits of this 28-bit product are then added to the upper 24 bits of the accumulator and the whole accumulator is shifted right four bits. This right shift makes room for the upper four bits of the product. The four bits shifted out are used in the next multiply iteration.

2.4 Dual-Port Register File

The Register File is a dual port RAM structure containing 24, 16-bit registers. Sixteen of these registers are general purpose and user accessible. These user accessible registers - referred to as R0 through R15 - may be used as accumulators, index registers, base registers temporary operand registers, or stack pointers. The remaining eight registers are only accessible by microcode.

Adjacent registers are concatenated to effectively form 32-bit and 48-bit registers for storage of double-precision and extended-precision operands, respectively. Instructions access these operands by specifying the register containing the most significant part of the operand, and the register set wraps around automatically under microcode control, e.g., R15 concatenates with R0 for 32-bit operands and R15 concatenates with R0 and R1 for 48-bit operands.

2.5 Status Word Register

The Status Word Register (SW) holds the condition status (CS) bits C, P, Z, and N generated by ALU operations. The SW also stores the address state (AS) and processor state (PS) fields. Figure 3 defines the Status Word Register storage format.

The CS bits are stored with each logical, shift, and arithmetic operation performed by the ALU as required by MIL-STD-1750A and remain valid until changed by subsequent operations. The CS bits are interrogated during "jump on condition" and "instruction counter relative" MIL-STD-1750A branch instructions.

MA17501
MIL-STD-1750A Execution Unit

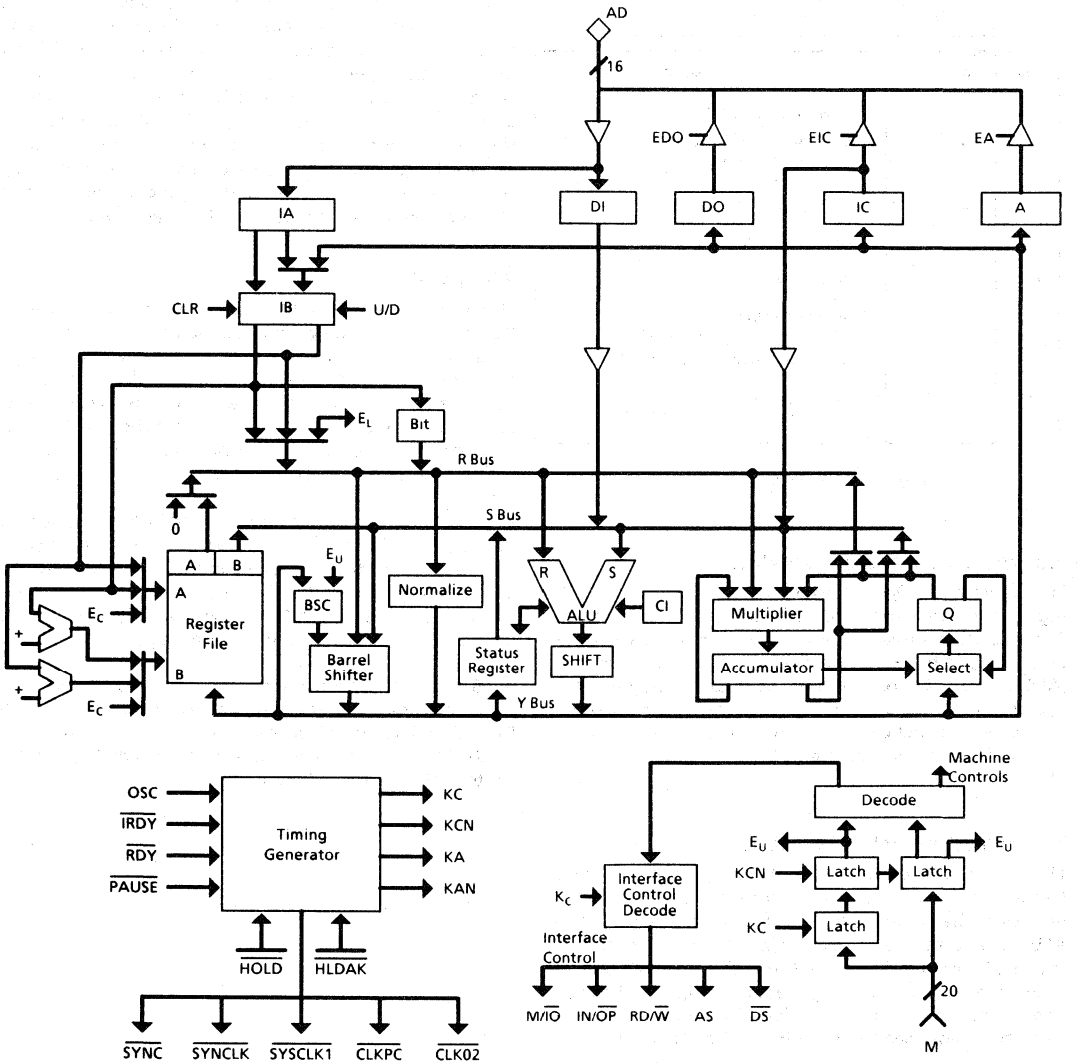
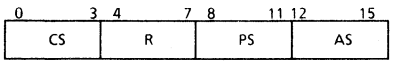


Figure 2. MA17501 Execution Unit Architecture



Field	Bits	Description
CS		CONDITION STATUS:
	0	C- Carry from an addition or no borrow from a subtraction
	1	P- Result >0
	2	Z- Result = 0
	3	N- Result<0
R	4 - 7	RESERVED
PS	8 - 11	PROCESSOR STATE: (a)- Memory access key code (b)- Privileged instruction enable
AS	12 - 15	ADDRESS STATE: Page register sets for expanded memory addressing

Figure 3. Status Word Format

2.5 Operand Transfer Registers

The Address (A), Data Output (DO), and Data Input (DI) registers are referred to as Operand Transfer Registers. These registers serve as storage buffers between internal EU buses and the EU's externally accessible address/data (AD) Bus. The DO register buffers data transferred from the EU to the AD Bus. The A register buffers operand addresses and XIO commands onto the AD Bus. The DI register buffers data transferred from the AD Bus to the EU.

2.6 Instruction Fetch Registers

The Instruction Counter (IC), Instruction A (IA), and Instruction B (IB) registers allow sequential instruction fetches to be performed without assistance from the ALU. The IC register, which holds the 16-bit address of the next instruction to be fetched from memory, is loaded automatically by reset, jump, or branch operations. Once loaded, it functions as a dedicated counter to sequence from one instruction to the next.

The current IC contents may be stored in registers R0 through R15 or in memory (pushed onto a stack) to provide return linkages for subroutine calls. As part of the microcoded interrupt handling routine the IC is saved in memory via the interrupt linkage pointer.

Registers IA and IB provide an instruction look-ahead capability. In the case of 16-bit instructions, IB holds the instruction currently executing while IA holds the next instruction to be executed. In the case of 32-bit instructions, IB and IA each hold half of the instruction. IA and DI (DI stores the immediate operands) are loaded as the instruction in IA is transferred to IB for execution; if the instruction in IB uses an immediate operand, IA is reloaded with the next instruction while DI maintains the immediate data. This overlapping of operations allows higher performance levels to be achieved.

2.7 Buses

Three 16-bit wide buses (R, S, and Y) interconnect the EU data storage and computational elements. The R and S buses accept operands from selected EU data storage elements and route them to inputs of selected EU computational elements. The Y, or destination, bus serves to route computational results either back to EU data storage and computational elements or to the various operand transfer registers.

A 16-bit multiplexed Address/Data (AD) Bus provides a communications path between the EU, other components of the MAS281 chip set, and any other devices mapped into the chip set's address space. Data transfers between the AD Bus and the R, S, and Y buses are buffered by the operand transfer registers.

A 20-bit multiplexed microcode (M) bus provides a pathway between the Control Unit (CU) and the Execution Register (E) buffered microcode decode logic on the EU chip. Microcode placed on this bus by the CU controls all actions of the EU.

2.8 Synchronisation Clock Generation Logic

The Execution Unit generates all of the synchronisation clocks required by the chip set and CPU system. The EU converts an externally supplied oscillator signal into five synchronisation signals: SYNCN, SYSCLK1N, SYNCLKN, CLKPCN, CLK02N. The EU generates SYNCN for elements external to the chip set whereas SYNCLKN and SYSCLK1N are generated for the Interrupt Unit and internal EU synchronisation, respectively. SYSCLK1N is also brought out on a pin for use by external monitoring systems. The EU generates CLKPCN and CLK02N for use in the Control Unit. The CU uses CLKPCN to precharge the M Bus and transmit the first microword while CLK02N is used to transmit microword two.

The EU also contains the wait state generation interface. Failure of memory or I/O subsystems to drive RDYN low at the proper time during the DSN pulse causes the EU to hold SYNCLKN, SYNCN, SYSCLK1N, and CLKPCN in the high state; CLK02N, AS, DSN, IN/OPN, and M/ION in the low state; and RD/WN in its current state for one or more oscillator cycles beyond the end of the normal five OSC cycle machine cycle. When RDYN is asserted low, the EU allows the machine cycle to conclude at the high-to-low transition of the current oscillator cycle. This will allow all the synchronisation and control signals to resume normal operation.

Additionally, IRDYN is used to signal completion of internal I/O command control of the Interrupt Unit (IU). The IU thus can extend the duration of the above mentioned bus signals. Failure of the IU to drive IRDYN low at the proper time during the DSN low pulse causes the EU to hold SYNCLKN, SYNCN, SYSCLK1N, and CLKPCN in the high state; CLK02N, AS, and DSN in the low state; and IN/OPN, M/ION, and RD/WN in their current states for one or more oscillator cycles beyond the end of the normal five OSC cycle machine cycle. When the IU asserts IRDYN low, the EU allows the machine cycle to conclude at the high-to-low transition of the current oscillator cycle. This will allow all the synchronisation and control signals to resume normal operation.

[**NOTE:** Whenever the EU is executing a machine cycle which requires IRDYN to drop low for completion, the machine cycle will be a minimum of six OSC cycles long. The maximum duration of this machine cycle depends on the length of time that the IU holds IRDYN high.]

3.0 Interface Signals

All signals comply with the voltage levels of Table 1. In addition, each of these functions is provided with Electrostatic Discharge (ESD) protection diodes. All unused inputs must be held to their inactive state via a connection to VDD or GND. A 500-ohm pull-up at the OSC input pin is recommended to damp line reflections.

Throughout this data sheet, active low signals are denoted by either a bar over the signal name or by following the name with an "N" suffix, e.g., HOLDN. Referenced signals that are not found on the MA17501 are preceded by the originating chip's functional acronym in parentheses, e.g., (IU)DMARN.

A description of each pin function, grouped according to functional interface, follows. The function acronym is presented first, followed by its definition, its type, and its detailed description. Function type is either input, output, high impedance (Hi-Z), or a combination thereof. Timing characteristics of each of the functions described is provided in Section 5.0.

3.1 Power Interface

The power interface consists of one 5V VDD connection and three common GND pins.

3.2 Clocks

The Execution Unit provides the synchronisation clocks for the MAS281 chip set. Together these clocks form the basic operation cycle.

3.2.1 Oscillator (OSC)

Input. The MA17501 requires a single external oscillator input for operation. The EU converts the oscillator into the five other clocks listed in this section. To minimise skew between OSC edges and signals derived from OSC, the OSC rise and fall times should be minimised. It is recommended that a clock driver with high drive capability, such as a 54AS244, 54ALS244 or 54HST240, be used to drive the OSC input.

In order to avoid double clocking due to line reflections, a 500-ohm pull-up resistor, placed close to the EU, is recommended.

3.2.2 Synchronisation Clock (SYNCN)

Output. The MA17501 provides the MAS281 Synchronisation Clock output to synchronise external circuitry to the MAS281 machine cycle. The high-to-low transition of this signal indicates the start of a new machine cycle.

SYNCN cycles associated with external memory or I/O bus transactions are a minimum of five OSC cycles in duration and may be extended by inserting wait states via the RDYN input. SYNCN low indicates that either an address or XIO command is on the AD Bus; a high indicates data is on the bus. Wait states extend the high state of SYNCN.

SYNCN cycles associated with internal CPU operations are either five or six OSC cycles in duration. Six OSC cycles are required for machine cycles associated with microcode branches or with the execution of internally (Interrupt Unit) decoded XIO commands. Five OSC cycles are used for all other internal operations, e.g., register to register transfers, ALU functions, etc.

[**NOTE:** For MAS281s operating at high OSC frequencies, the Interrupt Unit logic that creates IRDYN may cause a wait state to be inserted during execution of internal XIO commands. This would result in a SYNCN cycle of seven OSC cycles duration. Though unlikely, this condition must be taken into account in implementing a RDYN generation circuit. Refer to the description of the RDYN signal for further details].

3.2.3 IU Synchronisation Clock (SYNCLKN)

Output. The SYNCLKN signal is a logical equivalent of the SYNCN signal provided for Interrupt Unit synchronisation.

3.2.4 System Clock (SYSCLK1N)

Output. SYSCLK1N is the MA17501's synchronization clock. It is the logical equivalent of SYNCN and SYNCLKN with the exception that during PAUSEN low or during HLDAKN low, SYSCLK1N is held in its low state. SYSCLK1N, like SYNCLKN, has a VSS to VDD logic level swing.

3.2.5 Precharge Clock (CLKPCN)

Output. CLKPCN is used by the MA17502 Control Unit (CU) to synchronize the precharging of the internal M Bus and most other CU operations to the MAS281 machine cycle.

CLKPCN cycles associated with MAS281 external memory or I/O bus transactions are a minimum of five OSC cycles in duration and are extended when wait states are inserted via the RDYN input. CLKPCN low indicates that the internal CU M Bus is being precharged to the high state; the low-to-high transition places the lower 20 bits of a microinstruction on the external M Bus. Wait states extend the high state of CLKPCN. When PAUSEN or HLDAKN is low, CLKPCN is held low.

CLKPCN cycles associated with internal MAS281 operations are either five or six OSC cycles in duration. Six OSC cycles are required for machine cycles associated with microcode branches or with the execution of internally (Interrupt Unit) decoded XIO commands. Five OSC cycles are used for all other internal operations, e.g., register to register transfers, ALU functions, etc.

[**NOTE:** For MAS281s operating at high OSC frequencies, the Interrupt Unit logic that creates IRDYN may cause a wait state to be inserted during execution of internal XIO commands. This would result in a CLKPCN cycle of seven OSC cycles duration.]

3.2.6 Phase 2 Clock (CLK02N)

Output. CLK02N is used by the MA17502 Control Unit (CU) in conjunction with CLKPCN to synchronize microinstruction transmission on the M Bus to the MAS281 machine cycle.

CLK02N cycles associated with MAS281 external memory or I/O bus transactions are a minimum of five OSC cycles in duration and are extended when wait states are inserted via the RDYN input.

The high-to-low transition of CLK02N places the upper 20 bits of a microinstruction on the external M Bus. Wait states extend the trailing (based on SYNCN high-to-low beginning the machine cycle) low state of CLK02N. When PAUSEN or HLDAKN is low, CLK02N is held high.

CLK02N cycles associated with internal MAS281 operations are either five or six OSC cycles in duration. Six OSC cycles are required for machine cycles associated with microcode branches or with the execution of internally (Interrupt Unit) decoded XIO commands. Five OSC cycles are used for all other internal operations, e.g., register to register transfers, ALU functions, etc.

[**NOTE:** For MAS281s operating at high OSC frequencies, the Interrupt Unit logic that creates IRDYN may cause a wait state to be inserted during execution of internal XIO commands. This would result in a CLK02N cycle of seven OSC cycles duration.]

3.3 Bus Control

This group of signals is provided to control Address/Data (AD) bus transmissions (See Figure 4). The signals indicate when address or data information is on the AD Bus and what type of transaction is taking place during a particular machine cycle.

3.3.1 Address Strobe (AS)

Output/Hi-Z. AS high indicates that the Address/Data (AD) Bus contains address information. The address information is assured stable at the high-to-low transition of this signal. In this way, AS provides the necessary control for a system Address Bus transparent latch system interface.

The Interrupt Unit uses AS to extract the XIO command information off the AD Bus for internally decoded XIO commands, and the Memory Management Unit/Block Protection Unit (MMU(BPU)) uses AS to extract address information for memory management and block protection functions, and to extract XIO command information for MMU(BPU) decoded XIO commands.

AS is placed in the high-impedance state during DMA cycles by PAUSEN low and during the Hold state by HLDAKN low. During internal non-AD Bus related CPU operations, AS is held low for the entire machine cycle via microcode control.

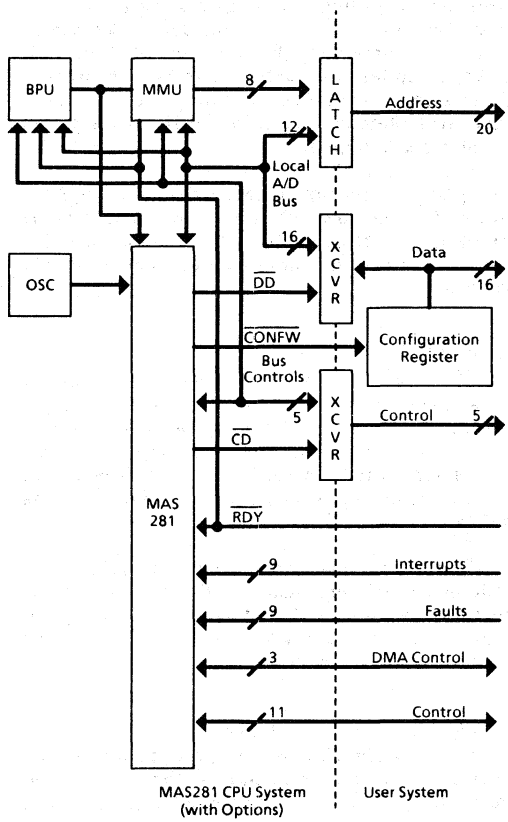


Figure 4. Typical MAS281/MA17504 System Interface

3.3.2 Data Strobe (DSN)

Output/Hi-Z. DSN low indicates that data is on the AD Bus (write/output cycles) or that the MAS281 AD Bus drivers are in the high-impedance state (read/input cycles). For write/output cycles, the data is guaranteed stable at the low-to-high transition of DSN. For read/input cycles, the DSN low-to-high transition indicates the acceptance of data by the MAS281 (SYSCLK1N high-to-low transition latches AD Bus data into the IA and DI registers).

DSN is placed in the high-impedance state during DMA cycles by PAUSEN low and during the Hold state by HLDAKN low. DSN is held high, for the entire machine cycle, during internal non-AD Bus operations via microcode.

3.3.3 Read/Write (RD/WN)

Output/Hi-Z. RD/WN defines the direction of data flow on the bidirectional AD Bus and provides read/write cycle information to the MMU(BPU) for write protection control. RD/WN high indicates a read/input bus cycle and data transfer to the MAS281. RD/WN low indicates a write/output bus cycle and data transfer from the MAS281.

This signal is asserted at the SYNCN high-to-low transition and remains valid for the duration of the current SYNCN period. RD/WN is placed in the high-impedance state during DMA cycles by PAUSEN low and during the Hold state by HLDAKN low.

3.3.4 Memory/Input-Output (M/ION)

Output/Hi-Z. M/ION defines the type of device involved in the data transfer occurring on the AD Bus and provides functional control for the Interrupt Unit (IU) and the Memory Management Unit/Block Protection Unit (MMU(BPU)). The IU ignores memory transfer AD Bus activity and the MMU(BPU) uses M/ION to decide whether to decode the address information on the AD Bus as an MMU(BPU) XIO command or a memory address. M/ION high indicates a memory access, and M/ION low indicates an input-output operation.

This signal is asserted at the SYNCN high-to-low transition and remains valid for the duration of the current SYNCN period. M/ION is placed in the high impedance state during DMA cycles by PAUSEN low and during the Hold state by HLDAKN low. M/ION is raised high, for the entire machine cycle, during internal non-AD Bus operations via microcode.

3.3.5 Instruction/Operand (IN/OPN)

Output/Hi-Z. IN/OPN high indicates an instruction is to be read from memory during the current AD Bus cycle. IN/OPN is low for all other MAS281 directed AD Bus transfers. The Memory Management Unit/Block Protection Unit (MMU(BPU)), when configured as a MMU, uses IN/OPN to select the proper page register set within the specified page register group.

IN/OPN is asserted at the SYNCN high-to-low transition and remains valid for the duration of the current SYNCN period. IN/OPN is placed in the high-impedance state during DMA cycles by PAUSEN low and during the Hold state by HLDAKN low.

3.3.6 Ready (RDYN)

Input. During external AD Bus transfers (those dealing with devices external to the MAS281 chip set), a low is required on this input to allow the MAS281 machine cycle to complete (high-to-low transition of SYNCN). RDYN high is used to prolong the data portion of the machine cycle (SYNCN high) to accommodate slow memory and I/O devices. The MAS281 assumes memory or I/O devices are NOT ready to provide (accept) data to (from) the AD Bus, and requires these devices to signal their readiness via the RDYN input.

A low on RDYN, enveloping the current machine cycle's fifth (or later) OSC cycle high-to-low transition, allows the current machine cycle to complete (SYNCN high-to-low transition) at the following low-to-high transition of the OSC input.

3.4 Buses

The following is a discussion of the communication buses connecting the MA17501 to the other chips of the MAS281 set. The AD Bus transfers all data and instructions and the M Bus provides the microcode instructions from the MA17502.

3.4.1 Address/Data Bus (AD Bus)

Input/Output/Hi-Z. These signals comprise a 16- bit bidirectional multiplexed address and data bus. During external bus transfers, the AD Bus accommodates the transfer of address and data information between the MA17501 and memory, or I/O ports. During internal bus operations, the AD Bus provides additional communication among the Execution, Control, Interrupt and Memory Management/Block Protection Units. AD00 is the most significant bit position and AD15 is the least significant bit position of both the 16-bit data and 16-bit address. A high on this bus corresponds to a logic one and a low corresponds to a logic zero.

Address information is valid on the bus at the AS high-to-low transition. The RD/WN signal indicates the MA17501 AD Bus driver's state during the data portion of the bus cycle (DSN low) and the M/ION function defines the type of device the transfer is with. The AD Bus drivers are placed in the high impedance state during Read operations (DSN low), during DMA cycles by PAUSEN low, and during the Hold state by HLDAKN low.

3.4.2 Microcontrol Bus (M Bus)

Input. The M Bus is a 20-bit multiplexed microcontrol bus which provides microcoded control to the EU. The Control Unit multiplexes the 40-bit microcode instructions into two 20-bit words. The upper 20 bits are placed on the M Bus by the CLKPCN low-to-high transition and the lower 20 bits are placed on the M Bus by the trailing high-to-low transition of CLK02N. The microinstruction is reassembled in the EU's Execution (E) register and used to control EU functions during the next machine cycle. M19 is the most significant bit position and M00 is the least significant bit position for both microwords. The high order 20 bits are transmitted first, followed by the low order 20 bits of the microinstruction. A high on this bus corresponds to a logic one and low corresponds to a logic zero.

3.5 System Support Interface

The system support interface signals have control over functions that affect the chip set as a whole.

2

3.5.1 Processor Pause (PAUSEN)

Input. PAUSEN is driven low by the Interrupt Unit upon acknowledgement of a DMA transfer request. A low on PAUSEN causes the EU to place all the bus control signals (AS, DSN, M/ION, RD/WN, IN/OPN) and the AD Bus in the high impedance state, and to disable all clock outputs, except for SYNCLKN and SYNCN The requesting device maintains control of the AD Bus and bus control lines until (IU)DMARN is raised high, thus causing PAUSEN to raise high.

It is recommended that the MAS281 chip set be buffered to the memory/input-output system. If an MMU(BPU) peripheral chip is used for memory expansion/protection it must reside on the MAS281 side of these buffer transceivers (see Figure 4). Thus, for a DMA device to access the MMU(BPU), the MAS281 AD Bus and bus control signal drivers must be in the high impedance state to allow the DMA device to drive these signals. The Interrupt Unit also provides the CDN signal for the directional control of the bus control transceivers.

3.5.2 Processor Hold Request (HOLDN)

Input. A low on this input suspends all chip set functions (except SYNCN and SYNCLKN) at the end of the current MIL-STD-1750A instruction. The AD Bus and bus control functions (AS, DSN, M/ION, IN/OPN, RD/WN) are placed in the high impedance state permitting a monitor system to take control of the memory/input-output system. The internal synchronization clocks are placed in an inactive state, which halts further instruction sequencing until HOLDN is released. As with DMA cycles, the reason for this is to allow access to the MMU(BPU) if an expanded memory system is used. The (IU)CDN output is provided for control bus transceiver directional control during the Hold state.

3.5.3 Processor Hold Acknowledge (HLDAKN)

Output. HLDAKN drops low after reaching the end of the MIL-STD-1750A instruction during which HOLDN was pulled low, or after encountering a BPT software instruction. The Hold state is terminated by raising HOLDN high (if HOLDN low initiated the Hold state), or by pulsing HOLDN low (if the Hold state was initiated by a BPT instruction). During the Hold state, software execution is suspended and the MAS281 interface functions are placed in the high impedance state to allow a monitor system to take control of the memory/input-output system.

3.6 Inter-Chip Control

The following signals perform control functions internal to the MAS281 chip set. These functions include microcode execution branching control and arithmetic error indication.

3.6 1 Internal Ready (IRDYN)

Input. The IRDYN signal is the means by which Interrupt Unit (IU) command cycles, involving the AD Bus, are completed. The IU drops IRDYN low when the XIO command has been decoded and allows the six OSC period machine cycle to complete. The IRDYN and RDYN signals are effectively ORed together to control the EU clock generation circuitry; therefore, RDYN should be high during IU decoded XIO commands.

3.6.2 Interrupt Unit Microinstruction Enable (INTREN)

Output. The Execution Unit controls the Interrupt Unit (IU) 3-bit microcode interface through the use of the INTREN signal. INTREN low enables the IU microcode decoding logic. IU functions handled through microcode are; enable/disable DMA interface XIO command control, set Normal Power-Up discrete, load fault register, and read encoded 4-bit vector identifying the highest priority pending interrupt.

Machine cycles during INTREN low are a special case of internal non-AD Bus operations. These cycles are denoted by a six OSC period machine cycle.

3.6.3 Overflow Indicator (OVIN)

Output. OVIN is an indication that a fixed- point overflow condition, as specified in MIL-STD-1750A, has occurred during an operation. The Interrupt Unit accepts this as an input to the pending interrupt register level four interrupt bit.

3.6.4 Privileged Instruction Fault (PIFN)

Input. PIFN low is an indication to the Execution Unit that a fault, requiring the current MIL-STD-1750A instruction to be aborted, has occurred. The faults that cause the instruction abort are 0, 5, and 8 which are, respectively, memory protect error ((IU)MPROEN low), an out-of-bounds memory/input-output address ((IU)EXADE low), or a bus fault timeout. In response to PIFN low, the EU maintains AS low, DSN high, and forces the M/ION signal high for two machine cycles. In addition, the EU will internally complete the current SYNCN cycle and resume operation. This allows the Control Unit to sequence to the interrupt handling routine without affecting the bus status.

3.6.5 Branch or Jump Control (T1)

Output. The Execution Unit raises the T1 signal high to indicate a microcode conditional branch condition is true. The Control Unit accepts T1 and feeds it into the microcode address multiplexer where microinstruction branches are effected.

3.6.6 Test Microword (TESTN)

Input. The TESTN signal is used during chip test to load 40-bit microinstructions into the EU execution register. TESTN low loads E39 (MSB) to E20, and TESTN high loads E19 to E00 (LSB). TESTN should be pulled-up to VDD in customer applications.

4.0 Operating Modes

The following discussions detail the MAS281 chip set operating modes from the perspective of the Execution Unit. MAS281 operating modes involving the MA17501 include: (1) Initialization, (2) Instruction Execution, (3) Interrupt Servicing, (4) Fault Servicing, (5) DMA Support, and (6) Software Development Support.

4.1 Initialisation

RESET starts the chip set microcoded initialisation sequence, but also affects the Execution Unit Circuitry directly. When RESET is raised high, the Hold state acknowledge signal (HLDAKN) is forced high thus releasing the MAS281 from the Hold state (if changing HOLDN is unable to release the Hold state). RESET also forces the clock generation circuitry to create a five OSC period machine cycle by disabling state machine inputs that vary the machine cycle length.

Upon releasing RESET, the EU Hold State circuitry is enabled and the clock generation circuitry is allowed to function normally. HOLDN will not have an effect on chip set operation until the initialisation routine has completed because the microcode branch to the Hold routine is disabled.

The microcoded initialisation routine clears the Instruction Counter (IC), Status Word Register (SW), and Register File (R00-R15) and performs the BIT. The successful completion of the BIT is necessary to guarantee the register file is cleared at the end of the initialisation routine.

The microcoded BIT exercises all legal microinstruction bit combinations and tests all internally accessible structures of the MAS281. For the Execution Unit this includes the full Register Set, ALU, Multiplier, Barrel Shifter, and Macroflag logic. Table 2 details the tests performed by each of the five BIT subroutines.

If any part of BIT fails, an error code identifying the failed subroutine is loaded into the Interrupt Unit Fault Register (via the AD Bus), BIT is aborted, and NPU is left in the low state. Table 2 defines the coding of the BIT results. (INTREN enables microcode control of the Interrupt Unit (IU) to raise NPU high (if BIT passes) and load BIT error codes (if BIT fails) into the IU Fault Register).

BIT	Test Coverage	BIT Fail Codes ($FT_{13, 14, 15}$)	Cycles
1	Microcode Sequencer IB Register Control Barrel Shifter Byte Operations and Flags	100	221
2	Temporary Registers (T0 - T7) Microcode Flags Multiply Divide	101	166
3	Interrupt Unit - MK, PI, FT Enable/Disable Interrupts	111	214
4	Status Word Control User Flags General Registers (R0 - R15)	110	154
5	Timer A Timer B	111	763
–	BIT Pass/Fail Overhead	–	26

Note: BIT pass is indicated by all zeros in FT bits 13, 14, and 15

Table 2. MAS281 BIT Summary

The last action performed by the initialisation routine is to load the instruction pipeline. Instruction fetches start at memory location zero (page zero) from the Start-Up ROM (if implemented). Whether or not BIT passes, the processor will begin instruction execution at this point.

[NOTE: To complete initialisation and pass BIT, interrupt and fault inputs must be high for the duration of the initialisation routine. Also, the Timers A and B must be clocked for BIT success.]

4.2 Instruction Execution

Instruction execution is characterized by a variety of operations composed of various types of machine cycles. The Execution Unit contains the clock generation circuitry that creates the different machine cycles depending on the particular operation being performed at the time. These operations include: (1) internal CPU cycles, (2) instruction fetches, (3) operand transfers, and (4) input/output transfers. Instruction execution may be interrupted at the end of any individual machine cycle by the PAUSEN (denoting DMA operations) clock generation circuitry input, and at the beginning of any given MIL-STD-1750A instruction by an (IU)IRN or HOLDN low input to the Control Unit.

4.2.1 Internal CPU Cycles

All CPU data manipulation and housekeeping operations are performed using internal CPU cycles. Internal CPU cycles are either five or six OSC periods long and are characterized by AS low and DSN, (IU)DDN, and M/ION high. Section 5.0 provides timing characteristics for internal CPU cycles.

The majority of Internal CPU Cycles are five OSC period machine cycles. Six OSC period machine cycles occur when executing conditional jump or branch microinstructions; the EU is calculating the branch condition to determine the state of the T1 output signal.

4.2.2 Instruction Fetches

Instruction fetches are used to keep the instruction pipeline full. This ensures that the next instruction is ready for execution when the preceding instruction is completed.

During jump and branch instruction execution the pipeline is flushed, then refilled via two consecutive instruction fetches starting at the new instruction location. The pipeline is also refilled as part of the interrupt and Hold processing.

Instruction fetches are five (minimum) OSC period machine cycles characterised by IN/OPN, M/ION, and RD/WN high. Instruction fetches use pipeline registers IA and IB, the instruction counter (IC), and the data input register (DI). Assuming an empty instruction pipeline (as a result of a reset, jump or branch), the contents of IC are placed on the AD Bus as an address. The returned value (the instruction) is stored in the IA register. The IC register is incremented (dedicated counter mode) and the next fetch is performed.

This second returned value, which may be an instruction or an immediate operand, is stored in both the IA and DI registers as the previous contents of IA advance to the IB register to be decoded into their microcoded routine. If the second returned value is an immediate operand, a third instruction fetch will occur with the instruction being loaded into IA only; DI retains the immediate operand.

The data portion (SYNCN high) of instruction fetch cycles can be extended beyond their minimum five OSC periods by use of the RDYN signal. RDYN held high during the high-to-low transition of the machine cycle's fifth OSC cycle will extend the data portion of the machine cycle. The machine cycle can be completed at any succeeding OSC cycle high-to-low transition by enveloping this OSC edge with RDYN low.

4.2.3 Operand Transfers

Operand transfers are used to obtain operands to be used by an instruction and to save any results of an instruction's execution. Machine cycles associated with operand transfers are a minimum of five OSC periods in duration. The RDYN signal can be used to insert wait states into the data portion of the machine cycle (SYNCN high) to accommodate slow memory.

Operand transfers use the address register (A), data input register (DI), and data output register (DO). Before the operand transfer begins, the Execution Unit calculates the effective operand address and stores this value in A.

For write transfers the EU loads the operand into DO. For operand ready cycles the EU latches the operand from the AD Bus into DI at the SYSCLK1N high-to-low transition.

All operand transfers between the MAS281 and memory are referenced to the AS and DSN bus control signals and are characterized by IN/OPN low, M/ION and CDN high, and RD/WN (high, read; low, write).

The EU first places the contents of A on the AD Bus at the SYSCLK1N high-to-low transition. Shortly following, AS is raised high to enable the system address bus transparent latch. This address is assured valid at the high-to-low transition of AS. At the SYSCLK1N low-to-high transition, DSN drops low to indicate the contents of DO have been placed on the AD Bus (write) or the EU AD Bus drivers have been placed in the high impedance state (read).

DSN subsequently raises high when the output data is stable, prior to SYSCLK1N dropping low, or raises high in response to SYSCLK1N dropping low to indicate the EU's acceptance of the input data.

All operand transfer cycles are allowed to complete via the RDYN input. During the data portion of the cycle the EU assumes memory is NOT READY, and requires RDYN low to signal the memory's readiness to complete the cycle. If RDYN is high at the high-to-low transition of the fifth OSC cycle within the operand transfer cycle, a wait state will be injected (one OSC period at a time) for each OSC high-to-low transition that RDYN remains high. Memory readiness, thus cycle completion, is signalled by RDYN low enveloping a subsequent OSC high-to-low transition.

4.2.4 Input/Output Transfers

Input/Output transfers are characterized by M/ION and IN/OPN low, and RD/WN (high, input; low, output). AS and DSN operate as during operand transfers. Two different types of input/output transfers are controlled by the Execution Unit: internal and external.

Internal I/O transfers involve all XIO commands that are decoded by the Interrupt Unit (IU) and use the local AD Bus to transfer response data. These commands are listed in Table 3 (the only exception is RCW; it is an IU decoded, IRDYN completed, External I/O command). Internal XIO commands implemented in the IU (per Table 3) use a six OSC period machine cycle and the IRDYN cycle completion input. Internal XIO commands implemented in the MA17504 MMU(BPU) use a minimum five OSC period machine cycle and the MMU(BPU) provides the RDYN cycle completion input to the EU.

The term "local AD Bus" in this context refers to the AD Bus on the processor side of the system data bus demultiplexing transceivers. The three chips of the MAS281 and the MA17504 (in either configuration) reside on the local AD Bus and communicate to the user system through the required address and data bus buffers, as depicted in Figure 4.

External I/O transfers involve all XIO and VIO instructions not included under Internal I/O transfers. They execute during a minimum five OSC period machine cycle that is extendable via RDYN, as previously described.

4.3 Interrupt Servicing

Interrupts are latched into the Interrupt Unit (IU) pending interrupt register by the SYNCLKN high-to-low transition. The IU signals the Control Unit (CU) that an interrupt is pending and the CU branches to the microcoded interrupt handling routine at the completion of the currently executing MIL-STD-1750A instruction.

The EU supports the interrupt handling routine by enabling microcode control of the IU at the proper time via the INTREN signal and by calculating the memory addresses of the service and linkage pointers based on the 4-bit interrupt priority code transmitted by the IU. Machine cycles during which INTREN is low are six OSC periods in length. During these INTREN cycles, DSN and M/ION are high, and AS is low.

The EU also provides a hardwired interrupt to the IU. The OVIN interrupt signals a fixed-point arithmetic overflow.

4.4 Fault Servicing

The Interrupt Unit (IU) latches fault inputs into the fault register on the high-to-low transition of SYNCLKN. Faults other than 0, 5, and 8 latch a level one pending interrupt in the IU and the interrupt sequencing proceeds as previously explained. Faults 0, 5, and 8 caused during non-DMA AD Bus transactions demand more immediate attention; the MIL-STD-1750A instruction during which the fault occurred must be aborted.

PIFN indicates to the Control Unit that one of these faults has occurred and forces a branch to the "next instruction fetch" microinstruction so that the interrupt caused by the PIFN fault can be serviced immediately. Under normal instruction execution circumstances, the bus control signals would operate during the machine cycle between the fault and the instruction fetch machine cycle. PIFN causes the bus control signals AS and DSN to stay in their inactive state during this transitional machine cycle to allow the branch to the microcoded interrupt routine without performing any AD Bus transactions.

4.5 Direct Memory Access

The Interrupt Unit DMA interface logic signals the Execution Unit (EU) that it has acknowledged a DMA request (PAUSEN low). PAUSEN low causes the EU to halt the synchronization clocks CLK02N (high), CLKPCN (low), and SYSCLK1N (low); disables clock generation circuitry input that could vary the machine cycle length; and places all bus control signals and the AD Bus in the high impedance state. The SYNCN and SYNCLKN clocks continue to operate with a five OSC cycle period. Upon removal of PAUSEN by the Interrupt Unit, the MAS281 resumes microinstruction execution where it was interrupted.

4.6 Software Development Support

The Execution Unit responds to a HOLDN signal by suspending all internal operations upon completion of the currently executing instruction. Microcode, from the Control Unit, directs HLDAKN low during the third SYNCN cycle after HOLDN has been pulled low and the previous instruction has been completed. M/ION, RD/WN, IN/OPN, AS, DSN, and the AD Bus are placed in the high impedance state permitting a monitor system to take control of the memory/input-output system. Raising HOLDN releases the MAS281 from the Hold state and instruction execution begins by refilling the pipeline.

The execution of a BPT instruction also causes HLDAKN to drop low and the bus control signals and AD Bus to be placed in the high impedance state. A low pulse on HOLDN releases the MAS281 from the BPT initiated Hold state.

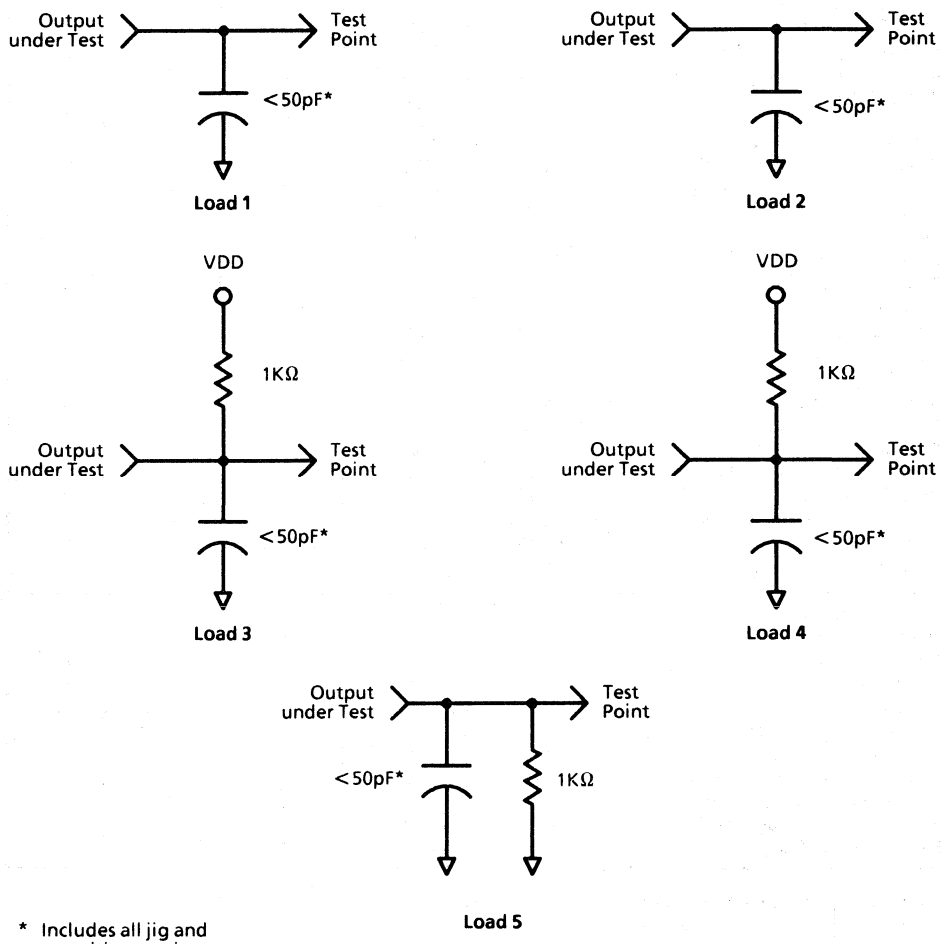
Operation	Command Code (Hex)	Mnemonic	Cycles*		
			M	P	B
Implemented in MAS281					
Set Fault Register	0401	SFR	2	3	9
Set Interrupt Mask	2000	SMK	2	3	9
Clear Interrupt Request	2001	CLIR	2	3	9
Enable Interrupts	2002	ENBL	2	3	9
Disable Interrupts	2003	DSBL	2	3	9
Reset Pending Interrupt	2004	RPI	2	3	9
Set Pending Interrupt Register	2005	SPI	2	3	9
Reset Normal Power Up Discrete	200A	RNS	2	3	9
Write Status Word	200E	WSW	2	3a	8.5a
Enable Start-Up ROM	4004	ESUR	2	3	9
Disable Start-up ROM	4005	DSUR	2	3	9
Direct Memory Access Enable	4006	DMAE	2	3	9
Direct Memory Access Disable	4007	DMAD	2	3	9
Timer A Start	4008	TAS	2	3	9
Timer A Halt	4009	TAH	2	3	9
Output Timer A	400A	OTA	2	3	9
Reset Trigger-Go	400B	GO	2	3	9
Timer B Start	400C	TBS	2	3	9
Timer B Halt	400D	TBH	2	3	9
Output Timer B	400E	OTB	2	3	9
Read Configuration Word	8400	RCW	2	2	4
Read Fault Register without Clear	8401	RFR	2	2	4
Read Interrupt Mask	A000	RMK	2	2	4
Read Pending Interrupt Register	A004	RPIR	2	2	4
Read Status Word	A00E	RSW	2	1	4
Read and Clear Fault Register	A00F	RCFR	2	2	4
Input Timer A	C00A	ITA	2	2	4
Input Timer B	C00E	ITB	2	2	4
Implemented in BPU					
Memory Protect Enable	4003	MPEN	2	4	8
Load Memory Protect RAM	50XX	LMP	2	4	8
Read Memory Protect RAM	D0XX	RMP	2	3	3
Implemented in MMU					
Write Instruction Page Register	51XY	WIPR	2	4	8
Write Operand Page Register	52XY	WOPR	2	4	8
Read Memory Fault Status	A00D	RMFS	2	3	3
Read Instruction Page Register	D1XY	RIPR	2	3	3
Read Operand Page Register	D2XY	ROPR	2	3	3

* M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles),
a = average if more than one alternative exists

Table 3. Internal I/O Command Summary

5.0 Timing Characteristics

This section provides the detailed timing specifications for the MA17501. Figure 5 depicts the test loads used to obtain timing data. Figures 6 through 20 depict the timing waveforms associated with various MA17501 signals. Table 5 provides values for parameters specified in the timing waveforms. All timing values provided in Table 5 are valid over the full military temperature range (-55°C to + 125°C), and are measured from 50% point to 50% point (50% VDD supply voltage, unless otherwise specified). Crosshatching in Figures 6 through 20 indicates either a "don't care" or indeterminate state.



* Includes all jig and parasitic capacitance

Figure 5. Test Loads

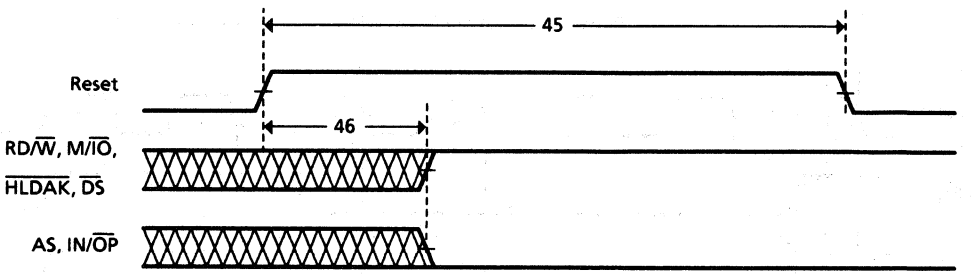


Figure 6. Reset Timing

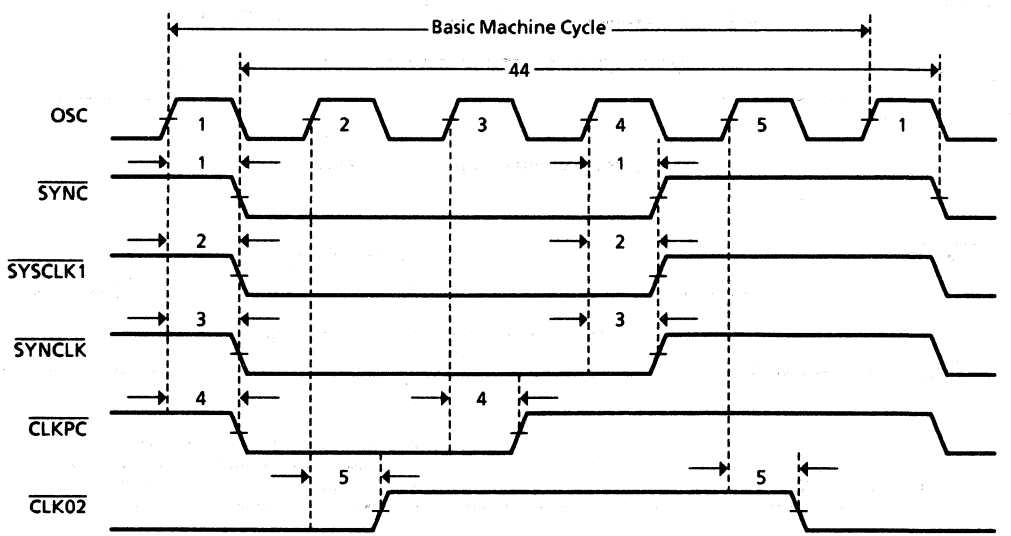


Figure 7. Basic Clock Timing

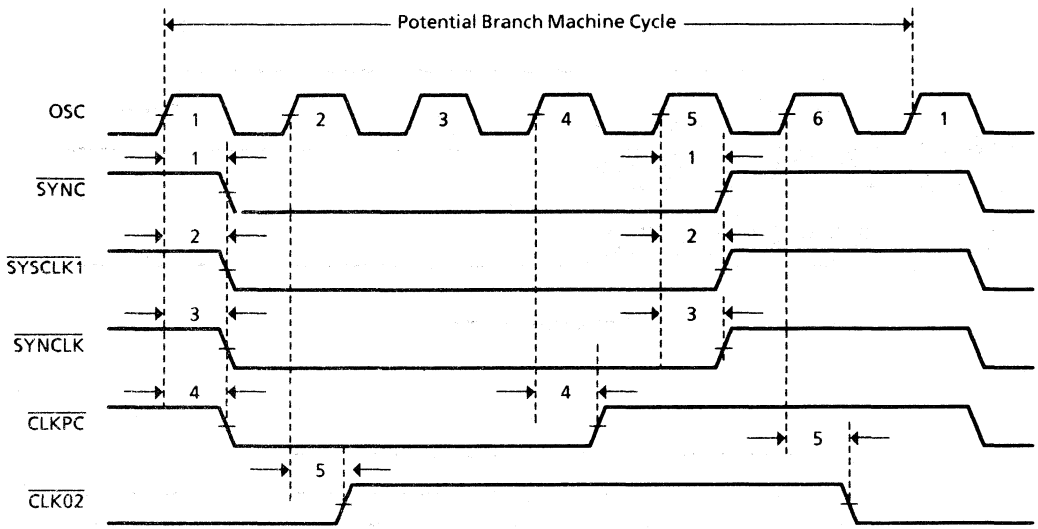


Figure 8. Potential Branch Clock Timing

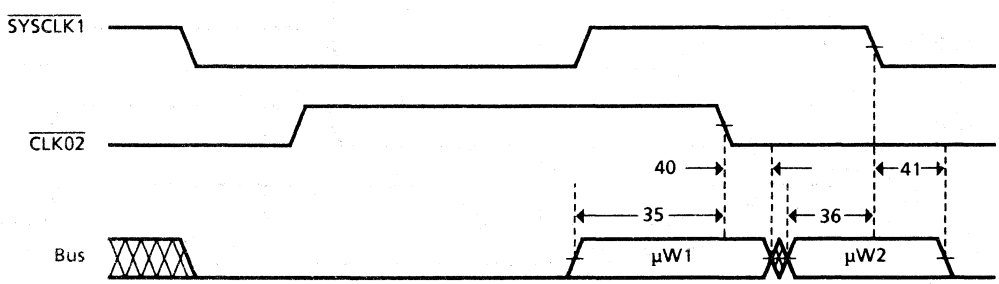
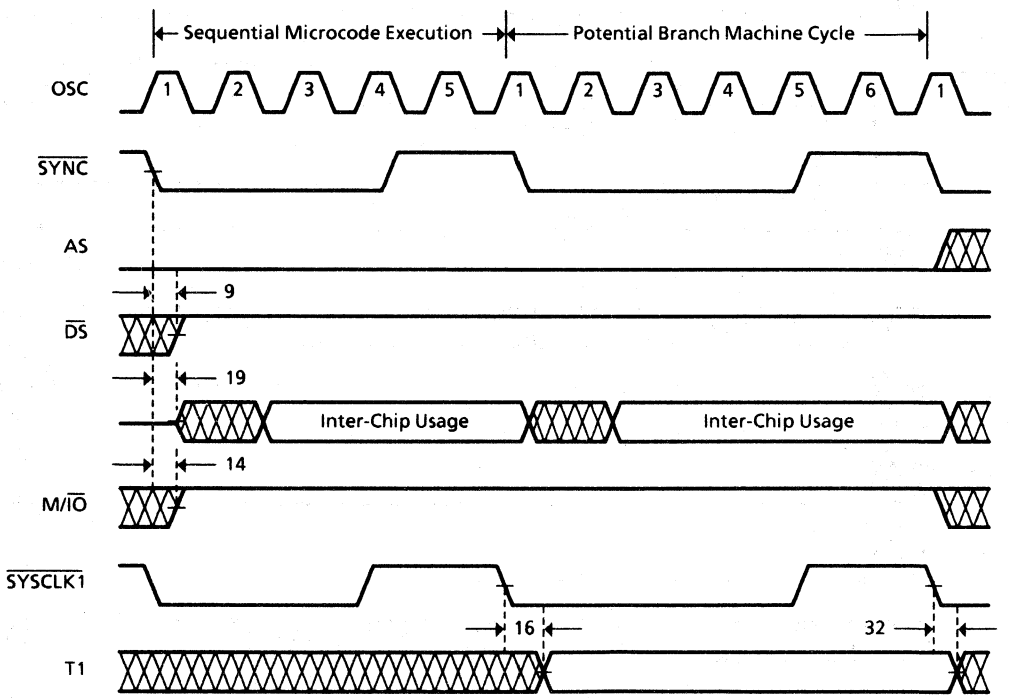
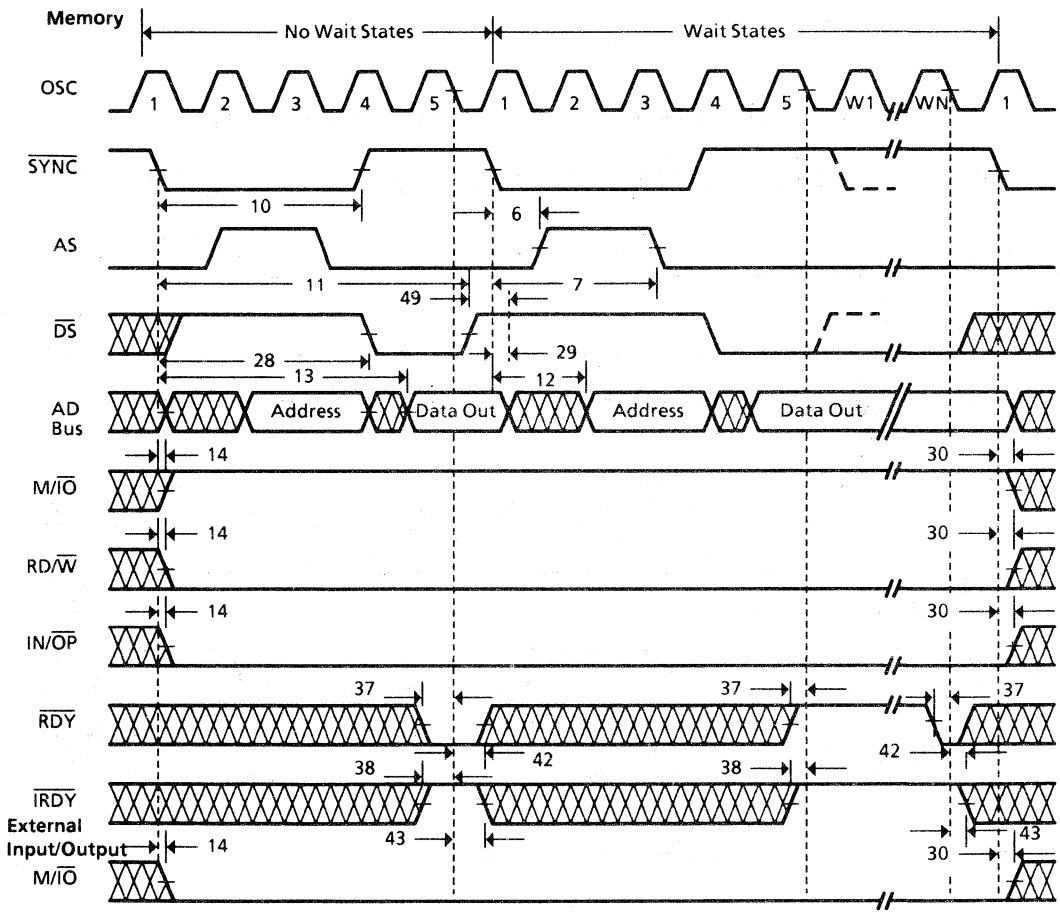


Figure 9. Microcode Bus Timing



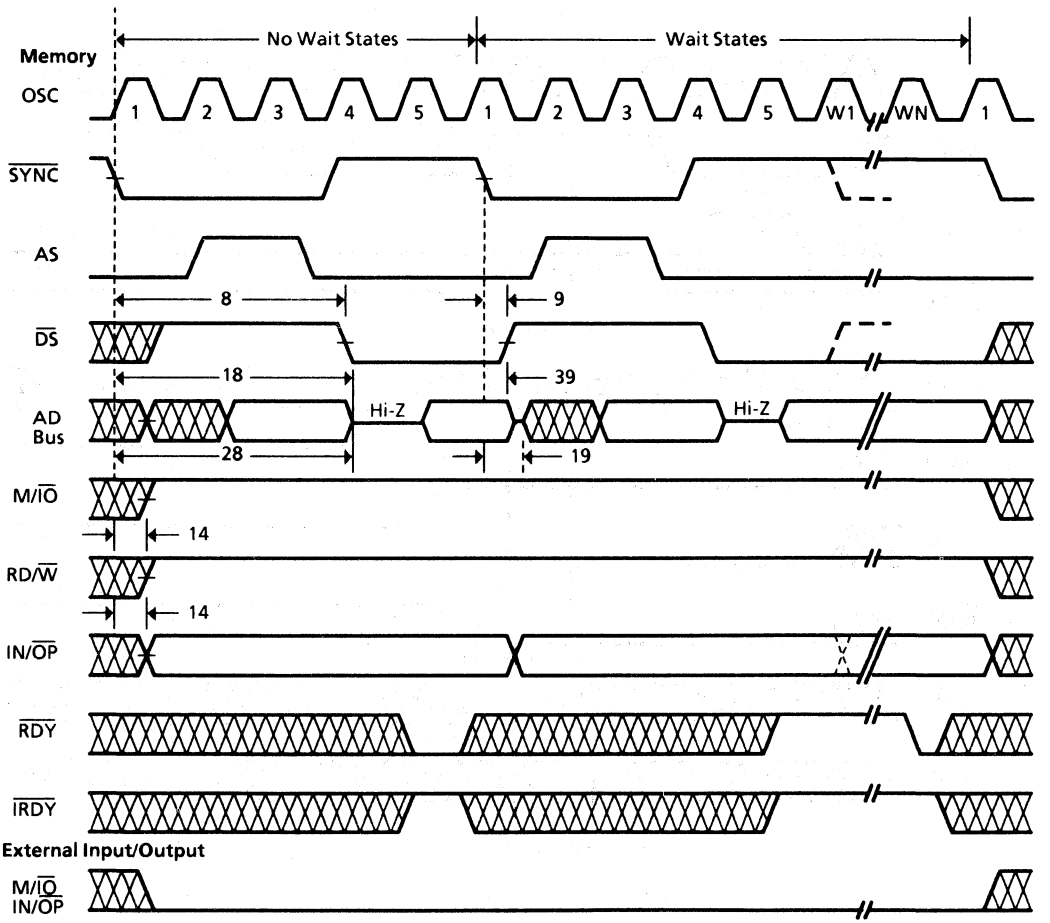
Note $\overline{RDY}$ is a "don't care" during internal CPU operations

Figure 10. Internal Processor Cycle



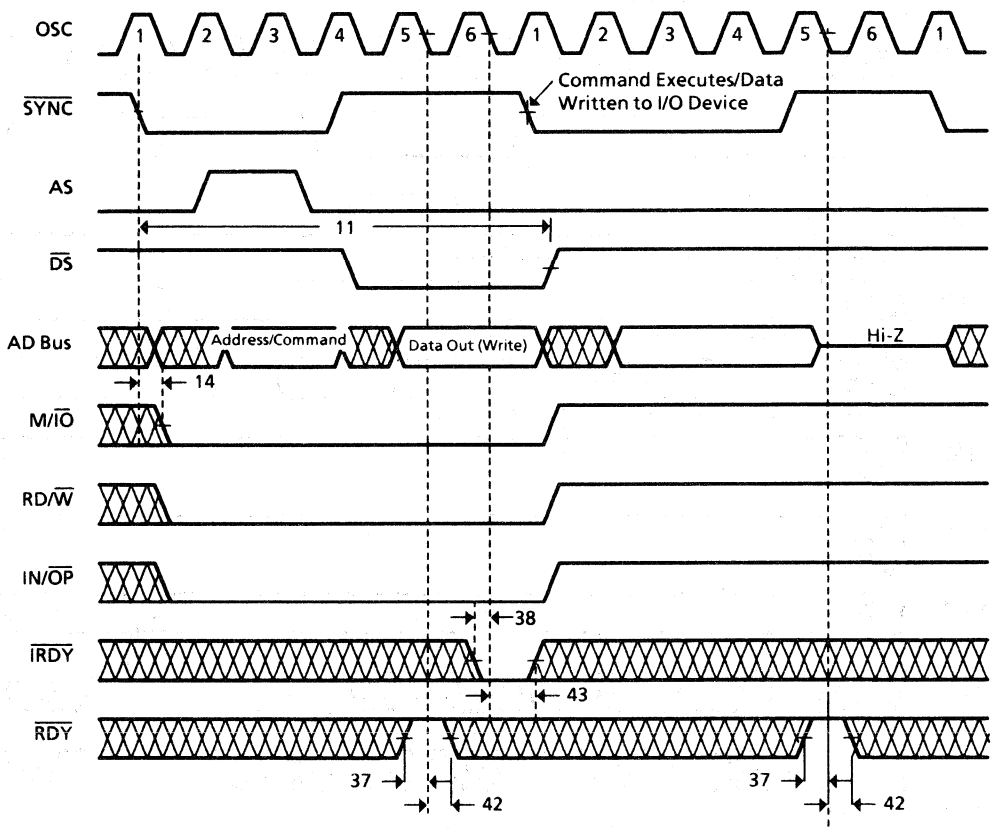
Notes
1 Dashed timing lines indicate non-wait cycle timing
2 Other output states
HLDAK = high
PAUSE = high
3 Other required input states
HOLD = high
DMAR = high
RESET = low

Figure 11. Write Transfer Timing



Notes
1 Dashed timing lines indicate non-wait cycle timing
2 Other output states
HLDAK = high
PAUSE = high
3 Other required input states
HOLD = high
DMAR = high
RESET = low

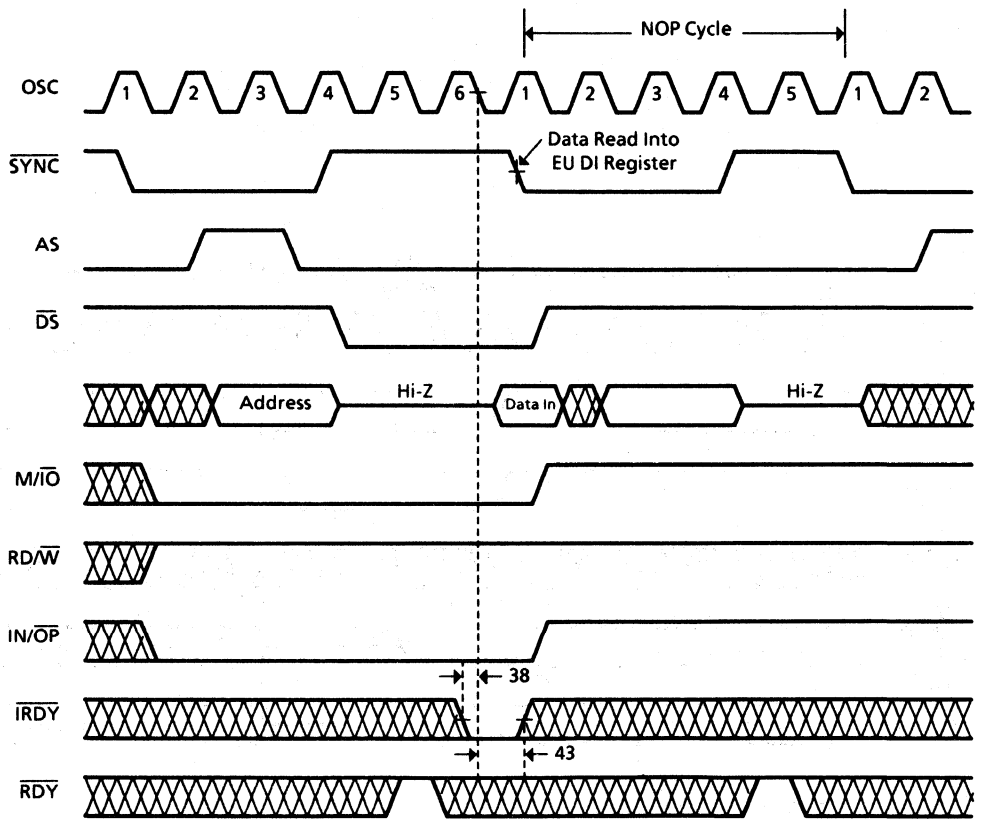
Figure 12. Read Transfer Timing



Notes:

1. Other output states:
   HLDAK = high
   PAUSE = low
2. Other required input states:
   HOLD = high
   DMAR = high
   RESET = low

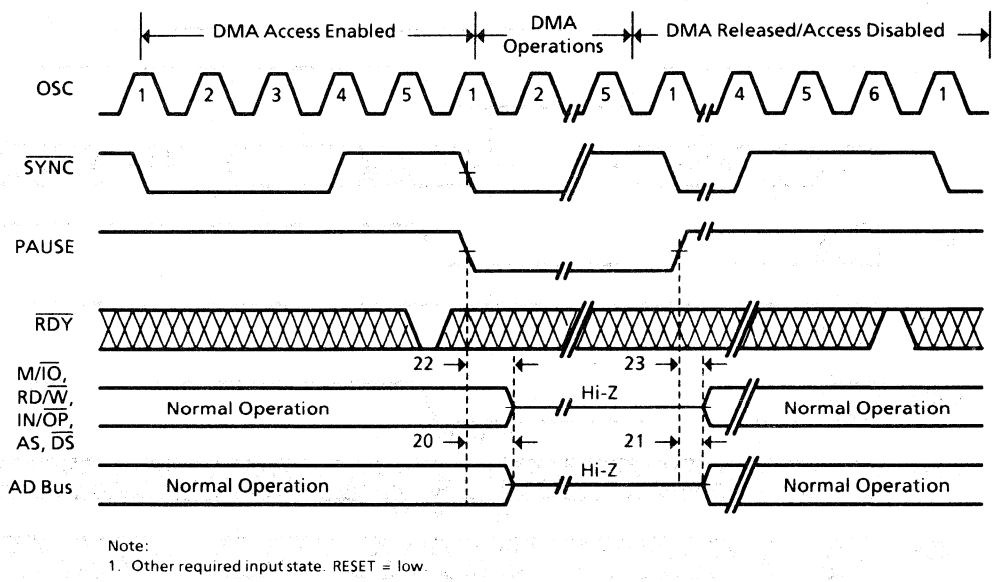
Figure 13. Internal I/O Timing - Write/Command



Notes:

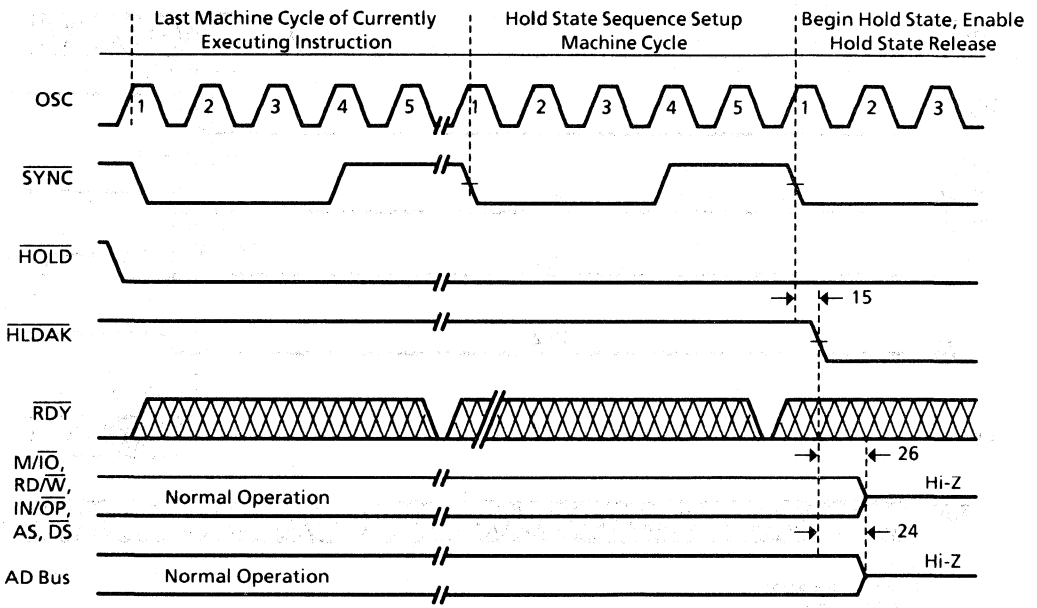
1. Other output states:
   - CD = high
   - HLDAK = high
   - PAUSE = low
2. Other required input states:
   - HOLD = high
   - DMAR = high
   - RESET = low

Figure 14. Internal I/O Timing - Read



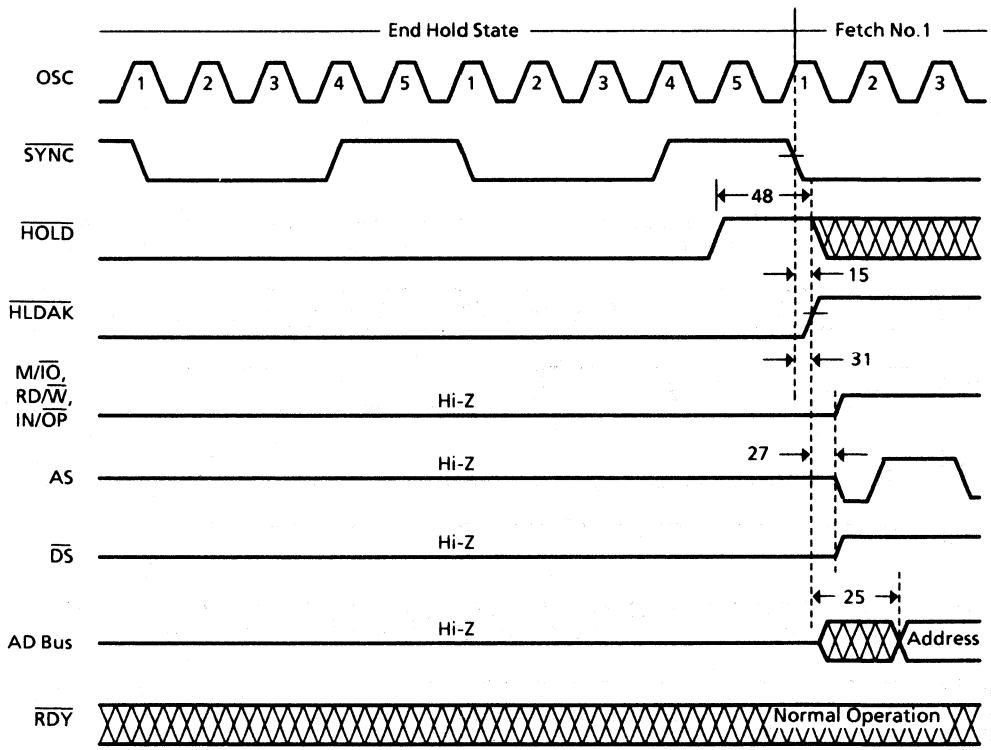
Note:
1. Other required input state. RESET = low.

Figure 15. DMA Access/Release Timing



Notes:
1. The 'don't care' state will contine to exist until HLDAK = high. RDY will then resume normal operation.
2. HOLD ↓ may occur at any time during software execution. The diagram shows the last possible time it can occur and be assured of entering the Hold state after the current instruction completes execution.
3. Other required input state. RESET = low.

Figure 16. Hold State Generation Timing



Note:
1. Other required input:
   RESET = low

Figure 17. Hold State Termination Timing

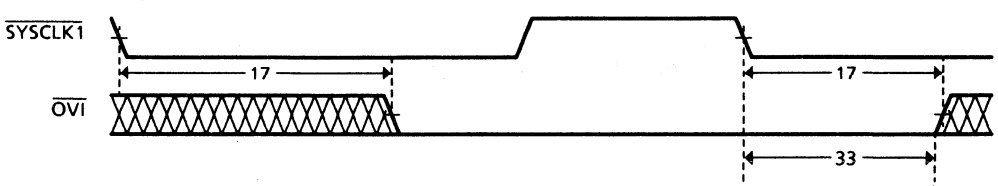


Figure 18. Fixed-Point Overflow Timing

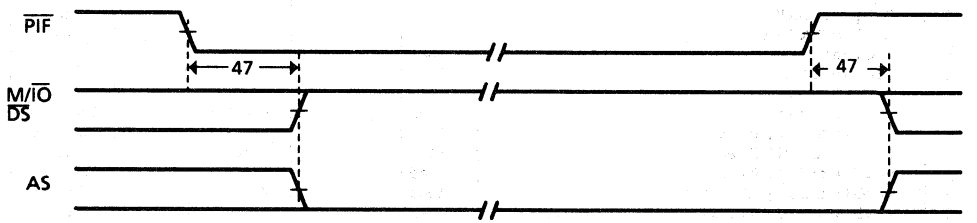


Figure 19. Instruction Abort Fault Timing

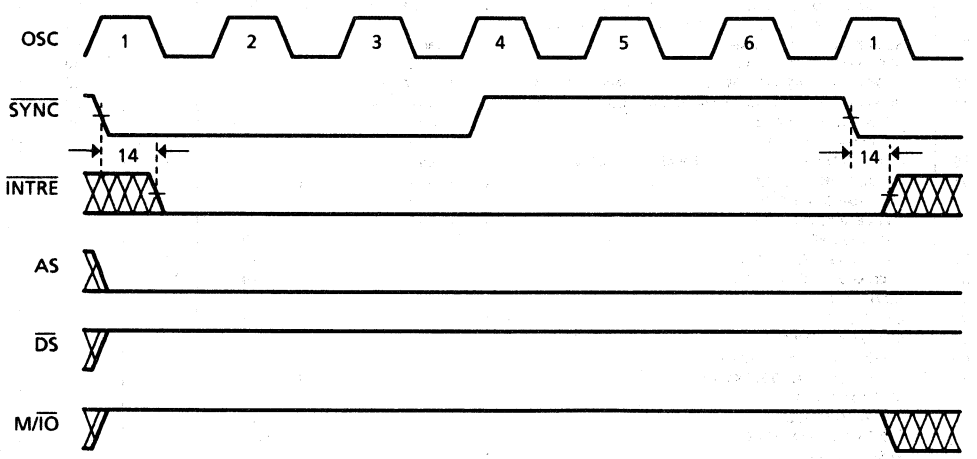


Figure 20. Interrupt Unit Microcode Enable Timing

No.	Parameter	Test Condition[1][5]	Min[2]	Typ[2]	Max[2]	Units
1	OSC ↑ to SYNCN	Load 1	10		40	ns
2	OSC ↑ to SYSCLK1N	Load 1			40	ns
3	OSC ↑ to SYNCLKN	Load 1			40	ns
4	OSC ↑ to CLKPCN	Load 1			40	ns
5	OSC ↑ to CLK02N	Load 1			40	ns
6	SYNCN ↓ to AS ↑	Load 1	1r – 10		1r + 5	ns
7	SYNCN ↓ to AS ↓[4]	Load 1	2.5r – 10		2.5r + 15	ns
8	SYNCN ↓ to DSN ↓ (Read)	Load 1	3r – 5		3r + 20	ns
9	SYNCN ↓ to DSN ↑ (Read)[3]	Load 1	10		25	ns
10	SYNCN ↓ to DSN ↓ (Write)	Load 1	3r – 5		3r + 20	ns
11	SYNCN ↓ to DSN ↑ (Write)[3]	Load 1	4.5r – 5		4.5r + 10	ns
12	SYNCN ↓ to Address Valid	Load 2	-		65	ns
13	SYNCN ↓ to Data Valid	Load 2	-		3r + 43	ns
14	SYNCN ↓ to M/ION, RD/WN, IN/OPN, INTREN Valid	Load 1	-		70	ns
15	SYNCN ↓ to HLDAKN Valid	Load 1	-		20	ns
16	SYSCLKN1 ↓ to T1 Valid	Load 1	-		60	ns
17	SYSCLKN1 ↓ to OVIN Valid	Load 1	-		150	ns
18	SYNCN ↓ to AD Bus Hi-Z (Read)[6]	Load 3	-		3r + 50	ns
19	SYNCN ↓ to AD Bus Active (Read)	Load 3	15		-	ns
20	PAUSEN ↓ to AD Bus Hi-Z[6]	Load 3	-		70	ns
21	PAUSEN ↑ to AD Bus Valid	Load 3	-		60	ns
22	PAUSEN ↓ to AS, DSN, M/ION, RD/WN, IN/OPN Hi-Z[6]	Loads 4, 5[8]	-		50	ns
23	PAUSEN ↑ to AS, DSN, M/ION, RD/WN, IN/OPN Valid	Loads 4, 5[8]	-		59	ns
24	HLDAKN ↓ to AD Bus Hi-Z[6]	Load 3	-		60	ns
25	HLDAKN ↑ to AD Bus Valid	Load 3	-		50	ns
26	HLDAKN ↓ to AS, DSN, M/ION, RD/WN, IN/OPN Hi-Z[6]	Loads 4, 5[8]	-		50	ns
27	HLDAKN ↑ to AS, DS,N M/ION, RD/WN, IN/OPN Valid	Loads 4, 5[8]	-		50	ns
28	Address after SYNCN ↓	Load 2	3r – 5		-	ns
29	Data after SYNCN ↓	Load 2	8		-	ns
30	M/ION, RD/WN, IN/OPN, INTREN after SYNCN ↓	Load 1	5		-	ns
31	HLDAKN after SYNCN ↓	Load 1	– 7		-	ns
32	T1N after SYSCLK1N ↓	Load 1	5		-	ns
33	OVIN after SYSCLK1N ↓	Load 1	5		-	ns
34	Data to SYNCN ↓		30		-	ns
35	Microcode to CLK02N ↓		10		-	ns
36	Microcode to SYSCLK1N ↓		10		-	ns
37	RDYN to OSC ↓		15		-	ns
38	IRDYN to OSC ↓		15		-	ns
39	Data after SYNCN ↓		0		-	ns
40	Microcode after CLK02N ↓		5		-	ns
41	Microcode after SYSCLK1N ↓		15		-	ns
42	RDYN after OSC ↓		5		-	ns
43	IRDYN after OSC ↓		10		-	ns
44	SYNCN ↓ to SYNCN ↓ (7)		5r – 2		5r + 2	ns
45	RESET ↑ to RESET ↓ (7)		-		2	SYNC
46	RESET ↑ to Related Outputs Valid (7)		-		50	ns
47	PIFN to Related Outputs Valid		-		50	ns
48	HOLDN to Related Outputs Valid (7)		-		50	ns
49	DSN to Data Valid (Write)(7)	Load 5 (DSN), Load 3 (Data)	15			ns

Notes:
(1) T_A = +25°C, -55°C and +125°C tested at VDD = 4.5 V and 5.5V
(2) r = 1 OSC period. 0.5r implies 50% OSC duty cycle.
(3) Add 1r for internal XIO; nr for memory wait.
(4) Excluding DMA and Hold conditions.
(5) Unless otherwise noted: V_{IL} = ≥0.0 V, V_{IHTTL} ≤4.0 V, V_{IHOSC} = 4.0 V timing measured from 50% to 50% points.
(6) High impedance measured by 20% (of VDD) voltage change using 1K-ohm pullup resistor.
(7) Data obtained by characterization or analysis; not routinely measured.
(8) Load 4 applies to bus interface signals AS, RD/W and IN/OP; Load 5 applies to bus interface signals M/ION and DSN.

Table 4. Timing Parameter Values

6.0 Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply voltage	-0.5	7	V
Input voltage	-0.3	V_{DD} + 0.3	V
Current through any pin	-20	20	mA
Operating temperature	-55	125	°C
Storage temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Ratings

7.0 DC Electrical Characteristics

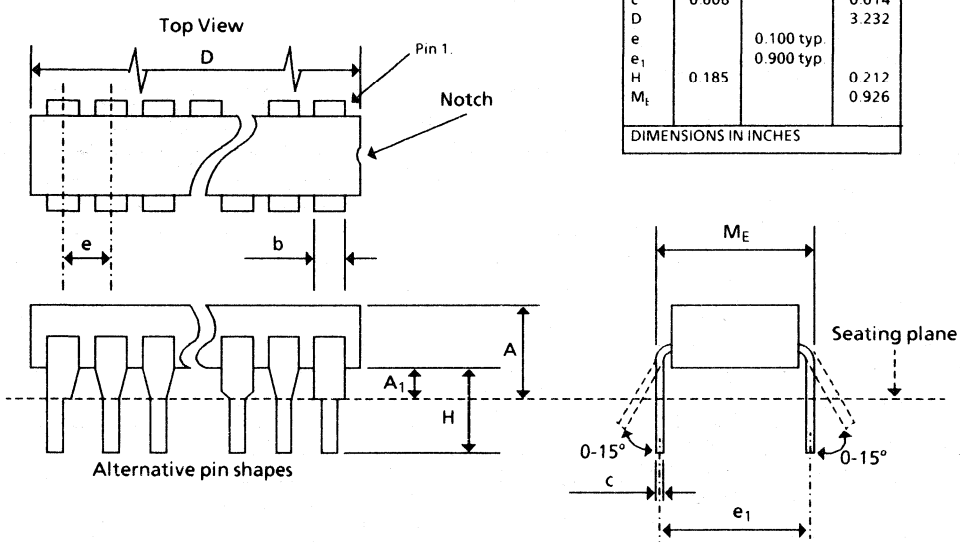
Symbol	Parameter	Condition	Total Dose Radiation Not Exceeding $3x10^5$ RAD (Si)			Units
			Min.	Typ.	Max.	
V_{DD}	Supply voltage	V_{SS} = 0	4.5	5.0	5.5	V
V_{IHC}	CMOS Input High Voltage (Note 1)	-	V_{DD}-1	-	-	V
V_{ILC}	CMOS Input Low Voltage (Note 1)	-	-	-	V_{SS} + 1	V
V_{IHT}	TTL Input High Voltage (Note 2)	-	2.0	-	-	V
V_{ILT}	TTL Input Low Voltage (Note 2)	-	-	-	0.8	V
V_{CH}	OSC Input High Voltage	-	4.0	-	-	V
V_{CL}	OSC Input Low Voltage	-	-	-	1.0	V
V_{OHC}	CMOS Output High Voltage (Note 1)	I_{OH} = -1.4mA, V_{DD} = 4.5V	4.0	-	-	V
V_{OLC}	CMOS Output Low Voltage (Note 1)	I_{OL} = 2.0mA, V_{DD} = 5.5V	-	-	0.5	V
V_{OHT}	TTL Output High Voltage (Note 2)	I_{OH} = -1.4mA, V_{DD} = 4.5V	3.5	-	-	V
V_{OLT}	TTL Output Low Voltage (Note 2)	I_{OL} = 2.0mA, V_{DD} = 5.5V	-	-	0.4	V
V_{OHCLK}	Clock Output High Voltage (Note 3)	I_{OH} = -12mA, V_{DD} = 4.5V	4.0	-	-	V
V_{OLCLK}	Clock Output Low Voltage (Note 3)	I_{OL} = 12mA, V_{DD} = 5.5V	-	-	0.5	V
I_I	Input Leakage Current (Note 4)	V_{DD} = 5.5V, V_{IN} = 0V or 5.5V	-	-	±10	uA
I_{OZ}	Output Leakage Current (Note 4)	V_{DD} = 5.5V, V_O = 0V or 5.5V	-	-	±50	uA
I_{IPU}	TESTN Input Pull-up Current (Note 5)	V_{DD} = 5.5V, TESTN = 0V	-	-150	-300	uA
I_{DDOP}	Operating Supply Current	V_{DD} = 5.5V, OSC = 20MHz	-	25	35	mA
I_{DDST}	Static Supply Current	V_{DD} = 5.5V, OSC = 0MHz	-	5	10	mA

Notes:
1. The following signals are CMOS compatible:
   a. CMOS inputs: Microcode Bus (M00-M19), TESTN, IRDYN and PIFN.
   b. CMOS outputs: T1, OVIN, INTREN, SYSCLK1N, SYNCLK, CLKPCN and CLKO2N.
2. The following signals are TTL compatible:
   a. TTL inputs: HOLDN, RESET, PAUSEN, RDYN and OSC.
   b. TTL outputs: HOLDAKN and SYNCN.
   c. TTL 3-state outputs: AS, DSN, M/ION, RD/WN and IN/OPN.
   d. TTL 3-state I/O signals: Address/Data Bus (AD00-AD15)
3. The clock output pins, SYSCLK1N, SYNCLK, CLKPCN and CLKO2N have a higher drive capability than the standard outputs.
4. Worst case at T_A = + 125°C, guaranteed but not tested at T_A = -55°C.
5. The TESTN input signal is used during chip test and has an integral pull-up resistor. In normal operation TESTN is at V_{DD}.

Table 6. Operating DC Electrical Characteristics

8.0 Packaging Information

Ceramic Dual-in-line
(Package type C)



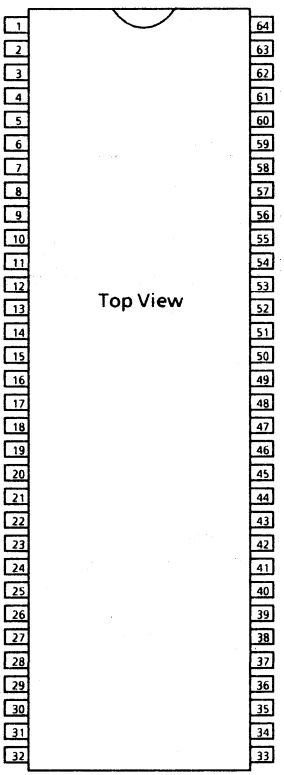
Ref.	Min.	Nom.	Max.
A			0.220
A_1	0.015		0.060
b	0.014		0.023
c	0.008		0.014
D			3.232
e		0.100 typ.	
e_1		0.900 typ.	
H	0.185		0.212
M_E			0.926

DIMENSIONS IN INCHES

Figures 21a. Dimensioned Drawing

MA17501

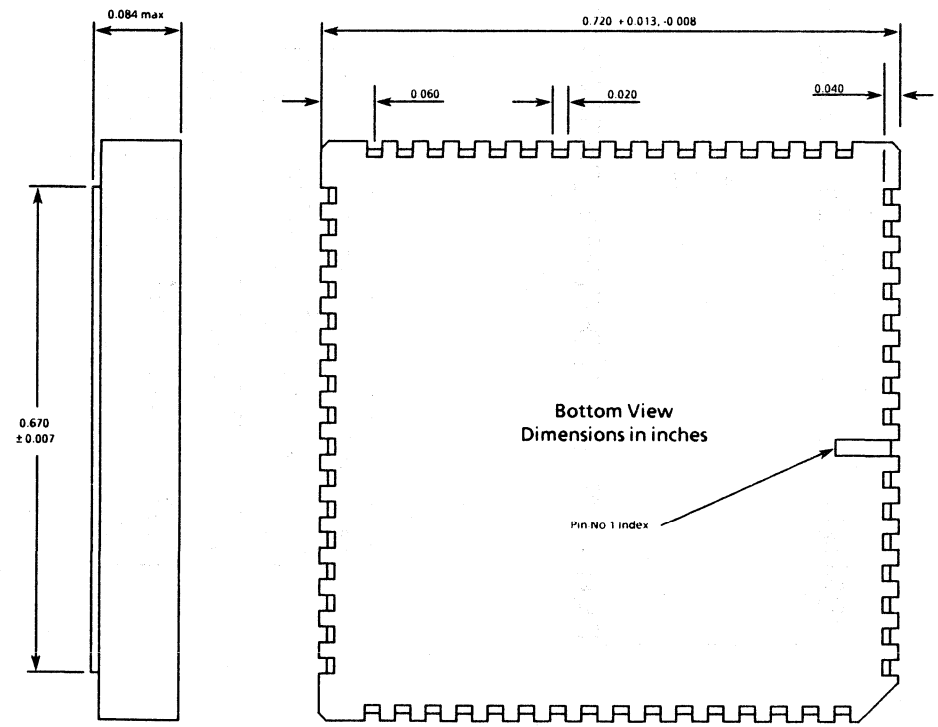
Radiation Hard MIL-STD-1750A Execution Unit



1	OSC	33	M02
2	NC	34	M01
3	SYSCLK1N	35	M00
4	SYNCLKN	36	TESTN
5	CLKPCN	37	AD15
6	CLK02N	38	AD14
7	AS	39	AD13
8	DSN	40	AD12
9	GND	41	NC
10	M/ION	42	VDD
11	RD/WN	43	AD11
12	GND	44	AD10
13	IN/OPN	45	AD09
14	INTREN	46	AD08
15	PIFN	47	AD07
16	M19	48	AD06
17	M18	49	AD05
18	M17	50	AD04
19	M16	51	AD03
20	M15	52	GND
21	M14	53	AD02
22	M13	54	AD01
23	M12	55	AD00
24	M11	56	HOLDN
25	M10	57	RESET
26	M09	58	HLDAKN
27	M08	59	PAUSEN
28	M07	60	T1
29	M06	61	OVIN
30	M05	62	IRDYN
31	M04	63	RDYN
32	M03	64	SYNCN

Figures 21b. Pin Assignments

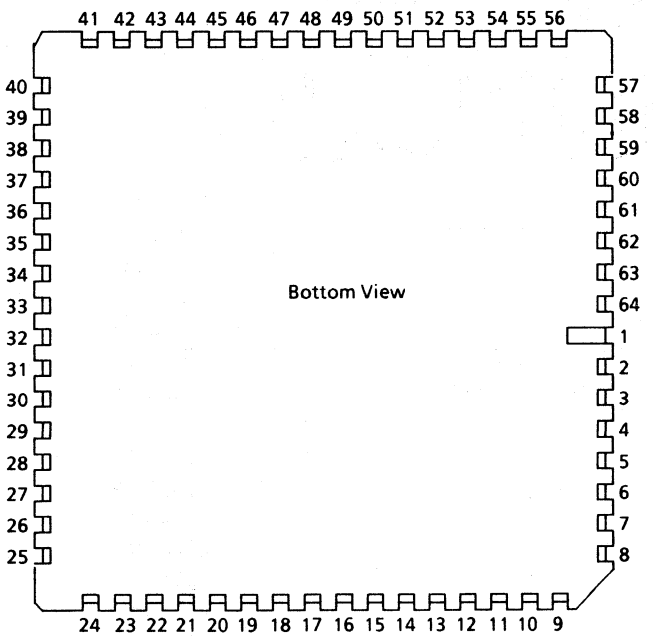
Leadless Chip Carrier
(Package type L)



Figures 22a. Dimensioned Drawing

MA17501

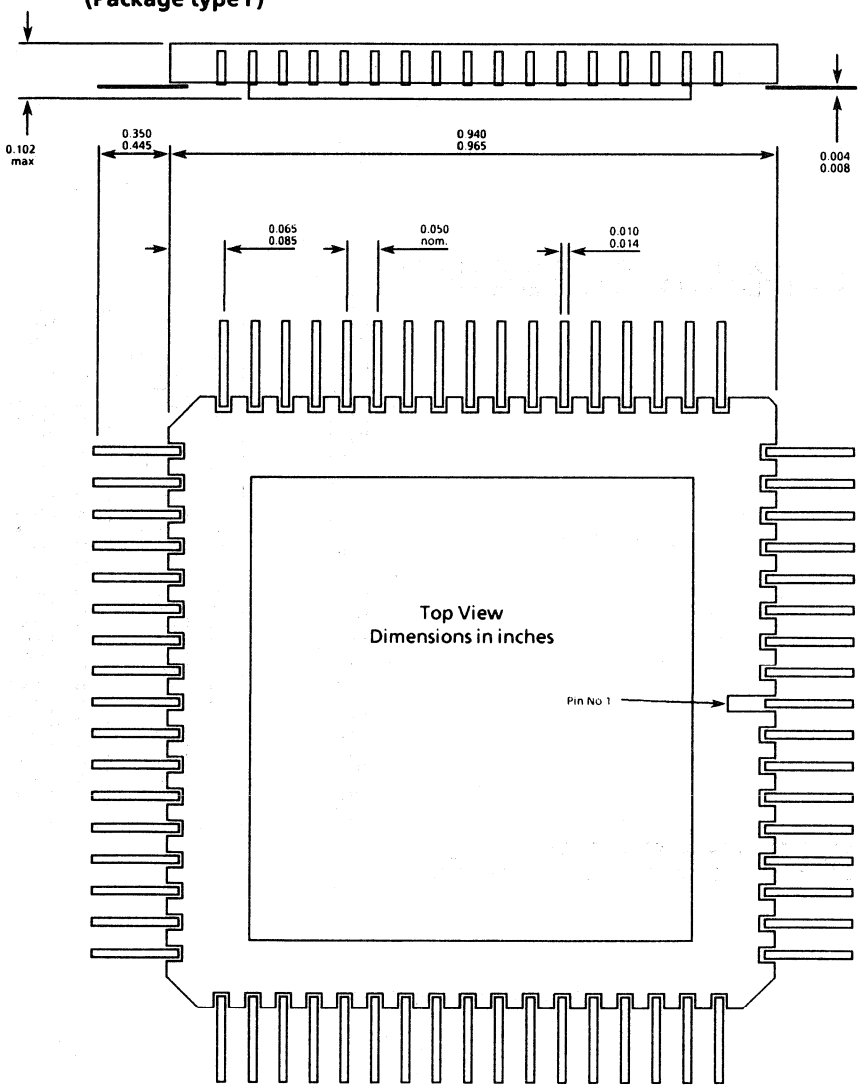
Radiation Hard MIL-STD-1750A Execution Unit



1	OSC	33	M02
2	NC	34	M01
3	SYSCLK1N	35	M00
4	SYNCLKN	36	TESTN
5	CLKPCN	37	AD15
6	CLK02N	38	AD14
7	AS	39	AD13
8	DSN	40	AD12
9	GND	41	NC
10	M/ION	42	VDD
11	RD/WN	43	AD11
12	GND	44	AD10
13	IN/OPN	45	AD09
14	INTREN	46	AD08
15	PIFN	47	AD07
16	M19	48	AD06
17	M18	49	AD05
18	M17	50	AD04
19	M16	51	AD03
20	M15	52	GND
21	M14	53	AD02
22	M13	54	AD01
23	M12	55	AD00
24	M11	56	HOLDN
25	M10	57	RESET
26	M09	58	HLDAKN
27	M08	59	PAUSEN
28	M07	60	T1
29	M06	61	OVIN
30	M05	62	IRDYN
31	M04	63	RDYN
32	M03	64	SYNCN

Figures 22b. Pin Assignments

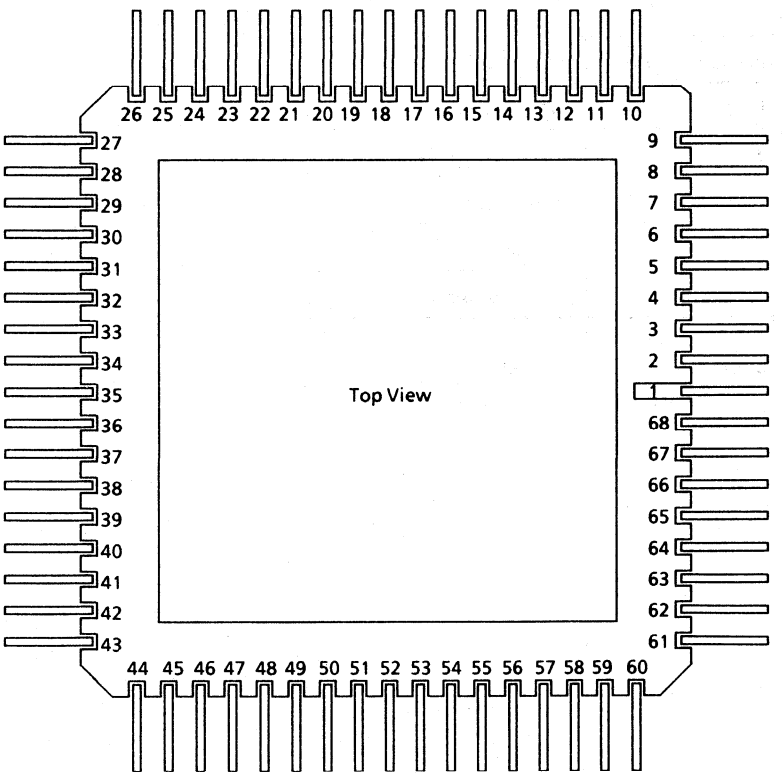
Topbraze Flatpack
(Package type F)



Figures 23a. Dimensioned Drawing

MA17501

Radiation Hard MIL-STD-1750A Execution Unit



1	OSC
2	NC
3	NC
4	SYSCLK1N
5	SYNCLKN
6	CLKPCN
7	CLK02N
8	AS
9	DSN
10	NC
11	GND
12	M/ION
13	RD/WN
14	GND
15	NC
16	IN/OPN
17	INTREN
18	PIFN
19	M19
20	M18
21	M17
22	M16
23	M15
24	M14
25	M13
26	M12
27	M11
28	M10
29	M09
30	M08
31	M07
32	M06
33	M05
34	M04
35	M03
36	M02
37	M01
38	M00
39	TESTN
40	AD15
41	AD14
42	AD13
43	AD12
44	NC
45	NC
46	VDD
47	AD11
48	AD10
49	AD09
50	AD08
51	AD07
52	AD06
53	AD05
54	AD04
55	AD03
56	GND
57	AD02
58	AD01
59	AD00
60	HOLDN
61	RESET
62	HLDAKN
63	PAUSEN
64	T1
65	OVIN
66	IRDYN
67	RDYN
68	SYNCN

Figures 23b. Pin Assignments

9.0 Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Total Dose (Function to specification, note 1)	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$1x10^{10}$ Rad(Si)/s
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/s
Neutron Hardness (Function to specification)	$1x10^{15}$ neutrons/cm2
Latch-up	Not possible
Single Event Upset (note 2)	$<10^{-10}$ errors/bit day

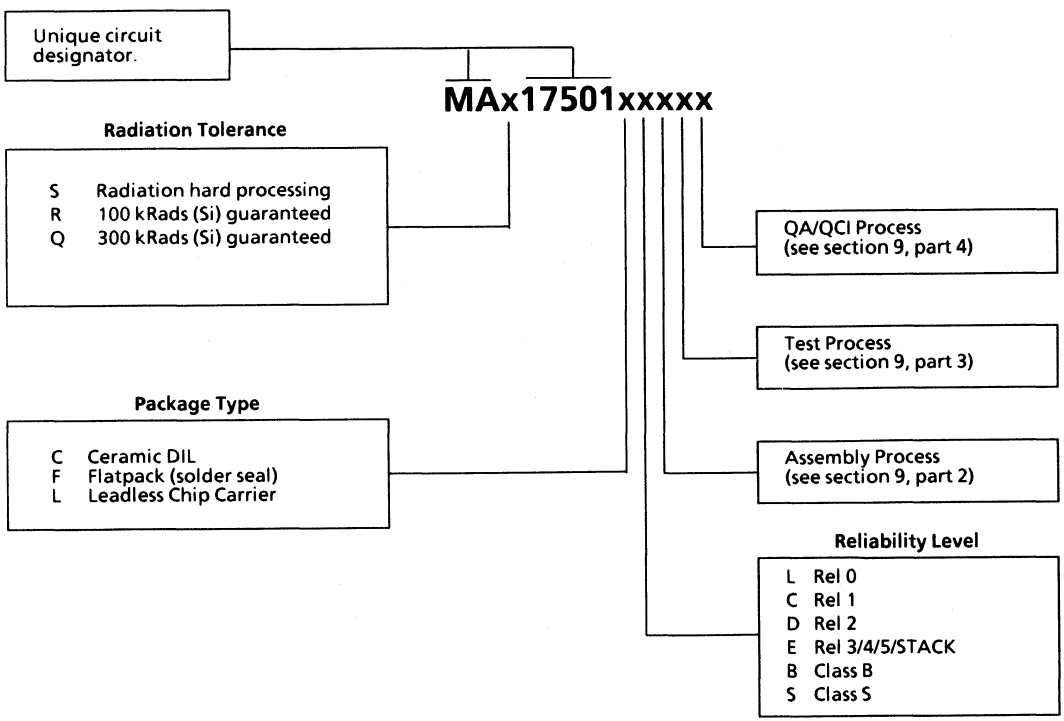
Note 1. Typical performance only, for guaranteed levels see ordering information
2. GSO 10% Worst Case

MA17501

Radiation Hard MIL-STD-1750A Execution Unit

10.0 Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



GEC PLESSEY

SEMICONDUCTORS

S10210FDS Issue 1 September 1990

MA17502

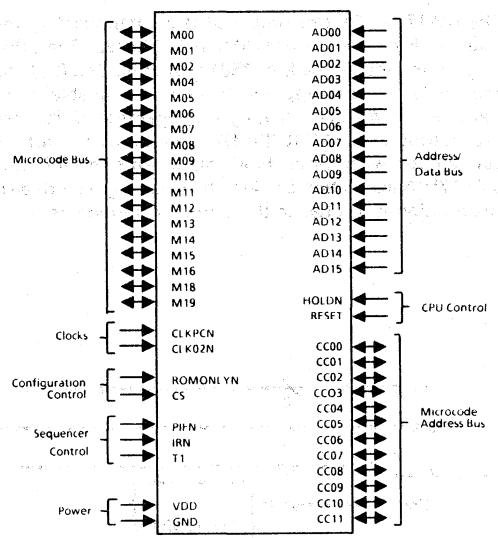
Radiation Hard MIL-STD-1750A Control Unit

2

Features

- MIL-STD-1750A Instruction Set Architecture
- Full Performance over Military Temperature Range
- 12-Bit Microsequencer
  - Instruction Prefetch
  - Pipelined Operation
  - Subroutine Capability
- On-Chip ROM
  - 2K x 40-Bit Microcode Store
  - 512 x 8-Bit Instruction Map
- MAS281 Integrated Built-in Self Test
- TTL Compatible System Interface
- Low Power CMOS/SOS Technology

Block Diagram



Product Description

The MA17502 Control Unit is a component of the Marconi Electronic Devices MAS281 chip set. Other chips in the set include the MA17501 Execution Unit and the MA17503 Interrupt Unit. Also available is the peripheral MA17504 Memory Management Unit/Block Protection Unit. In conjunction these chips implement the full MIL-STD-1750A Instruction Set Architecture.

The MA17502 - consisting of a microsequencer, a microcode storage ROM, and an instruction mapping ROM - controls all chip set operations. Table 1 provides brief signal definitions.

The MA17502 is offered in several speed and screening grades, and in dual in-line, flatpack or leadless chip carrier packaging. Screening options are described in this document. For availability of speed grades, please contact Marconi Electronic Devices.

MA17502

Radiation Hard MIL-STD-1750A Control Unit

GEC PLESSEY
SEMICONDUCTORS

1.0 System Considerations

The MA17502 Control Unit (CU) is a component of the Marconi Electronic Devices MAS281 chip set. The other chips in the set are the MA17501 Execution Unit (EU) and the MA17503 Interrupt Unit (IU). Also available is the peripheral MA17504 Memory Management Unit/Block Protection Unit (MMU(BPU)). The Control Unit, in conjunction with these chips, implements the full MIL-STD-1750A Instruction Set Architecture. Figure 1 depicts the relationship between the chip set components.

The CU provides the microprogram storage and sequencing resources for the chip set. The EU provides the MAS281's system synchronizing and arithmetic/logic computational resources. The IU provides interrupt and fault handling resources, DMA interface control signals, and the three MIL-STD-1750A timers. The MMU/BPU may be configured to provide either 1M-word memory management (MMU) or 1K-word memory block write protection (BPU) functions.

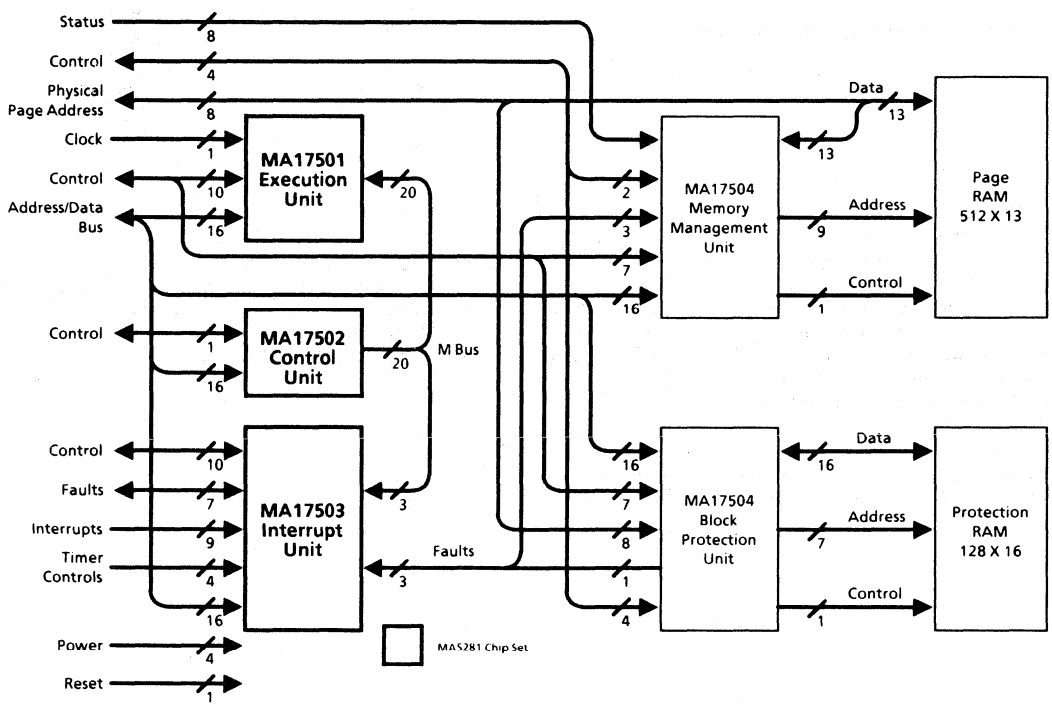


Figure 1. MAS281 Chip Set With Optional MA17504 & Support RAMs

MA17502

Radiation Hard MIL-STD-1750A Control Unit

Signature	I/O	Definition
AD00 - AD15	I	External 16-Bit Address/Data Bus
CC00 - CC11	I/O	12-Bit Microcode Address Bus
$\overline{\text{CLKPC}}$	I	Precharge Clock
$\overline{\text{CLK02}}$	I	Phase 2 Clock
$\overline{\text{CS}}$	I	Chip Select
$\overline{\text{HOLD}}$	I	Hold Request Suspends Internal Processor Functions
$\overline{\text{IR}}$	I	Interrupt Request
M00 - M19	I/O/Z	20-Bit Microcode Bus
$\overline{\text{NC}}$	–	No Connection
$\overline{\text{PIF}}$	I	Privileged Instruction Fault
$\overline{\text{RESET}}$	I	Rest Indicates Device Initialization
$\overline{\text{ROMONLY}}$	I	Indicates if Control Unit to be Used as ROM Only
T1	I	Branch or Jump Control
VDD		Power (External), 5 Volts
GND		Ground

Table 1. Signal Definitions

As shown in Figure 1, the MAS281 is the minimum processor configuration consisting of an Execution Unit, a Control Unit, and an Interrupt Unit. This configuration is capable of accessing a 64K-word address space. Addition of an MMU configured MA17504 allows access to a 1M-word address space. Addition of a BPU configured MA17504 provides hardware support for 1K-word memory block write protection.

The CU, as with all components of the MAS281 chip set, is fabricated with Marconi Electronic Devices' CMOS/SOS process technology. Input and output buffers associated with signals external to the MAS281 are TTL compatible.

Detailed descriptions of the CU's companion chips are provided in separate data sheets. Additional discussions on chip set system considerations, interconnection details, and the Digital Avionics Instruction Set (DAIS) mix benchmarking analysis are provided in separate applications notes.

2.0 Architecture

The Control Unit consists of a microsequencer, an instruction mapping ROM, a microcode storage ROM, and various buses. Details of these components are shown in Figure 2 and are discussed below:

2.1 Microsequencer

The CU microsequencer is a 12-bit wide microcode address generator. Major features of the microsequencer include a microprogram counter (PC), a microprogram counter save register (PC Save), microcode address increment logic, instruction pipeline registers IA and IB, an iteration of loop counter, a next microcode address source multiplexer, and various pipelining latches. These features are represented in Figure 2.

The 12-bit microcode address width allows the microsequencer to access up to 4096 words of microcode. The MIL-STD-1750A instructions are implemented as sequences of microinstructions stored within the lower 2048 locations of this address space. The address for each microinstruction in a sequence is provided by the next microcode address source multiplexer. This multiplexer, under control of the CU control logic, select from one of six next address sources. Sequential, direct jump, conditional jump, and subroutine address generation modes are supported.

Sequential addressing is accomplished by providing a path from the output of the next microcode address multiplexer to an incrementer and back to the PC register input. Direct jumps are supported by routing a portion of the microinstruction to one of the next microcode address source multiplexer inputs. Conditional jumps are determined in the ALU of the Execution Unit which communicates the decision to the CU via the T1 signal. The T1 signal enables a portion of the microcode word to create the new address. Subroutine jumps are accomplished by loading the contents of the incremented PC register into the PC Save register and then performing a direct jump. Upon completion of the subroutine, the contents of the PC Save register are used as the next microcode address.

A new microinstruction sequence begins when an opcode residing in the IA or IB register is selected by the next microcode address source multiplexer and used as an address to simultaneously access both the CU's Instruction Mapping ROM and the Microcode Storage ROM. The instruction Mapping ROM access provides a pointer which is then used to update the microprogram counter (PC); the Microcode Storage ROM access provides the first microinstruction of the sequence. Remaining microinstructions in a sequence are accessed through the use of the four address generation modes discussed above.

Iterative microprogram operations are achieved through the use of the loop counter. The loop counter may be selectively loaded from either the AD bus or directly from microcode. This counter tracks the number of iterations remaining and, when appropriate, issues a completion signal (CZ). When an iterative operation is called for, the loop counter is loaded and the CU control logic repeats a particular microinstruction sequence, using the four address generation modes discussed above, until the CZ signal is received.

2.2 Instruction Mapping ROM

The CU instruction mapping ROM provides 512 8-bit words of microcode instruction vector storage. The address space of this ROM is mapped into a portion of the microcode storage ROM's address space. Hence, both ROMs are accessed whenever the microcode address falls within this range. The eight bits from the instruction mapping ROM serve as the lower eight bits of a 12-bit microcode address; the upper four bits are a hardwired constant. The 12-bit microcode address formed from the 4-bit constant and the mapping ROM's eight bits are loaded into the PC register of the microsequencer and serve as a means to access non-sequential microcode addresses within the address space allocated to both the instruction mapping and microcode storage ROMs.

2.3 Microcode ROM

The CU microcode ROM provides 2K (2048) 40-bit words of storage capacity. All of the microcode required to implement the full MIL-STD-1750A Instruction Set Architecture (ISA) fits in one such ROM.

2.4 Buses

A 16-bit multiplexed Address/Data (AD) bus provides a communications path between the CU, the other components of the MAS281 chip set, the MA17504 MMU/BPU, and any other devices mapped into the chip set's address space. The CU receives MIL-STD-1750A instructions, accessed from system memory, over this bus and loads them into its instruction pipeline registers.

A 20-bit multiplexed Microcode (M) bus provides a pathway between the CU chip and the microcode decode logic on all other chips which are under CU microcode control. The 40-bit wide microinstructions from the CU's microcode ROM are multiplexed on chip as two 20-bit words and presented on the interchip M bus during alternate phases of CLK02N. Microcode bits 39 through 20 are placed on the M bus during the CLK02N low phase and bits 19 through 0 during the high phase of CLK02N. The M bus is bidirectional to permit microcode memory expansion.

A 12-bit microcode address (CC) bus is used to route microcode addresses from the next microcode address source multiplexer to the microcode and instruction mapping ROMs as shown in Figure 2.

3.0 Interface Signals

All signal definitions are shown in Table 1. In addition, each of these functions is provided with Electrostatic Discharge (ESD) protection diodes. All unused inputs must be held to their inactive state via a connection to VDD or GND.

Throughout this data sheet, active low signals are denoted by either a bar over the signal name or by following the name with an "N" suffix. e.g. HOLDN. Referenced signals that are not found on the MA17502 are preceded by the orginating chip's functional acronym in parentheses, e.g. (IU)DMAKN.

A description of each pin function, grouped according to functional interface, follows. The function acronym is presented first, followed by its definition, its type, and its detailed description. Function type is either input, output, high impedance (Hi-Z), or a combination thereof. Timing characteristics of each of the functions described are provided in Section 6.0.

3.1 Power Interface

The power interface consists of a single 5V VDD connection and two common GND connections.

3.2 Clocks

The clock interface, discussed below, is the means by which the synchronous, microcoded operation of the MAS281 is driven.

3.2.1 Precharge Clock (CLKPCN)

Input. The MA17501 Execution Unit (EU), generates the CLKPCN signal for the Control Unit. The Control Unit uses this signal for most of its internal sequencing. During the low phase of CLKPCN, the internal M Bus is precharged to the high state to accelerate its response.

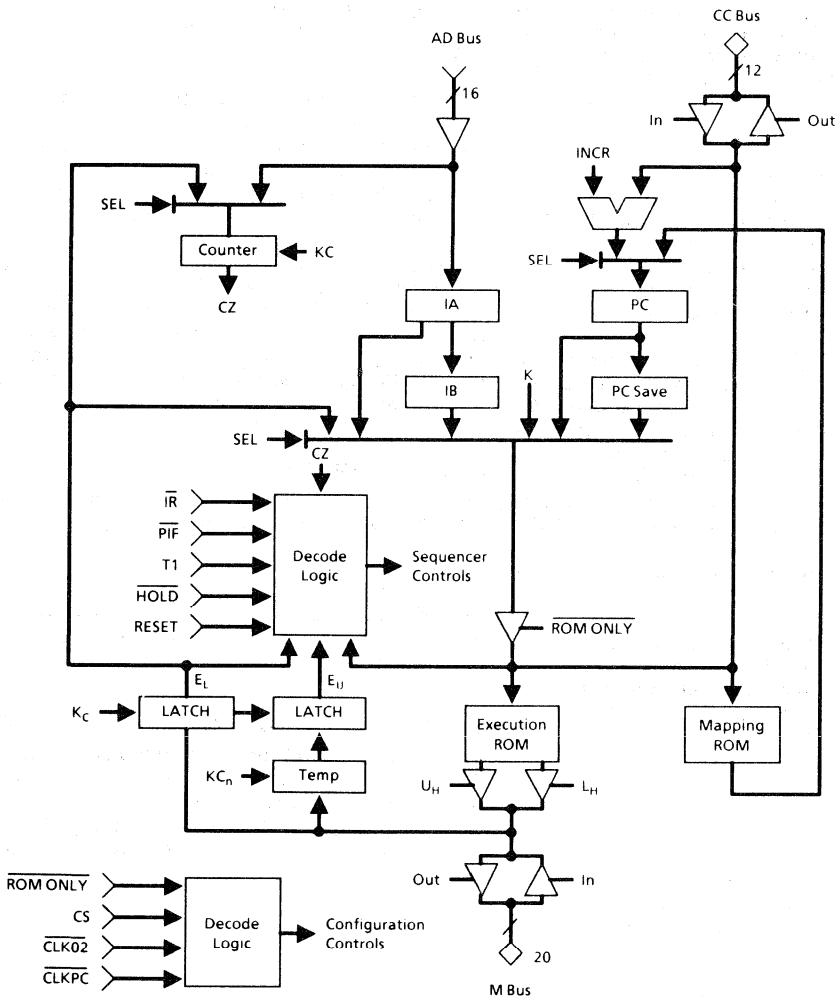


Figure 2. MA17502 Control Unit Architecture

The normal CLKPCN period is defined by five OSC cycles (two cycles low and three cycles high). When a microcode branch is indicated by the EU, the low state of CLKPCN is extended to three OSC cycles. During execution of Interrupt Unit decoded XIO and microcode commands, the high state of CLKPCN is extended to four OSC cycles. Also, during external bus cycles, RDYN may be used to cause the EU to prolong the high state of CLKPCN to greater than three OSC cycles; this allows the MAS281 chip set to interface with slower external memory or input/output devices.

During DMA ((IU)DMAKN is low) or Hold ((EU)HLDAKN is low), CLKPCN will remain low until the CPU takes control again.

3.2.2 Phase 2 Clock(CLK02N)

Input. The MA17501 generates the CLK02N signal for the Control Unit. The CU then uses this signal, in conjunction with CLKPCN, to control the distribution of microcode on the M Bus. CLK02N is used to multiplex the 40-bit microcode instruction into two 20-bit words (μW1 and μW2). The high-to-low edge of CLK02N switches μW1 (bits 39 through 20) off the M Bus while switching μW2 (bits 19 through 0) onto the M Bus.

The normal CLK02N period is defined by five OSC cycles (one cycle low, three cycles high, one cycle low). When a microcode branch is indicated by the EU, the high state of CLK02N is extended to four cycles. During execution of Interrupt Unit decoded XIO and microcode commands, the trailing low state of CLK02N is extended to two OSC cycles. Also, during external bus cycles, RDYN may be used to cause the EU to prolong the CLK02N trailing low state to greater than one OSC cycle; this allows the MAS281 chip set to interface with slower external memory or input/output devices.

During DMA ((IU)DMAKN is low) or Hold ((EU)HLDAKN is low), CLKPCN will remain low until the CPU takes control again.

3.3 Buses

The following is a discussion of the communication buses connecting the three-chip set. The AD Bus and M Bus are mainly operand transfer buses, while the CC Bus is strictly for providing microcode addresses to auxiliary CUs.

3.3.1 Address/Data Bus(AD Bus)

Input. These signals comprise the multiplexed address and data bus. During external bus operations, the AD bus accommodates the transfer of instructions, from memory and I/O ports, to the MA17502. During internal bus operations, the AD bus provides additional data to the Control Unit from the Execution Unit. AD00 is the most significant bit position and AD15 is the least significant bit position of both the 16-bit data and 16-bit address. A high on this bus corresponds to a logic 1 and a low corresponds to a logic 0. Information on the AD Bus is clocked into the CU by the high-to-low transition of CLKPCN.

3.3.2 Microcode Bus (M Bus)

Input/Output/Hi-Z. The M Bus is the 20-bit multiplexed microcode bus. The 40-bit microcode instruction is multiplexed onto the M Bus as two 20-bit words (μW1 and μW2). The first half of the microcode word, μW1 (bits 39 through 20), is assured valid on the high-to-low transition of CLK02N and μW2 (bits 19 through 0) is assured valid on the high-to-low transition of CLKPCN. M00 corresponds to microcode bit 0 (μW1) or 20 (μW2) while M19 corresponds to microcode bit 19 (μW1) or 39 (μW2). A high level indicates a logic 1 and a low level indicates a logic 0. A high level on CS allows the Control Unit to distribute microcode over this bus, a low level places the bus in the high impedance state.

During DMA or Hold states, CLKPCN is held low, thus holding the internal M bus in the precharged state. Precharging the internal M Bus forces the 20 bits of the external M Bus low.

3.3.3 Microcode Address Bus (CC Bus)

Input/Output/Hi-Z. The CC bus is provided for future expansion and is left unconnected.

3.4 Sequencer Control

The following is a discussion of the microsequencer control input signals. These signals support chip set functions that require microcode branching based on the results of operations performed in the Execution or Interrupt Units.

3.4.1 Interrupt Request (IRN)

Input. A low on this input directs the CU to service pending interrupt requests latched by the Interrupt Unit (IU). Upon completion of the currently executing MIL-STD-1750A instruction, the CU checks the IRN input. If IRN is low, then the CU sequencer will branch to the microcoded interrupt service routine; else the next MIL-STD-1750A instruction is mapped to its microcode routine. The microcoded interrupt service routine stores the processor state, retrieves the highest priority pending interrupt's service routine processor state, and vectors software execution to the user's interrupt service routine. IRN originates in the IU.

3.4.2 Privileged Instruction Fault (PIFN)

A low on this signal causes the CU to enable control of the DMA interface (located in the Interrupt Unit), abort the currently executing MIL-STD-1750A instruction and check the IRN input for a pending level 1 interrupt caused by the IU latching a memory protect (MPROEN), memory address (EXADEN), or Bus Time-out fault. PIFN originates in the IU.

3.4.3 Branch or Jump Control (T1)

Input. A high on this input directs the CU microcode address sequencer to branch execution to a non-sequential microcode address. This signal is under the control of the Execution Unit's ALU and its level is dependent on the outcome of the presently executing microcode instruction, e.g. conditional branch. T1 originates in the EU.

3.5 Configuration Control

The following inputs are provided for control of multiple CU systems. They allow for expansion of the microcode store to 4K 40-bit words.

3.5.1 ROM-Only (ROMONLYN)

Input. This signal is provided for future microcode expansion and must be pulled up to VDD.

3.5.2 Chip Select (CS)

Input. A high on this signal enables the CU to drive the 20-bit external M Bus. This signal is provided for future microcode expansion and must be pulled up to VDD.

3.6 CPU Control

Grouped under this heading are signals that have CPU-wide control of normal operation. Each of these has the ability to "freeze" the processor.

3.6.1 Hold Request (HOLDN)

Input. A low on this input will suspend internal processor functions at the end of the currently executing MIL-STD-1750A instruction. When this signal becomes active, the CU completes the currently executing MIL-STD-1750A instruction, then branches to the Hold microcode routine and enters the Hold state. The CU will resume normal operation by refilling the instruction pipeline registers (IA and IB) upon release of HOLDN.

3.6.2 System Reset (RESET)

Input. A high on this input for a duration of at least one CLKPCN period will reset the MAS281 chip set by forcing the Control Unit to microcode address zero. The high-to-low transition of this input will cause the CU to begin executing the MAS281 initialisation sequence starting with the first instruction in microcode. Built-in Test (BIT) is performed as part of the initialisation sequence. At the conclusion of initialisation and successful execution of BIT, the MAS281 will be initialised as shown in Table 3.

4.0 Operating Modes

The following discussions detail the MAS281 chip set operating modes from the perspective of the Control Unit. MAS281 operating modes involving the MA17502 include: (1) Initialisation, (2) Instruction Execution, (3) Interrupt Servicing, (4) DMA Support, and (5) HOLD Support.

4.1 Initialisation

The MA17502 sequences the MAS281 chip set through the microcoded initialisation routine in response to a high pulse on the RESET input. This routine clears the chip set registers, disables and masks interrupts, reads the configuration register, resets the output discrete register (if applicable), initialises the MMU and BPU (if applicable), performs Built-in Test (BIT), raises the Start-Up ROM Enable discrete, clears and starts timers A and B, resets the Trigger-Go counter, and loads the instruction pipeline. The initialisation sequence is contained in the first 33 locations of microcode ROM (an additional 14 locations contain the optional MMU and BPU initialisation code). Because the initialisation sequence clears the Execution Unit's Instruction Counter and Status Word (also the address and processor state copies stored in the MMU(BPU), if applicable), program execution begins with the instruction located at address zero (page zero). Table 2 provides a detailed breakdown of the initialisation sequence and Table 3 summarises the resulting initialised state.

BIT occupies 332 words of microcode storage ROM, and consists of five subroutines that exercise the internal circuitry of the MAS281, as outlined in Table 4. BIT begins by pulling the Normal Power-UP ((IU)NPU) output low; this is the first time after power-up that the state of NPU is guaranteed. If all five BIT subroutines execute successfully, NPU is raised high.

If any part of BIT fails, an error code identifying the failed subroutine is loaded into the Interrupt Unit Fault Register (via the AD Bus), BIT is aborted, and NPU is left in the low state. Table 4 defines the coding of the BIT results. (NPU is raised high through microcode control of the IU in conjunction with the (EU)INTREN signal. The BIT error codes are loaded in the IU Fault Register via the AD Bus under microcode control of the IU in conjunction with the (EU)INTREN signal.)

In the event of such a failure, the resulting chip set reset state is dependent on where in BIT the error occurred and may not be the same as that shown in Table 3. A BIT failure indication in the fault register sets the level 1 pending interrupt. Since initialisation disables and masks interrupts, the IRN input will remain high; thus the interrupt will not be serviced immediately.

The last action performed by the initialisation routine is to load the instruction pipeline. Instruction fetches start at memory location zero (page zero) from the Start-Up ROM (if implemented). Whether BIT passes or not, the processor will begin instruction execution at this point.

Note: To complete initialisation and pass BIT, interrupt and fault inputs must be high for the duration of the initialisation routine. Also, the Timers A and B must be clocked for BIT success.

Label	Cycle	
MAIN	B1	1. Enable Control of DMAE Output signal
	P	2. -
	B1	3. Clear MAS281 Execution Unit Status Word (SW) Clear Interrupt Mask (MK) (Internal I/O command, SKM, 2000H)
	B1	4. Clear Pending Interrupt Register (PI) and Fault Register (FT) (Internal I/O Command, CLIR, 2001H) Clear Instruction Counter (IC)
	P	5. -
	B1	6. Disable Interrupts (Internal I/O Command, DSBL, 2003H)
	P	7. -
	B1	8. Clear MMU Status Word (Internal I/O Command, WSW, 200EH) (Note 1)
	P	9. -
	B1	10. Disable DMA Access (Internal I/O Command, DMAD, 4007H)
	P	11. -
	B1	12. Read Configuration Register (Internal I/O Command,RCW, 8400H, CONFWN Drops low per Figure 25, Section 5.0)
	P	13. -
	P	14. -
	B2	15. - (If Output Discrete Register Present, then Continue; Else, Skip to 18.)
	p	(16). -
	I/O	(17). Clear Output Discrete Register (External I/O Command)
	P	18. -
	B2	19. - (If BPU present, then Branch to BPU; else, continue)
	P	20. -
	B2	21. - (If MMU present, then Branch to MMU; Else, Continue)
	p	22. -(Setup Temporary Register to indicate No MMU Present)
	B2	23. -(Branch to MAS281 BIT)
	P	24. -
	B1	25. Enable Start-Up ROM (Internal I/O Command, ESUR, 4004H; SURE Raises High per Figure 25, Section 5.0)
	P	26. -
	B1	27. Clear and Start Timer A (Internal I/O Command, OTA, 400AH)
	B1	28. Reset the Trigger-Go timer (Internal I/O Command, GO, 400BH)
	P	29. -
	B1	30. Clear and Start Timer B (Internal I/O Command, OTB, 400EH)
	B2	31. -(Branch to Load Instruction Pipeline Routine)
	M	32. Load data-In register (DI) and instruction Register A (IA) from [IC], Increment IC
	M	33. Load Data-In Register (DI) and Instruction Register a (IA) from [IC] ([IA] Moves to IB), Increment IC, Map Instruction Register B (IB) into Microcode Routine
BPU	P	(1). -
	P	(2). -(Set Loop to Clear Memory Protect RAM)
	I/O	(3). Clear a Location in MPRAM (Internal I/O Command, LMP, 50XXH), Increment Address; Do 128 Times
		(4). -(Branch Back to 20.)
MMU	P	(1). -
	P	(2). -
	P	(3). -(Setup Loop to Load Instruction Page Registers (IPR) and Operand Page Registers (OPR) with Sequential Values of 0 to 255)
	P	(4). -
	P	(5). -
	I/O	(6). Load a Location in the IPR with the value of the Location Address (Internal I/O Command, WIPR, 51XYH)
	I/O	(7). Load a Location in the OPR Increment Loaded Value with the Value of the Location Address (Internal I/O Command, WOPR,52XYH)
	P	(8). -(Increment IPR Address)
	P	(9). -(Increment OPR Address; Repeat Loop [4. - 9.] 256 Times)
	B2	(10). -(Setup Temporary Register to Indicate MMU Present; Branch back to 23)

Notes:
1. This operation is performed whether or not an MMU is present.
2. "-" indicates internal CPU operation.
3. Sequence numbers in "( )" are performed only under the stated conditions.
4. Each step enumerated above represents a single machine (SYNC) cycle of the type shown in the "Cycle" column.
   "P" indicates a 5 OSC cycle, 60% duty cycle, machine cycle.
   "I/O" and "M" indicate a 5 OSC cycle, 50% duty cycle, machine cycle.
   "B1" indicates a 6 OSC cycle, 50% duty cycle, machine cycle.
   "B2" indicates a 6 OSC cycle, 66% duty cycle, machine cycle.

Table 2. MAS281 Initialisation Sequence

MA17502
Radiation Hard MIL-STD-1750A Control Unit

MAS281	
Instruction Counter (IC)	Zeroed
Status Word (EU and MMU) (SW)	Zeroed
Fault (FT)	Zeroed
Pending Interrupt (PI)	Zeroed
Mask (MK)	Zeroed
General Register File (R0 R15)	Zeroed
Interrupts	Disabled
DMA Access	Disabled
Timer A	Reset and Started
Timer B	Reset and Started
Trigger-Go Timer	Reset and Started
MMU	
Page Registers	Group Zero Enabled
AL, W, E, Fields	Zeroed
PPA Field	Logical to Physical Map
BPU	
Write Protect	Zeroed
Global Memory Protect	Enabled

Table 3. Initialisation State

BIT	Test Coverage	BIT Fail Codes ($FT_{13, 14, 15}$)	Cycles
1	Microcode Sequencer IB Register Control Barrel Shifter Byte Operations and Flags	100	221
2	Temporary Registers (T0 - T7) Microcode Flags Multiply Divide	101	166
3	Interrupt Unit - MK, PI, FT Enable/Disable Interrupts	111	214
4	Status Word Control User Flags General Registers (R0 - R15)	110	154
5	Timer A Timer B	111	763
-	BIT Pass/Fail Overhead	-	26

Note: BIT pass is indicated by all zeros in FT bits 13, 14 and 15.

Table 4. Built In Test (BIT) Summary

4.2 Instruction Execution

The MIL-STD-1750A microcoded instruction subroutines are stored in 1255 locations of microcode storage ROM. The Control Unit receives instructions from memory, via the AD Bus, through the instruction pipeline registers IA and IB. When the previous instruction or special process (Interrupts or Hold) has been completed, the new instruction residing in register IB is selected by the next microcode address source multiplexer. A 4-bit hardwired constant, appended by the instruction opcode, is then used as the first address of a microcode sequence which distributes the required control to execute the instruction. The microsequencer generates the remaining microcode addresses necessary to complete the sequence as described in Section 2.0 of this data sheet entitled, "Architecture".

Upon completion of the current instruction, the CU will accept the next instruction in the program unless an interrupt, DMA, or Hold request is received. The interrupt and Hold request share a common branch point in microcode. If an interrupt and Hold request are both pending at the conclusion of the MIL-STD-1750A instruction microcode routine, the Hold request has priority and is serviced first. Upon release of the Hold state, the first instruction will execute even if the interrupt is still pending; when this instruction is complete the interrupt will be serviced (assuming the HOLDN input has not been driven low during execution of this instruction). Interrupt, DMA, and Hold support are explained in more detail in following sections.

4.3 Direct Memory Access

Direct Memory Access (DMA) is controlled by the Execution Unit (EU) in concert with the Interrupt Unit DMA interface. The CU supports DMA by suspending processor control upon completion of the current machine cycle. If DMA is enabled ((UI)DMAE signal, high) a DMA request ((IU)DMARN input, low) to the MAS281 causes the IU to acknowledge with DMAKN, low. When the EU receives the DMAKN (DMA Acknowledge) signal from the IU, the CU clocks are suspended (CLKPCN, low; CLK02N, high) halting the MAS281's microcode sequencing. Microinstruction execution remains suspended until DMARN is removed. When DMARN is removed, microcode execution resumes where DMARN had interrupted it.

4.4 Interrupt Handling

Interrupts are handled by the interrupt Unit (IU) and communicated to the CU via the IRN input. The CU checks the status of the IRN (Interrupt Request) signal after the completion of each MIL-STD-1750A microcode instruction sequence. If the IRN signal is low, the CU initiates interrupt handling, otherwise the CU processes a new instruction.

IU interrupt handling is controlled by the CU through three microcode bits - M04, M05, and M06. Upon receipt of the IRN signal and after completion of the currently executing instruction, the CU branches to a microcoded interrupt handling routine. The microprogram sequence supplies microcoded control to the IU for reading the highest priority pending interrupt vector code, which also clears this pending interrupt.

Due to the similarity of interrupt and hold request handling by the CU, if a Hold and interrupt request are pending at the end of an instruction sequence the Hold has priority and will be serviced .

4.5 Hold Support

The CU accepts a Hold request in much the same way as an interrupt request. After the completion of each MIL-STD-1750A microcode instruction sequence, the CU checks the status of the HOLDN signal. If the HOLDN signal is low, a microcoded sequence suspends further internal processing functions; otherwise, the CU processes a new instruction or services interrupt requests (Hold requests have priority over interrupt requests).

The Control Unit responds to an active HOLDN signal, upon completion of the currently executing instruction, but branching to a microprogrammed sequence of instructions that suspends all internal operations. This sequence of microinstructions allows the processor to resume instruction execution at the point HOLDN was accepted when the CU regains control of the processor. The MAS281 remains in the Hold state until HOLDN is pulled high (if the Hold state was reached through the hardware interface, HOLDN) or HOLDN is pulsed low (if the Hold state was reached through software, BPT instruction).

5.0 Software Considerations

The MAS281 chip set implements the full MIL-STD-1750A instruction set. Table 6a gives a brief listing of this instruction set and provides performance data for each instruction. Table 6b provides a summary of the I/O commands implemented in MAS281 and MA17504 MMU/BPU hardware. A complete description of this instruction set is provided in MIL-STD-1705A (Notice 1). The register set available to the software programmer is depicted in Figure 3. A discussion of data types, addressing modes, and benchmarking considerations follows.

5.1 Data Types

The MAS281 chip set supports 16-bit fixed-point single-precision, 32-bit fixed-point double-precision, 32-bit floating-point, and 48-bit extended-precision floating-point data types. Figure 4 depicts the formats of these data types.

All numerical data is represented in two's complement form. Floating-point numbers are represented by a fractional two's complement mantissa with an 8-bit two's complement exponent. The MAS281 expects all floating point operands to be normalised. If they are not normalised, the results from an instruction are not defined.

5.2 Addressing Modes

The MAS281 chip set supports the eight addressing modes specified in MIL-STD-1750A. These addressing modes are shown in Figure 5 and are defined below.

5.2.1 Register Direct (R)

The register specified by the instruction (RB) contains the required operand.

5.2.2 Memory Direct (D,DX)

Memory Direct (without indexing) is an addressing mode in which the instruction contains the memory address (A) of the required operand. In Memory Direct (indexed), the memory address of the required operand is specified by the sum of the contents of an index register (RX) and the instruction address field (A). Registers R1 through R15 may be specified for indexing.

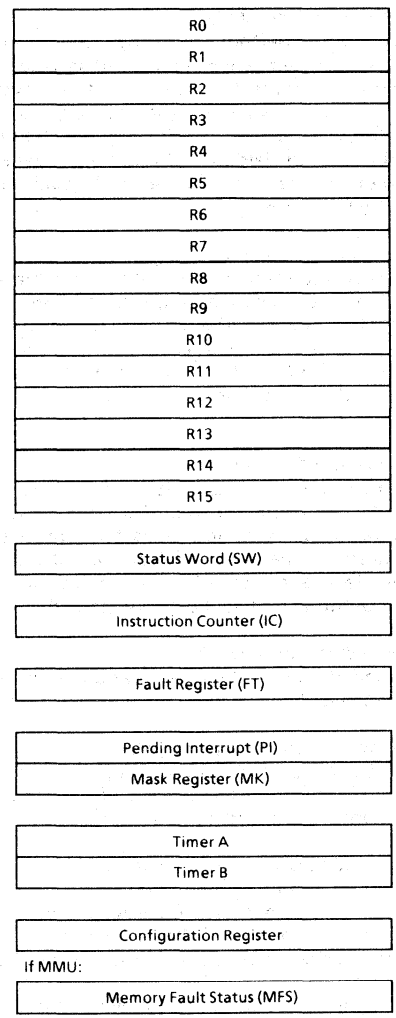


Figure 3. Register Set Model

5.2.3 Memory Indirect (I,IX)
Memory Indirect (without indexing) is an addressing mode in which the memory address (A) specified by the instruction contains the address of the required operand. In Memory Indirect (pre-indexed), the sum of the contents of a specified index register (RX) and the instruction address field (A) is the address of the address of the required operand. Registers R1 through R15 may be specified for indexing.

5.2.4 Immediate Long (IM)
There are two formats that implement Immediate Long Addressing; one allows indexing and one does not. For the indexable format, if the specified index register (RX) is not equal to zero, the contents of RX are added to the immediate field to form the required operand, otherwise, the immediate field contains the required operand.

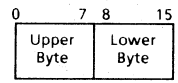
5.2.5 Immediate Short (IS)
In this mode the required 4-bit operand is contained within the 16-bit instruction. The Immediate Short addressing mode accommodates two formats; one which interprets the contents of the immediate field as positive data and the other which interprets the contents of the immediate field as negative data.

5.2.6 Immediate Short Positive (ISP)
The immediate operand is treated as a positive integer between 1 and 16.

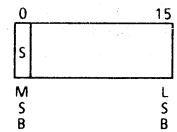
5.2.7 Immediate Short Negative (ISN)
The immediate operand is treated as a negative integer between 1 and 16. Its internal form is a two's complement, sign-extended 16-bit number.

5.2.8 Instruction Counter Relative (ICR)
This addressing mode is used for 16-bit branch instructions. The contents of the instruction counter minus two (the address of the current instruction) is added to the sign-extended 8-bit displacement field (D) within the instruction. This sum then points to the memory address to which control may be transferred if a branch is to be taken.

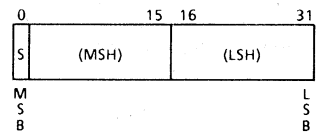
Byte



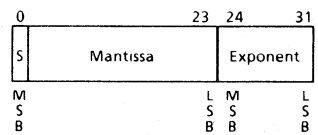
Single-Precision Fixed-Point



Double-Precision Fixed-Point



Floating-Point



Extended-Precision Floating-Point

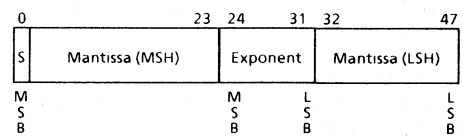
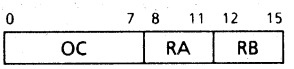
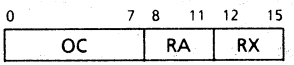
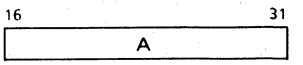
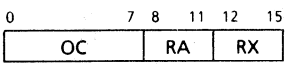
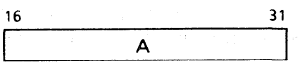
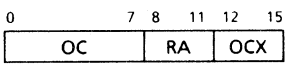
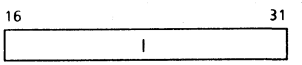
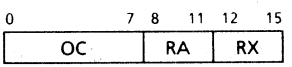
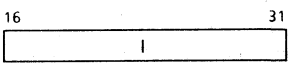
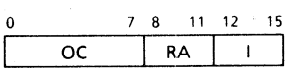
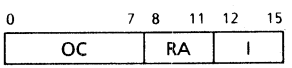
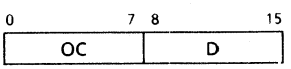
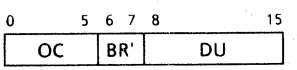
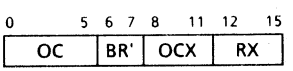
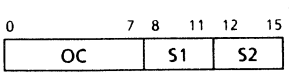


Figure 4. Data Formats

Mode	Format
1. Register Direct "R"	
2. Memory Direct "D" "DX"	  RX = 0 (Non-Indexed) RX ≠ 0 (Indexed)
3. Memory Indirect "I" "IX"	  RX = 0 (Non-Indexed) RX ≠ 0 (Indexed)
4. Immediate Long a. Not Indexable "IM"	 
b. Indexable "IM" "IMX"	  RX = 0 (Non-Indexed) RX ≠ 0 (Indexed)
5. Immediate Short a. Positive "ISP"	
b. Negative "ISN"	
6. IC Relative "ICR"	
7. Base Relative a. Not Indexable "B"	 BR' = BR-12
b. Indexable "B" "BX"	 RX = 0 (Non-Indexed) RX ≠ 0 (Indexed)
8. Special "S"	

Legend:

OC	=	Operation Code
RA	=	Destination Register
RB	=	Source Register
RX	=	Index Register
A	=	Address (Logical)
OCX	=	Extension to Operation Code
I	=	Immediate Data
D	=	Displacement
BR'	=	Base Register Reference
DU	=	Displacement (Positive)
S1, S2	=	Special Code

Figure 5. Addressing Modes

5.2.9 Base Relative (B)

There are two formats which implement Base Relative Addressing; one allows indexing and one does not. For the non-indexable form the contents of the instruction specified base register (BR = BR' + 12) is added to the 8-bit displacement field (DU) of the 16-bit instruction. For the indexable form, the sum of the contents of a specified index register (RX) and a specified base register (BR = BR' + 12) is the address of the required operand. Registers R1 through R15 may be specified for indexing and the base register may be R12 through R15.

5.2.10 Special (S)

This addressing mode is applicable to instructions that do not follow the above formats.

5.3 Benchmarking

Table 6a defines the number and type of machine cycles associated with each MIL-STD-1750A instruction. This information may be used when benchmarking MAS281 performance. The Digital Avionics Instruction Set (DAIS) mix, which defines a typical frequency of occurrence for MIL-STD-1750A instructions, is used here for this purpose.

One problem with the DAIS mix, however, is that it does not reflect the impact of data dependencies on system performance. For example, a multiplication in which one operand is zero may be performed much faster than one with two non-zero operands. Also, the DAIS mix does not specify such time consuming operations as normalization and alignment.

Realistic benchmarks must therefore take both an instruction mix and data dependencies into account. To this end, machine cycle counts in Table 6a which have data dependencies are annotated with either an "a" suffix to reflect an average number of machine cycles (where each of several possibilities is equally likely) or with a "wa" suffix to reflect a weighted average number of machine cycles (where some data possibilities are more likely than others). Weighted averages are only applicable to floating-point operations.

Weighted averages provided in Table 6a, based on the Sweeney (IBM Systems Journal, Vol. 4, No. 1, 1965) guidelines, take a wide range of data dependencies into consideration. Normalization and alignment operations are also represented. Table 5 defines MAS281 throughput, at various frequencies and wait states, for the DAIS mix using Sweeney data dependencies.

It should be noted that using the Sweeney guidelines is a conservative approach to benchmarking. If best case assumptions are made and such operations as normalization and alignment are not considered, MAS281 performance figures are approximately 50% higher than those indicated in Table 5.

f_{OSC} MHz	0	1	2	3
25	743.4	698.3	658.4	622.8
20	594.7	558.7	526.7	498.2
15	446.0	419.0	395.0	373.7
10	297.4	279.3	263.4	249.1

Number of Wait States in Memory Access Cycle

Table 5. Throughput (KIPS)

5.4 Instruction Summary

Operation	Op Code/Ext	Mnemonic	Format	Cycles *		
				M	P	B
LOAD/STORE						
Single Precision Load	81	LR	R	1	0	0
	0X	LB	B	2	1	0
	4X 0	LBX	BX	2	1	0
	82	LISP	ISP	1	0	0
	83	LISN	ISN	1	0	0
	80	L	D,DX	3	0	0
	85	LIM	IM,IMX	2	0	0
	84	LI	I,IX	4	1	0
Double-Precision Load	87	DLR	R	1	2	0
	0X	DLB	B	3	1	0
	4X 1	DLBX	BX	3	2	0
	86	DL	D,DX	4	0	0
	88	DLI	I,IX	5	1	0
Single-Precision Store	0X	STB	B	2	2	0
	4X 2	STBX	BX	2	2	0
	90	ST	D,DX	3	1	0
	94	STI	I,IX	4	1	0
Store a Non-Negative Constant	91	STC	D,DX	3	1	0
	92	STCI	I,IX	4	1	0
Double-Precision Store	0X	DSTB	B	3	2	0
	4X 3	DSTX	BX	3	2	0
	96	DST	D,DX	4	0	0
	98	DSTI	I,IX	5	1	0
Load Multiple Registers	89	LM	D,DX	3 + n	1	1
Store Multiple Registers	99	STM	D,DX	3 + n	1	1
INTEGER ARITHMETIC						
Single-Precision Integer Add	A1	AR	R	1	1	0
	1X	AB	B	2	2	0
	4X 4	ABX	BX	2	2	0
	A2	AISP	ISP	1	1	0
	A0	A	D,DX	3	1	0
	4A 1	AIM	IM	2	1	0
Increment Memory by a Positive Integer	A3	INCM	D,DX	4	1	0
Single-Precision Absolute Value of Register	A4	ABS	R	1	1.5	1a
Double-Precision Absolute Value of Register	A5	DABS	R	1	2.5	1a

*M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles),
a = average if more than one alternative exists

Table 6a. Instruction Summary

Operation	Op Code/Ext	Mnemonic	Format	Cycles *		
				M	P	B
Double-Precision Integer Add	A7	DAR	R	1	3	0
	A6	DA	D,DX	4	1	0
Single Precision Integer Subtract	B1	SR	R	1	1	0
	1X	SBB	B	2	2	0
	4X 5	SBBX	BX	2	2	0
	B2	SISP	ISP	1	1	0
	B0	S	D,DX	3	1	0
	4A 2	SIM	IM	2	1	0
Decrement Memory by a Positive Integer	B3	DECM	D,DX	4	1	0
Single Precision Negate Register	B4	NEG	R	1	1	0
Double-Precision Negate Register	B5	DNEG	R	1	3	0
Double-Precision Integer Subtract	B7	DSR	R	1	3	0
	B6	DS	D,DX	4	1	0
Single Precision Integer Multiply with 16-Bit Product	C1	MSR	R	1	6.5	4a
	C2	MISP	ISP	1	7.5	4a
	C3	MISN	ISN	1	7.5	4a
	C0	MS	D,DX	3	6.5	4a
	4A 4	MSIM	IM	2	6.5	4a
Single Precision Integer Multiply with 32-Bit Product	C5	MR	R	1	5	3
	1X	MB	B	2	7	3
	4X 6	MBX	BX	2	7	3
	C4	M	D,DX	3	5	3
	4A 3	MIM	IM	2	5	3
Double-Precision Integer Multiply	C7	DMR	R	1	41	4.5a
	C6	DM	D,DX	4	40	4.5a
Single Precision Integer Divide with 16-Bit Dividend	D1	DVR	R	1	20.25	5.5a
	D2	DISP	ISP	1	20	5.5a
	D3	DISN	ISN	1	20.5	5.5a
	D0	DV	D,DX	3	20.25	5.5a
	4A 6	DVIM	IM	2	20.25	5.5a
Single Precision Integer Divide with 32-Bit Dividend	D5	DR	R	1	21.75	6.5a
	1X	DB	R	2	22.75	6.5a
	4X 7	DBX	BX	2	22.75	6.5a
	D4	D	D,DX	3	21.75	6.5a
	4A 5	DIM	IM	2	22.75	6.5a
Double-Precision Integer Divide	D7	DDR	R	1	79.5	5.5a
	D6	DD	D,DX	4	77.5	5.5a

*M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles),
a = average if more than one alternative exists

Table 6a (continued). Instruction Summary

Operation	Op Code/Ext	Mnemonic	Format	Cycles *		
				M	P	B
LOGICAL						
Inclusive Logical OR	E1	ORR	R	1	0	0
	3X	ORB	B	2	1	0
	4X F	ORBX	BX	2	1	0
	E0	OR	D,DX	3	0	0
	4A 8	ORIM	IM	2	0	0
Logical AND	E3	ANDR	R	1	0	0
	3X	ANDB	B	2	1	0
	4X E	ANDX	BX	2	1	0
	E2	AND	D,DX	3	0	0
	4A 7	ANDM	IM	2	0	0
Exclusive Logical OR	E5	XORR	R	1	0	0
	E4	XOR	D,DX	3	0	0
	4A 9	XORM	IM	2	0	0
Logical NAND	E7	NR	R	1	1	0
	E6	N	D,DX	3	1	0
	4A B	NIM	IM	2	1	0
Set Bit	51	SBR	R	1	0	0
	50	SB	D,DX	4	1	0
	52	SBI	I,IX	5	2	0
Reset Bit	54	RBR	R	1	1	0
	53	RB	D,DX	4	1	0
	55	RBI	I,IX	5	2	0
Test Bit	57	TBR	R	1	0	0
	56	TB	D,DX	3	0	0
	58	TBI	I,IX	4	1	0
Test and Set Bit	59	TSB	D,DX	4	0	2
Set Variable Bit in Register	5A	SVBR	R	1	0	1
Reset Variable Bit in Register	5C	RVBR	R	1	1	1
Test Variable Bit in Register	5E	TVBR	R	1	0	1
Store Register Through Mask	97	SRM	D,DX	4	3	0
BYTE						
Load From Upper Byte	8B	LUB	D,DX	3	0	0
	8D	LUBI	I,IX	4	1	0
Load From Lower Byte	8C	LLB	D,DX	3	1	0
	8E	LLBI	I,IX	4	2	0
Store Into Upper Byte	9B	STUB	D,DX	4	1	0
	9D	SUBI	I,IX	5	3	0
Store Into Lower Byte	9C	STLB	D,DX	4	1	0
	9E	SLBI	I,IX	5	2	0
Exchange Bytes in Register	EC	XBR	S	1	0	1

*M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles),

Table 6a (continued). Instruction Summary

Operation	Op Code/Ext	Mnemonic	Format	Cycles *		
				M	P	B
COMPARE						
Single-Precision Compare	F1	CR	R	1	0	0
	3X	CB	B	2	1	0
	4X C	CBX	BX	2	1	0
	F2	CISP	ISP	1	0	0
	F3	CISN	ISN	1	0	0
	F0	C	D,DX	3	0	0
	4A A	CIM	IM	2	0	0
Compare Between Limits	F4	CBL	D,DX	4	2.75	1.75a
Double-Precision Compare	F7	DCR	R	1	2	0
	F6	DC	D,DX	4	0	0
JUMP/BRANCH						
Jump on Condition	70	JC	D,DX	2	0.5	1a
	71	JCI	I,IX	3	0.5	1a
Jump to Subroutine	72	JS	D,DX	2	2	0
Subtract One and Jump	73	SOJ	D,DX	2	2.5	1a
Branch Unconditionally	74	BR	ICR	2	2	0
Branch if Equal to (Zero)	75	BEZ	ICR	1.5	1	1a
Branch if Less than (Zero)	76	BLT	ICR	1.5	1	1a
Branch to Executive	77	BEX	S	16	12	3a
Branch if Less than or Equal to (Zero)	78	BLE	ICR	1.5	1	1a
Branch if Greater than (Zero)	79	BGT	ICR	1.5	1	1a
Branch if Not Equal to (Zero)	7A	BNZ	ICR	1.5	1	1a
Branch if Greater than or Equal to (Zero)	7B	BGE	ICR	1.5	1	1a
SHIFT						
Shift Left Logical	60	SLL	R	1	1	0
Shift Right Logical	61	SRL	R	1	1	0
Shift Right Arithmetic	62	SRA	R	1	1	0
Shift Left Cyclic	63	SLC	R	1	1	0
Double Shift Left Logical	65	DSLL	R	1	3	0
Douible Shift Right Logical	66	DSRL	R	1	2	0
Double Shift Right Arithmetic	67	DSRA	R	1	2	0
Double Shift Left Cyclic	68	DSLC	R	1	3	0
Shift Logical, Count in Register	6A	SLR	R	1	1	3
Shift Arithmetic, Count in Register	6B	SAR	R	1	1.5	3.50a
Shift Cyclic, Count in Register	6C	SCR	R	1	1	3.25a
Double Shift Logical, Count in Register	6D	DSLR	R	1	2.25	4a
Double Shift Arithmetic, Count in Register	6E	DSAR	R	1	3.19	4.94a
Double Shift Cyclic, Count in Register	6F	DSCR	R	1	3.5	3a

*M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles),
a = average if more than one alternative exists

Table 6a (Continued). Instruction Summary

Operation	Op Code/Ext	Mnemonic	Format	Cycles *		
				M	P	B
CONVERT						
Convert Floating-Point to 16-Bit Integer	E8	FIX	R	1	4.25	4.5a
Convert 16-Bit Integer to Floating-Point	E9	FLT	R	1	3	2a
Convert Extended-Precision Floating-Point to 32-Bit Integer	EA	EFIX	R	1	12.25	6.25a
Convert 32-Bit Integer to Extended-Precision Floating-Point	EB	EFLT	R	1	7.5	3.5a
STACK						
Stack IC and Jump to Subroutine	7E	SJS	D,DX	4	3	0
Unstack IC and return from Subroutine	7F	URS	S	3	1	1
Pop Multiple registers off the Stack	8F	POPM	S	2.5 + n (n = 0 to 15)	2.25 + n (n = 0 to 15)	4.25a
Push Multiple Registers onto the Stack	9F	PSHM	S	1 + n (n = 0 to 15)	4.5 + n (n = 0 to 15)	2a
I/O (See I/O Command Summary)						
Execute I/O	48	XIO**	IM,IMX	3	3.583	6.277a
Vectored I/O	49	VIO**	D,DX	-	-	-
SPECIAL						
Built-In Function Call	4F	BIF	S			
Move Multiple Words, Memory-to-Memory	93	MOV	S	1 + 4n	1 + 3n	1 + 2na
Exchange Words in Registers	ED	XWR	R	1	2	0
Load Status	7D	LST**	D,DX	8	2	3
	7C	LSTI**	I,IX	9	2	4
No Operation	FF	NOP	S	1	2	2
Break Point	FF	BPT	S	3	4	4

*M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles),
a = average if more than one alternative exists
** Privileged instruction.

Table 6a (Continued). Instruction Summary

Operation	Op Code/Ext	Mnemonic	Format	Cycles *		
				M	P	B
FLOATING-POINT						
Extended-Precision Floating-Point Load	8A	EFL	D,DX	5	0	1
Extended-Precision Floating-Point Store	9A	EFST	D,DX	5	0	1
Floating-Point Absolute Value of Register	AC	FABS	R	1	1.75	3.25a
Floating-Point Negate Register	BC	FNEG	R	1	3.25	3.75a
Floating-Point Compare	F9	FCR	R	1	2.75	2.875wa
	3X	FCB	B	2	2.75	2.875wa
	4X D	FCBX	BX	2	2.75	2.875wa
	F8	FC	D,DX	3	1.75	2.875wa
Extended-Precision Floating-Point Compare	FB	EFCR	R	1	3.25	2.875wa
	FA	EFC	D,DX	4.25a	2.75	2.875wa
Floating-Point Add	A9	FAR	R	1	7.625	8.25wa
	2X	FAB	B	3	6.625	8.25wa
	4X 8	FABX	BX	3	6.625	8.25wa
	A8	FA	D,DX	4	5.625	8.25wa
Extended-Precision Floating-Point Add	AB	EFAR	R	1	21.3125	10.5625wa
	AA	EFA	D,DX	5	19.3125	10.5625wa
Floating-Point Subtract	B9	FSR	R	1	8.625	8.625wa
	2X	FSB	B	3	7.625	8.625wa
	4X 9	FSBX	BX	3	7.625	8.625wa
	B8	FS	D,DX	4	6.625	8.625wa
Extended-Precision Floating-Point Subtract	BB	EFSR	R	1	23.0625	11.8125wa
	BA	EFS	D,DX	5	21.0625	11.8125wa
Floating-Point Multiply	C9	FMR	R	1	12.75a	6.25wa
	2X	FMB	B	3	12.75a	6.25wa
	4X A	FMBX	BX	3	12.75a	6.25wa
	C8	FM	D,DX	4	11.75a	6.25wa
Extended-Precision Floating-point Multiply	CB	EFMR	R	1	59.75	6.25wa
	CA	EFM	D,DX	5	57.75	6.25wa
Floating-Point Divide	D9	FDR	R	1	31.5	32.75wa
	2X	FDB	B	3	30.5	32.75wa
	4X B	FDBX	BX	3	30.5	32.75wa
	D8	FD	D,DX	4	29.5	32.75wa
Extended-Precision Floating-Point Divide	DB	EFDR	R	1	102.625	47.875wa
	DA	EFD	D,DX	5	100.625	47.875wa

*M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles),
a = average if more than one alternative exists
wa = weighted average favouring one or more possible alternatives

Table 6a (Continued). Instruction Summary

4.5 Internal I/O Command Summary

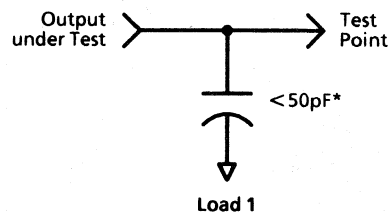
Operation	Command Code (Hex)	Mnemonic	Cycles *		
			M	P	B
Implemented in MAS281					
Set Fault Register	0401	SFR	2	3	9
Set Interrupt Mask	2000	SMK	2	3	9
Clear Interrupt request	2001	CLIR	2	3	9
Enable Interrupts	2002	ENBL	2	3	9
Disable Interrupts	2003	DSBL	2	3	9
Reset Pending Interrupt	2004	RPI	2	3	9
Set Pending Interrupt Register	2005	SPI	2	3	9
Reset Normal Power Up Discrete	200A	RNS	2	3	9
Write Status Word	200E	WSW	2	3a	8.5a
Enable Start-Up ROM	4004	ESUR	2	3	9
Disable Start-Up ROM	4005	DSUR	2	3	9
Direct Memory Access Enable	4006	DMAE	2	3	9
Direct Memory Access Disable	4007	DMAD	2	3	9
Timer A Start	4008	TAS	2	3	9
Timer A Halt	4009	TAH	2	3	9
Output Timer A	400A	OTA	2	3	9
Reset Trigger-Go	400B	GO	2	3	9
Timer B Start	400C	TBS	2	3	9
Timer B Halt	400D	TBH	2	3	9
Output Timer B	400E	OTB	2	3	9
Read Configuration Word	8400	RCW	2	2	4
Read Fault Register Without Clear	8401	RFR	2	2	4
Read Interrupt Mask	A000	RMK	2	2	4
Read Pending Interrupt Register	A004	RPIR	2	2	4
Read Status Word	A00E	RSW	2	1	4
Read and Clear Fault Register	A00F	RCFR	2	2	4
Input Timer A	C00A	ITA	2	2	4
input Timer B	C00E	ITB	2	2	4
Implemented in BPU					
Memory Protect Enable	4003	MPEN	2	4	8
Load Memory Protect RAM	50XX	LMP	2	4	8
Read Memory Protect RAM	D0XX	RMP	2	3	3
Implemented in MMU					
Write Instruction Page Register	51XY	WIPR	2	4	8
Write Operand Page Register	52XY	WOPR	2	4	8
Read Memory Fault Status	A00D	RMFS	2	3	3
Read Instruction Page Register	D1XY	RIPR	2	3	3
Read Operand Page Register	D2XY	ROPR	2	3	3

*M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles),
a = average if more than one alternative exists

Table 6b. Internal I/O Command Summary

6.0 Timing Characteristics

This section provides the detailed timing specifications for the MA17502. Figure 6 depicts the test load used to obtain timing data. Figures 7 through 9 depict the timing waveforms associated with various MA17502 signals. Table 7 provides values for parameters specified in the timing waveforms. All timing values provided in Table 7 are valid over the full military temperature range (-55°C to + 125°C), and are measured from 50% point to 50% point (50% of VDD supply voltage, unless otherwise specified). Crosshatching in Figure 7 indicates either a "don't care" or indeterminate state.



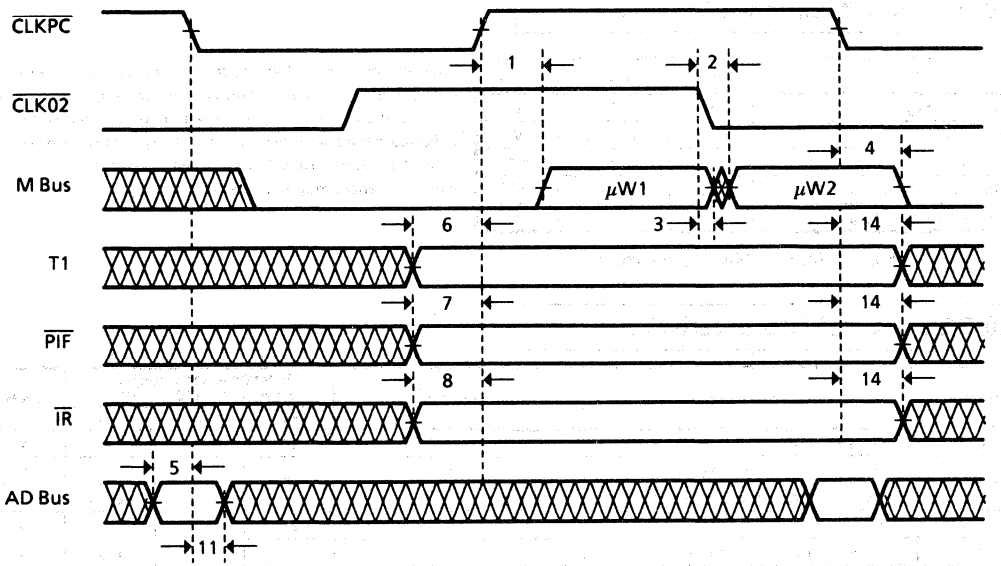
* Includes all jig and parasitic capacitance.

Figure 6. Test Load

No	Parameter	Test Condition(1)(2)	Min	Max	Units
1	$\overline{CLKPC}$ ↑ to Microword 1 Valid	Load 1	-	95	ns
2	$\overline{CLK02}$ ↓ to Microword 2 Valid	Load 1	-	41	ns
3	Microword 1 after $\overline{CLK02}$ ↓	Load 1	5	-	ns
4	Microword 2 after $\overline{CLKPC}$ ↓	Load 1	14	-	ns
5	AD Bus to $\overline{CLKPC}$ ↓	-	20	-	ns
6	$\overline{T1}$ to $\overline{CLKPC}$ ↑	-	46	-	ns
7	$\overline{PIF}$ to $\overline{CLKPC}$ ↑	-	56	-	ns
8	$\overline{IR}$ to $\overline{CLKPC}$ ↑	-	47	-	ns
9	HOLD to $\overline{CLKPC}$ ↓	-	30	-	ns
10	RESET to $\overline{CLKPC}$ ↓	-	30	-	ns
11	AD Bus after $\overline{CLKPC}$ ↓	-	15	-	ns
12	HOLD after $\overline{CLKPC}$ ↓	-	15	-	ns
13	RESET after $\overline{CLKPC}$ ↓	-	15	-	ns
14	T1, PIF, IR after $\overline{CLKPC}$ ↓	-	0	-	ns

Notes:
(1) T_A = + 25°C, - 55°C and + 125°C tested at VDD = 4.5V and 5.5V
(2) Unless otherwise noted: VIL ≥ 0.0V, VIHTTL ≤ 4.0V;
timing measured from 50% to 50% point.

Table 7a. Timing Parameter Values



Note ROMONLY and CS are pulled up to VDD

Figure 7. Basic Timing

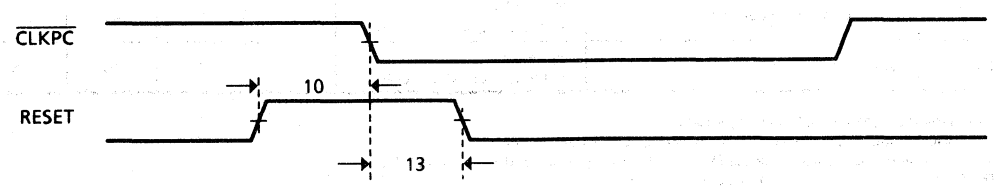


Figure 8. RESET Timing

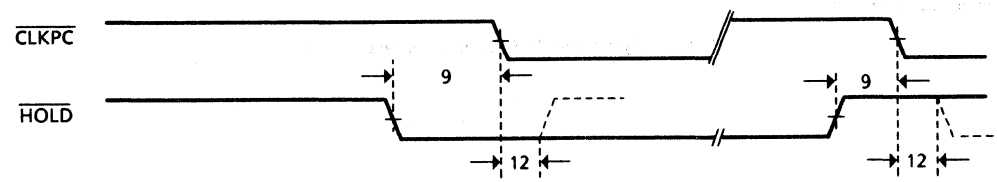


Figure 9. HOLD Timing

7.0 Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply voltage	-0.5	7	V
Input voltage	-0.3	V_{DD} + 0.3	V
Current through any pin	-20	20	mA
Operating temperature	-55	125	°C
Storage temperature	-65	150	°C

Table 8. Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8.0 DC Electrical Characteristics

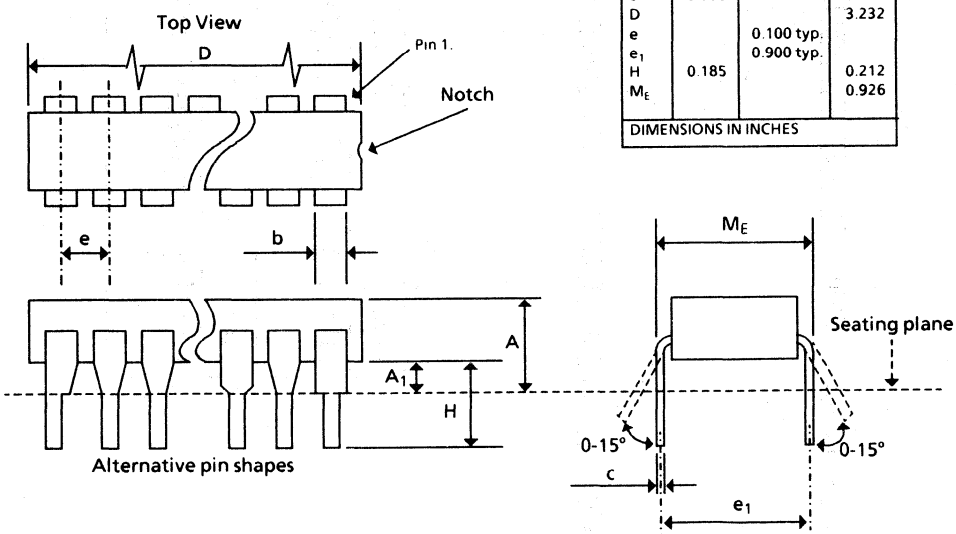
Symbol	Parameter	Condition	Total Dose Radiation Not Exceeding $3x10^5$ RAD (Si)			Units
			Min.	Typ.	Max.	
V_{DD}	Supply voltage	V_{SS} = 0	4.5	5.0	5.5	V
V_{IHC}	CMOS Input High Voltage (Note 1)	-	V_{DD}-1	-	-	V
V_{ILC}	CMOS Input Low Voltage (Note 1)	-	-	-	V_{SS} + 1	V
V_{IHT}	TTL Input High Voltage (Note 2)	-	2.0	-	-	V
V_{ILT}	TTL Input Low Voltage (Note 2)	-	-	-	0.8	V
V_{OHC}	CMOS Output High Voltage (Note 1)	I_{OH} = -1.4mA, V_{DD} = 4.5V	4.0	-	-	V
V_{OLC}	CMOS Output Low Voltage (Note 1)	I_{OL} = 2.0mA, V_{DD} = 5.5V	-	-	0.5	V
I_I	Input Leakage Current (Note 3)	V_{DD} = 5.5V, V_{IN} = 0V or 5.5V	-	-	±10	uA
I_{OZ}	Output Leakage Current (Note 3)	V_{DD} = 5.5V, V_O = 0V or 5.5V	-	-	±50	uA
I_{IPU}	CS and ROMONLYN Input Pull-up Current (Note 4)	V_{DD} = 5.5V, CS or ROMONLYN = 0V	-	-	-300	uA
I_{DDOP}	Operating Supply Current	V_{DD} = 5.5V, CLKPCN = CLK02N = 4MHz	-	25	40	mA
I_{DDST}	Static Supply Current	V_{DD} = 5.5V, CLKPCN = CLK02N = 0MHz	-	5	10	mA

Notes:
1. The following signals are CMOS compatible:
   a. CMOS inputs: CS, ROMONLYN, T1, IRN, PIFN, CLKO2N and CLKPCN.
   b. CMOS I/O signals: Microcode bus (M00-M19) and Microcode address bus (CC00-CC11).
2. The following signals are TTL compatible:
   a. TTL inputs: Address/Data Bus (AD00-AD15), RESET and HOLDN.
3. Worst case at T_A = + 125°C, guaranteed but not tested at T_A = -55°C.
4. CS and ROMONLYN inputs are provided for future microcode expansion and have internal pull-up resitors. These signals should be high for normal operation.

Table 9. Operating DC Electrical Characteristics

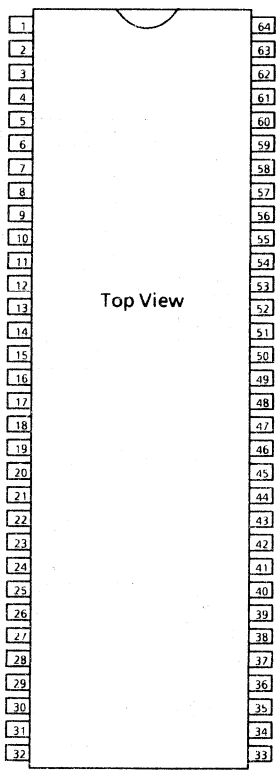
9.0 Packaging Information

Ceramic Dual-in-line - Package type C)



Ref.	Min.	Nom.	Max.
A			0.220
A_1	0.015		0.060
b	0.014		0.023
c	0.008		0.014
D			3.232
e		0.100 typ.	
e_1		0.900 typ.	
H	0.185		0.212
M_E			0.926
DIMENSIONS IN INCHES			

Figures 10a. Dimensioned Drawing

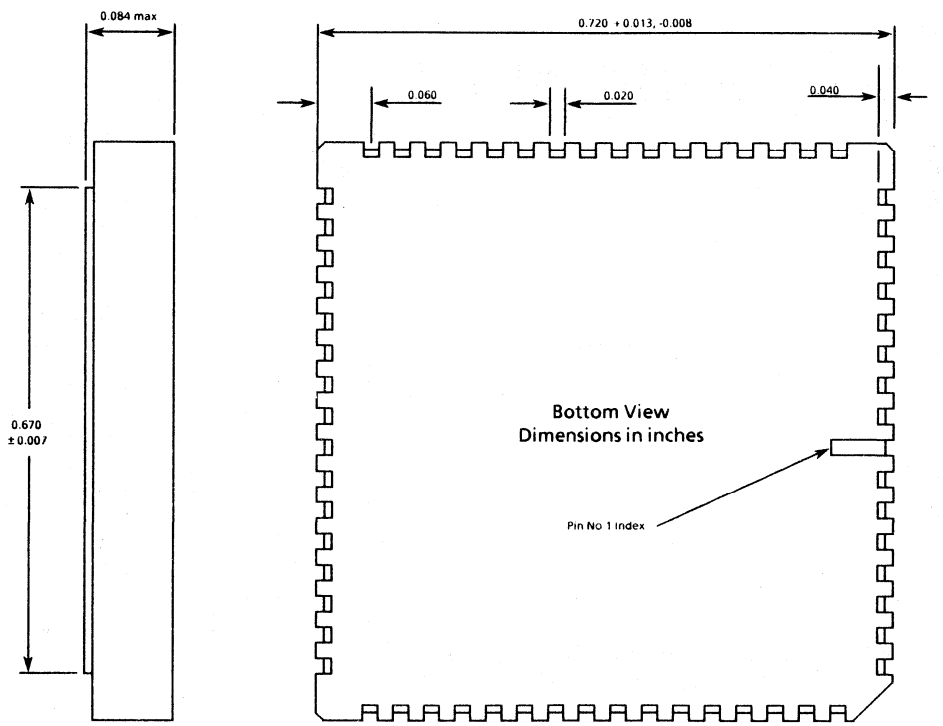


1	IRN	33	M08
2	VDD	34	NC
3	PIFN	35	M07
4	AD00	36	M06
5	AD01	37	M05
6	AD02	38	M04
7	AD03	39	M03
8	AD04	40	M02
9	AD05	41	M01
10	AD06	42	GND
11	AD07	43	CS
12	AD08	44	M00
13	AD09	45	CC00
14	AD10	46	CC01
15	AD11	47	CC02
16	AD12	48	CC03
17	AD13	49	CC04
18	AD14	50	CC05
19	AD15	51	CC06
20	CLK02N	52	CC07
21	CLKPCN	53	CC08
22	M19	54	CC09
23	M18	55	CC10
24	M17	56	CC11
25	M16	57	ROMONLYN
26	M15	58	NC
27	M14	59	GND
28	M13	60	NC
29	M12	61	NC
30	M11	62	T1
31	M10	63	RESET
32	M09	64	HOLDN

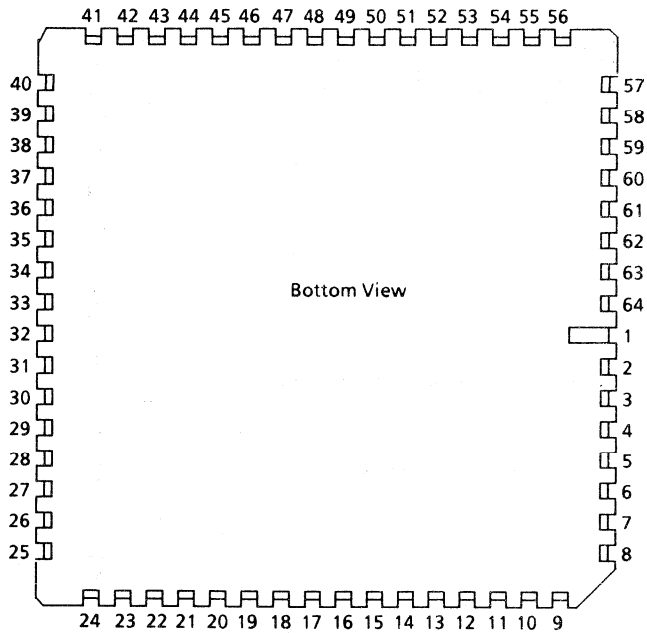
Figures 10b. Pin Assignments

MA17502
Radiation Hard MIL-STD-1750A Control Unit

Leadless Chip Carrier - Package type L



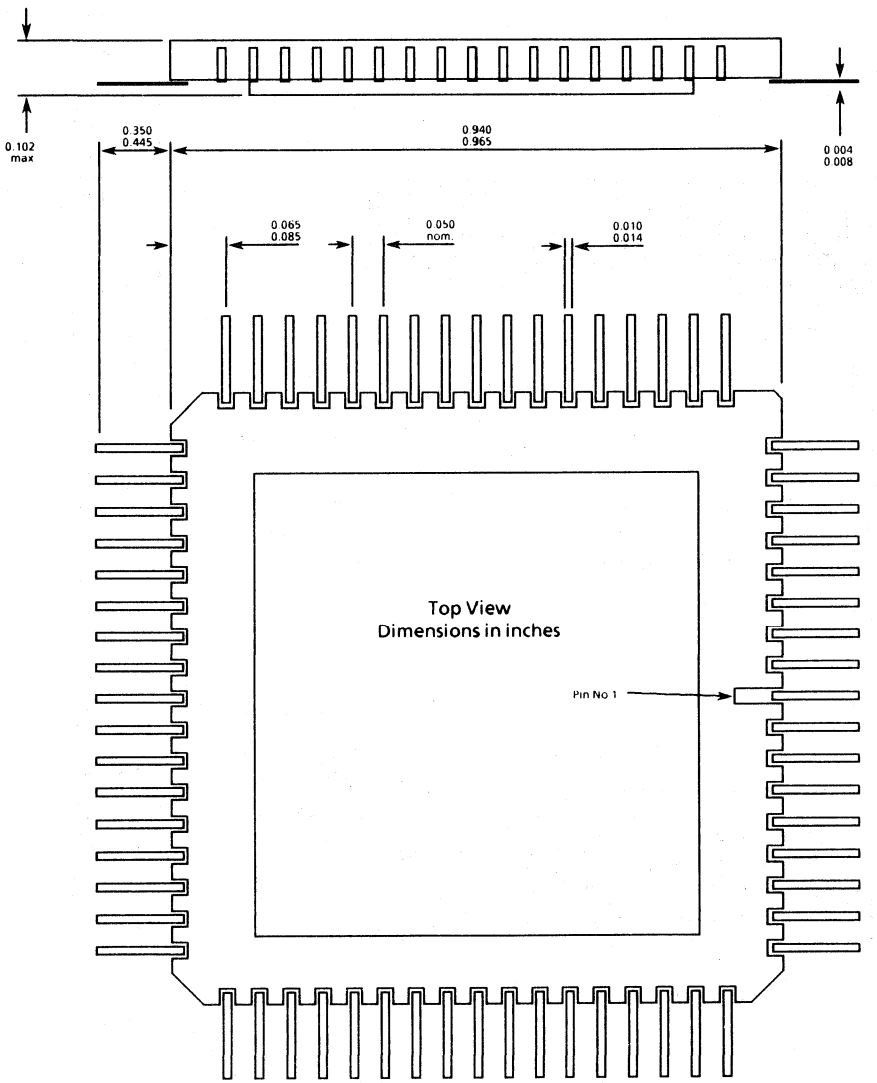
Figures 11a. Dimensioned Drawing



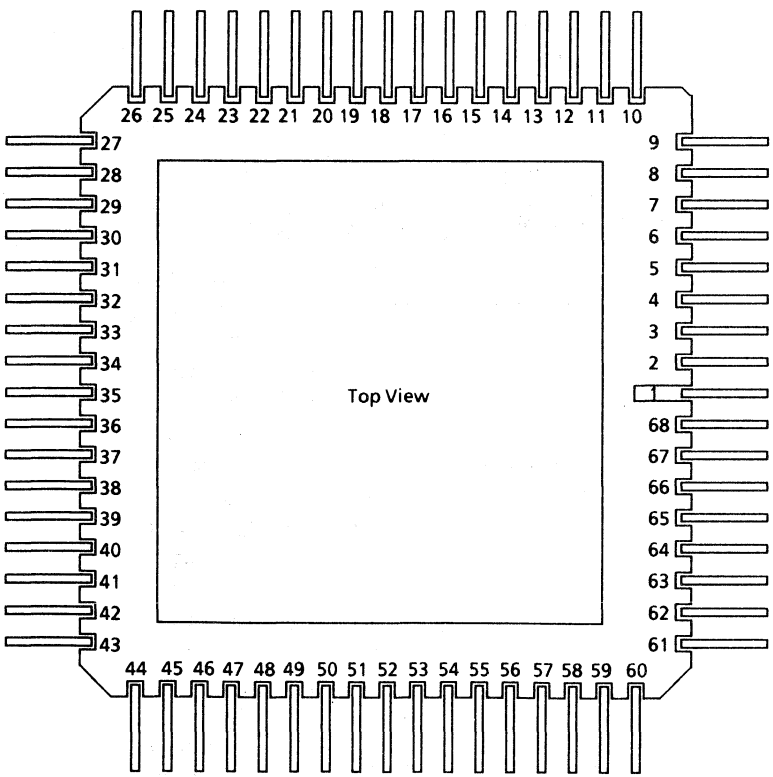
1	IRN	33	M08
2	VDD	34	NC
3	PIFN	35	M07
4	AD00	36	M06
5	AD01	37	M05
6	AD02	38	M04
7	AD03	39	M03
8	AD04	40	M02
9	AD05	41	M01
10	AD06	42	GND
11	AD07	43	CS
12	AD08	44	M00
13	AD09	45	CC00
14	AD10	46	CC01
15	AD11	47	CC02
16	AD12	48	CC03
17	AD13	49	CC04
18	AD14	50	CC05
19	AD15	51	CC06
20	CLK02N	52	CC07
21	CLKPCN	53	CC08
22	M19	54	CC09
23	M18	55	CC10
24	M17	56	CC11
25	M16	57	ROMONLYN
26	M15	58	NC
27	M14	59	GND
28	M13	60	NC
29	M12	61	NC
30	M11	62	T1
31	M10	63	RESET
32	M09	64	HOLDN

Figures 11b. Pin Assignments

Topbraze Flatpack - Package type F



Figures 12a. Dimensioned Drawing



1	IRN
2	NC
3	VDD
4	PIFN
5	AD00
6	AD01
7	AD02
8	AD03
9	AD04
10	AD05
11	AD06
12	AD07
13	AD08
14	AD09
15	AD10
16	AD11
17	AD12
18	AD13
19	AD14
20	AD15
21	CLK02N
22	CLKPCN
23	M19
24	M18
25	M17
26	M16
27	M15
28	M14
29	M13
30	M12
31	M11
32	M10
33	M09
34	M08
35	NC
36	NC
37	M07
38	M06
39	M05
40	M04
41	M03
42	M02
43	M01
44	NC
45	GND
46	CS
47	M00
48	CC00
49	CC01
50	CC02
51	CC03
52	CC04
53	CC05
54	CC06
55	CC07
56	CC08
57	CC09
58	CC10
59	CC11
60	ROMONLYN
61	NC
62	GND
63	NC
64	NC
65	NC
66	11
67	RESET
68	HOLDN

Figures 12b. Pin Assignments

MA17502
Radiation Hard MIL-STD-1750A Control Unit

10.0 Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

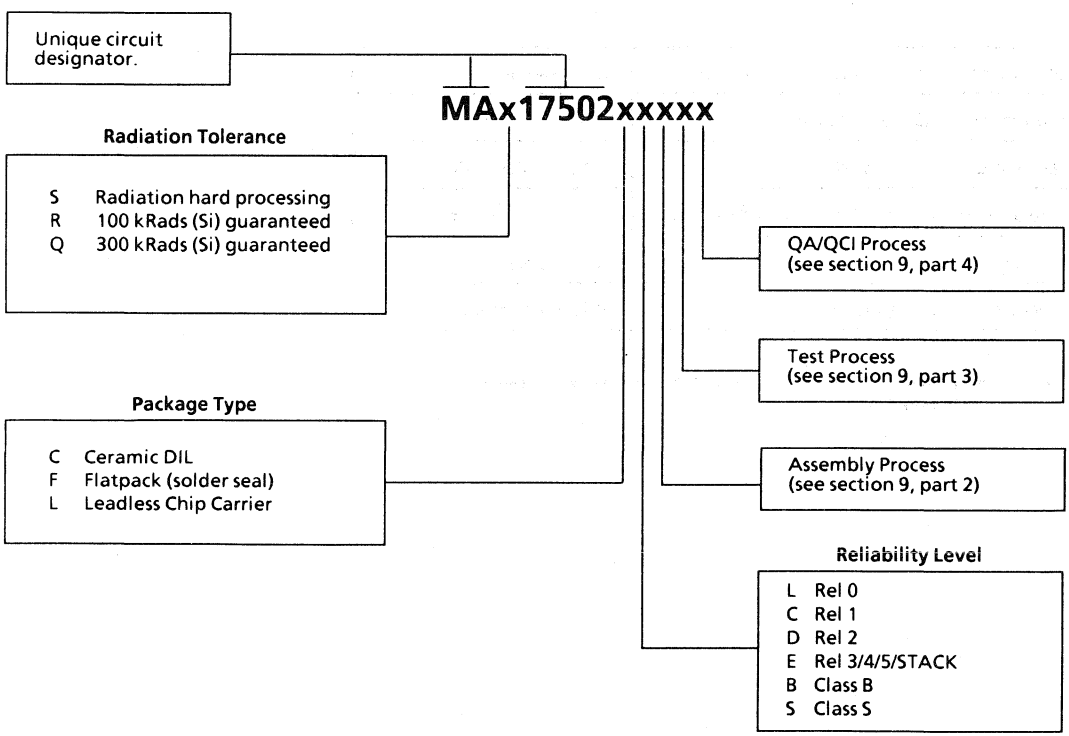
Total Dose (Function to specification, note 1)	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$1x10^{10}$ Rad(Si)/s
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/s
Neutron Hardness (Function to specification)	$1x10^{15}$ neutrons/cm2
Latch-up	Not possible
Single Event Upset (note 2)	$<10^{-10}$ errors/bit day

Note 1. Typical performance only, for guaranteed levels see ordering information.
2. GSO 10% Worst Case

GEC PLESSEY
SEMICONDUCTORS

11.0 Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



GEC PLESSEY

SEMICONDUCTORS

MA17503

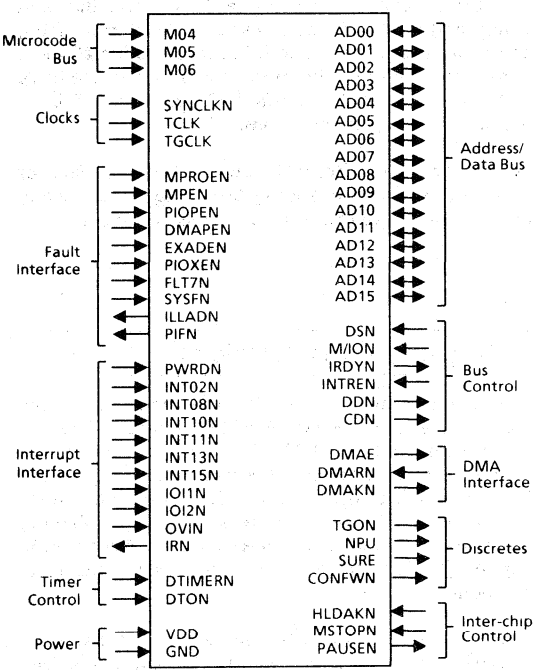
MIL-STD-1750A Interrupt Unit

S10209FDS Issue 1.4 November 1990

Features

- Mil-Std-1750A Instruction Set Architecture
- Full Performance over Military Temperature Range (-55°C to + 125°C)
- Radiation Hard CMOS/SOS Technology
- Interrupt Handler
  - 9 User Interrupt Inputs
  - Pending Interrupt Register
  - Interrupt Mask Register
  - Interrupt Priority Encoder
- Fault Handler
  - 8 User Faults Inputs
  - Fault Register
- Timers
  - Timer A
  - Timer B
- Trigger-Go
- DMA Interface
- Interface Discretes
  - Normal Power-Up
  - Start-Up ROM Enable
  - Configuration Word Enable
- Implements 26 MIL-STD-1750A Specified I/O Commands
- MAS281 Integrated Built-In Self Test
- TTL Compatible System Interface

Block Diagram



General Description

The MA17503 Interrupt Unit is a component of the Marconi Electronic Devices MAS281 chip set. Other chips in the set include MA17501 Execution Unit and the MA17502 Control Unit. Also available is the peripheral MA17504 Memory Management/Block Protection Unit. The Interrupt Unit, in conjunction with these additional chips, implements the full MIL-STD-1750A Instruction Set Architecture.

MA17503

MIL-STD-1750A Interrupt Unit

GEC PLESSEY

SEMICONDUCTORS

The MA17503 - consisting of the Pending Interrupt Register, Mask Register, Interrupt Priority Encoder, Fault Register, Timer A, Timer B, Trigger-Go Counter, Bus Fault Timer, and DMA interface - handles all interrupt fault, and DMA interfacing, in addition to providing all three hardware timers. The Interrupt Unit also implements 26 of the MIL-STD-1750A specified I/O commands. Table 1 provides brief signal definitions.

The MA17503 is offered in dual-in-line, flatpack or leadless chip carrier packaging. Screening and packaging options are described at the end of this document.

1.0 System Considerations

The MA17503 Interrupt Unit (IU) is a component of the Marconi Electronic Devices MAS281 chip set. This chip set implements the full MIL-STD-1750A instruction set architecture. Other chips in the set include the MA17501 Execution Unit (EU) and MA17502 Control Unit (CU). Also available is the peripheral MA17504 Memory Management Unit/Block Protection Unit (MMU(BPU)). Figure 1 depicts the relationship between the chip set components.

The IU provides the interrupt and fault handling interfaces for the chip set. The IU also provides the DMA control interface logic, contains interval Timers A and B, the Trigger-Go Counter, the Bus Fault Timeout timer, and decodes all MIL-STD-1750A specified I/O commands in support of these functions. The EU provides the arithmetic and logical computation resources for the chip set. The EU and IU are each controlled by microcode from the CU. The MMU(BPU) may be configured to provide either 1M-word memory management (MMU) or 1K-word memory block write protection (BPU) functions.

As shown in Figure 1, the MAS281 is the minimum processor configuration consisting of an Execution Unit, a Control Unit, and an Interrupt Unit. This configuration is capable of accessing a 64K-word address space. Addition of a MMU configured MA17504 allows access to a 1M-word address space. Addition of a BPU configured MA17504 provides hardware support for 1K-word memory block write protection.

Signal	I/O	Definition
AD00 - AD15	I/O/Z	16-Bit Address/Data Bus
M04, M05, M06	I	3 Bits of the Microcode Intruction Word
INTREN	I	Interrupt Unit Microcode Inerface Enable
DMAKN	O	DMA Request Acknowledge
DMAE	O	DMA Interface Enable
DMARN	I	DMA Request
M/ION	I	Memory/Input-Output
DSN	I	Data Strobe
SYNCLKN	I	Synchronisation Clock
IRDYN	O	Interrupt Unit Ready
DDN	O	Data Transceiver Direction Control
CDN	O	Control Bus Transceiver Direction Control
SYSFN	I	System Fault
FLT7N	I	Fault 7 (Undefined Fault)
PIOXEN	I	Programmed I/O Transfer Error
EXADEN	I	External Address Error
DMAPEN	I	DMA Parity Error
PIOPEN	I	Programmed I/O Parity Error
MPEN	I	Memory Parity Error
MPROEN	I	Memory Protection Error
ILLADN	O	Illegal Address
PIFN	O	Instruction Abort
PWRDN	I	Power-Down Interrupt
INT02N	I	Level 2 Interrupt
INT08N	I	Level 8 Interrupt
INT10N	I	Level 10 Interrupt
INT11N	I	Level 11 Interrupt
IOI1N	I	I/O Register Interrupt 1
INT13N	I	Level 13 Interrupt
IOI2N	I	I/O Register Interrupt 2
INT15N	I	Level 15 Interrupt
OV1N	I	Fixed-Point Overflow Interrupt
IRN	O	Interrupt Request
TCLK	I	Clock for Timers A and B
TGCLK	I	Trigger Go Timer Clock
DTIMERN	I	Disable Timers
DTON	I	Disable Bus-Fault Timeout
TGON	O	Trigger-Go Timer Overflow
NPU	O	Normal Power-up Indicator
SURE	O	Start-up ROM Enable
CONFWN	O	Configuration Word Enable
HLDAKN	I	Hold Acknowledge
MSTOPN	I	Microcode Stop
PAUSE	O	Processor Pause
VDD	I	Power
GND	I	Ground

Table 1. Signal Definitions

MA17503
MIL-STD-1750A Interrupt Unit

The IU, as with all components of the MAS281 chip set, is fabricated with Marconi Electronic Devices' CMOS/SOS process technology.

Detailed descriptions of the IUs companion chips are provided in separate data sheets. Additional discussions on chip set system considerations, interconnection details, and Digital Avionics Instruction Set (DAIS) mix benchmarking analysis are provided in separate application notes.

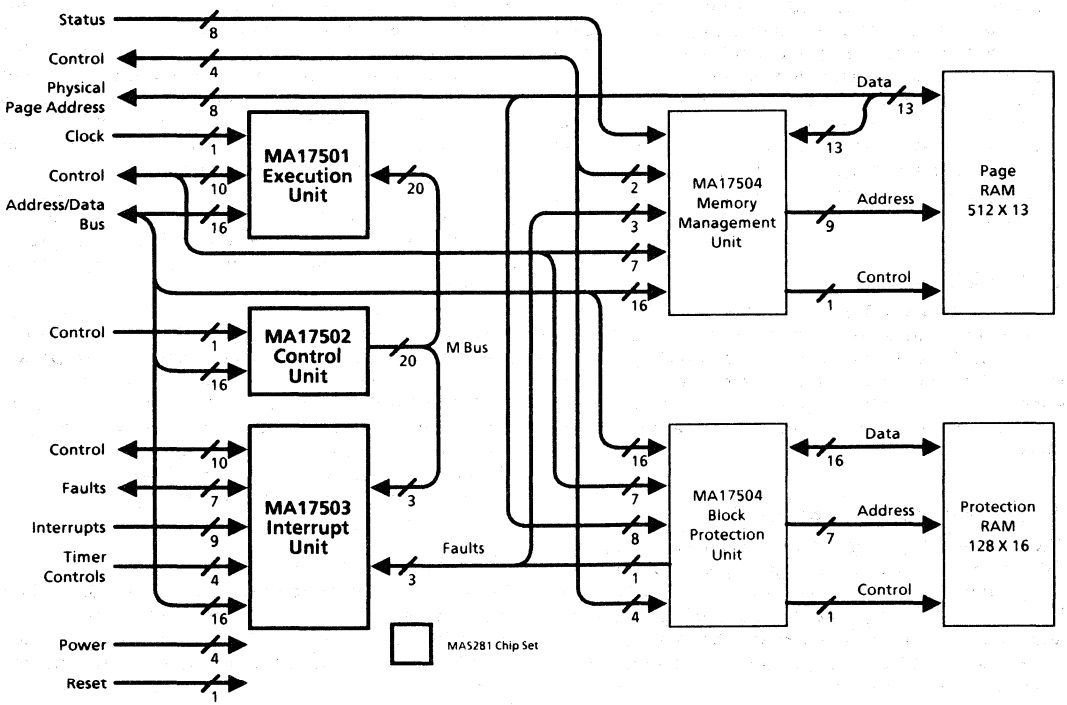


Figure 1. MAS281 Chip Set with Optional MA17504s and Support RAMs

2.0 Architecture

The Interrupt Unit consists of a Pending Interrupt Register, Mask Register, Interrupt Priority Encoder, Fault Register, two interval timers, two watchdog timers, DMA Control interface, and both microcode and internal I/O instruction decode logic. Details of these components are depicted in Figure 2 and are discussed below:

2.1 Pending Interrupt Register

The Pending Interrupt Register (PI) is the dedicated 16-bit register that latches all pending interrupt requests and stores them until serviced. The inputs to the PI are buffered by falling-edge detectors to prevent repeat latching of interrupt requests held low longer than required. The PI supports nine external interrupts inputs and seven chip set generated interrupts. The output of the PI is ANDed with the Mask Register to create the interrupt request (IRN) signal for the MA17502 Control Unit. A one in a PI bit position indicates an interrupt is pending and the interrupt level is equal to the bit position.

2.2 Mask Register

The Mask Register (MK) is the dedicated 16-bit register containing the information that filters the PI output to the Priority Encoder and the IRN generation logic. A one in a MK bit position allows the interrupt request, of the same bit position in the PI, to enter the Priority Encoder and cause IRN to drop low. PI bits 1 - 4 and 6 - 15 are maskable.

2.3 Interrupt Priority Encoder

The Interrupt Priority Encoder accepts the enabled, mask filtered, output of the PI and generates a four bit code designating the level of the highest priority pending interrupt. Level zero (PI bit zero) has the highest priority and level 15 (PI bit 15) the lowest. The four bit priority code is placed on the AD Bus during the microcoded interrupt handling routine.

2.4 Fault Register

The Fault Register (FT) is the dedicated 16-bit register that latches the 15 specified (fault 12 is reserved) faults. The FT supports eight external Fault inputs and three chip-set generated Faults. The output of the FT is ORed together, buffered by a falling-edge detector, and input to the PI to generate the level one interrupt. FT bits 13 - 15 are used to indicate the results of the MAS281 BIT. Once the FT has latched a fault, it can only be cleared via internal I/O command (individual fault bits cannot be cleared).

Anti-repeat logic between the FT and PI prevents latching more than a single interrupt into the PI before the user interrupt service routine has cleared the FT. The microcoded interrupt service routine reads the interrupt priority vector from the Interrupt Unit and clears the serviced interrupt from the PI. At this point the PI is ready to latch another interrupt into this bit. When this microcoded service routine acts on a level 1 interrupt, it clears the PI bit 1, but the FT maintains the interrupting fault bit(s). Therefore, a level 1 interrupt would be latched again if there were no anti-repeat logic to prevent a never ending loop of interrupts from occurring.

Interrupts are serviced at the end of the currently executing instruction if not masked and if interrupts are enabled. System software servicing level 1 interrupts must clear the FT via the RCFR internal I/O command at some point in the routine to allow subsequent faults to latch a level 1 interrupt request. A non-destructive read of the FT is provided by the internal I/O command RFR, but this command should be used carefully.

2.5 Interval Timers

The Interrupt Unit contains both MIL-STD-1750A 16-bit interval timers, A and B. The TCLK input is synchronized with SYNCLKN and increments Timer A once a TCLK period. Timer B is incremented by the synchronized TCLK divided by 10. Timer A overflow sets PI bit 7 and Timer B overflow sets PI bit 9. The timers are controlled via the I/O command decode logic, or they can be disabled via the DTIMERN input.

MA17503
MIL-STD-1750A Interrupt Unit

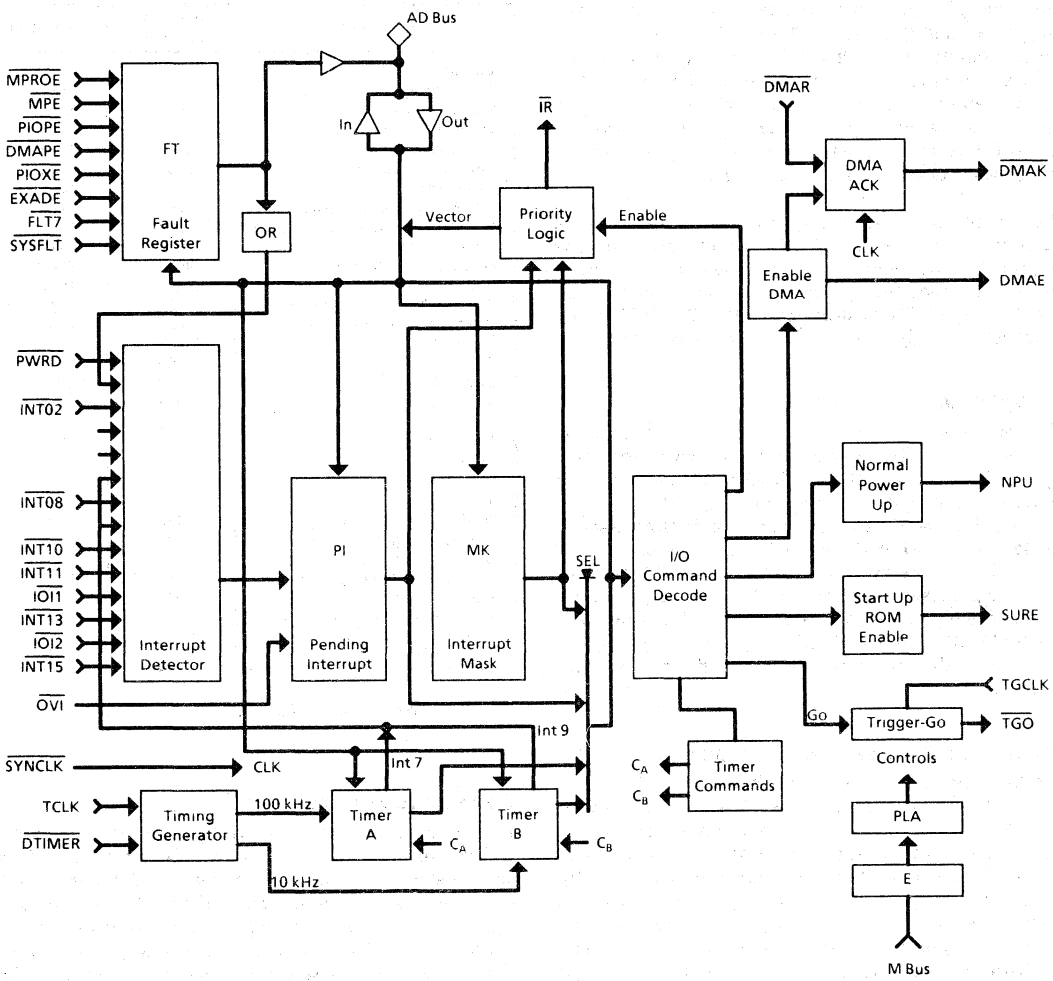


Figure 2. MA17503 Interrupt Unit Architecture

2.6 Watchdog Timers

The Interrupt Unit contains two watchdog timers, Trigger-Go and Bus Fault. The Bus Fault timer assures timely completion of all AD Bus cycles by terminating bus cycles over two TCLK (maximum, minimum one TCLK period) periods in duration. This function is automatic, but can be disabled by DTON low. FT bit 5 or 8 is set for terminated I/O transfers or memory transfers, respectively, when the Bus Fault timer expires.

The Trigger-Go timer is an autonomous 16-bit ripple counter incremented by TGCLK. Upon power-up, the Trigger-Go timer begins to count. The GO I/O command resets the timer, thus preventing it from overflowing and causing TGON to drop low. The DTIMERN input prevents the Trigger-Go timer from incrementing.

2.7 DMA Control Interface

The DMA control interface logic is contained in the Interrupt Unit. The interface is composed of the three signals: DMAE, DMARN, and DMAKN. If the interface is enabled, an internal I/O command raises DMAE high to indicate the MAS281's readiness to accept DMA transfer requests (DMARN low). A subsequent low on DMARN causes the IU to respond with DMAKN low. DMAKN low halts the processor and places all AD Bus and bus control lines in the high-impedance state. Control is returned to the MAS281 when DMARN is pulled high again. DTIMERN is the user available way to disable the DMA interface.

2.8 Internal I/O Command Decode Logic

The Interrupt Unit implements the 26 MIL-STD-1750A specified I/O command functions listed in Table 2. The IU also decodes an additional 386 commands that are implemented in the MMU(BPU) and the two Status Word XIO commands that are handled in microcode for AD Bus control. The IU continually monitors AD Bus traffic. When M/ION is low, the IU latches the information present on the AD Bus during the address portion of the bus cycle. This information is subsequently decoded and creates the appropriate control signals to perform the I/O command function.

Operation	Command Code (Hex)	Mnemonic
Output		
Set Fault Register	0401	SFR
Set Interrupt Mask	2000	SMK
Clear Interrupt Request	2001	CLIR
Enable Interrupts	2002	ENBL
Disable Interrupts	2003	DSBL
Reset Pending Interrupt	2004	RPI
Set Pending Interrupt Register	2005	SPI
Reset Normal Power Up Discrete	200A	RNS
Write Status Word	200E	WSW
Enable Start Up ROM	4004	ESUR
Disable Start up ROM	4005	DSUR
Direct Memory Access Enable	4006	DMAE
Direct Memory Access Disable	4007	DMAD
Timer A Start	4008	TAS
Timer A Halt	4009	TAH
Output Timer A	400A	OTA
Reset Trigger-Go	400B	GO
Timer B Start	400C	TBS
Timer B Halt	400D	TBH
Output Timer B	400E	OTB
Input		
Read Configuration Word	8400	RCW
Read Fault Register Without Clear	8401	RFR
Read Interrupt Mask	A000	RMK
Read Pending Interrupt Register	A004	RPIR
Read Status Word	A00E	RSW
Read and Clear Fault Register	A00F	RCFR
Input Timer A	C00A	ITA
Input Timer B	C00E	ITB

Table 2. Internal I/O Command Summary

2.9 Microcode Decode Logic

The microcode decode logic can be split into command and control functions. Microcode instruction bits 4, 5 and 6 are decoded as commands for the FT, the interrupt interface, the DMA interface, and the discrete output signal, NPU. The microcode command interface is enabled when INTREN is pulled low and is disabled during DMA and the Hold state. Microcode bits 5 and 6 provide control of DDN during memory read and write cycles, and external I/O cycles.

3.0 Interface Signals

All signals comply with the voltage levels of Table 1. In addition, each of these functions is provided with Electrostatic Discharge (ESD) protection diodes. All unused inputs must be held to their inactive state via a connection to VDD or GND.

Throughout this data sheet, active low signals are denoted by either a bar over the signal name or by following the name with an "N" suffix (e.g., DMAKN). Referenced signals that are not found on the MA17503 are preceded by the originating chip's functional acronym in parentheses (e.g., (EU)OSC).

Following is a description of each pin function grouped according to functional interface. The function name is presented first, followed by its acronym, its type, and its description. Function type is either input, output, high impedance (Hi-Z), or a combination thereof. Timing characteristics of each of the functions described is provided in Section 5.0.

3.1 Power Interface

The power interface consists of one 5V VDD connection and one GND connection.

3.2 Clocks

The clock interface, discussed below, provides synchronization for Interrupt Unit operations and the clock inputs for the interval and watchdog timers.

3.2.1 Synchronisation Clock (SYNCLKN)

Input. The MA17501 Execution Unit (EU) generates the SYNCLKN signal for the Interrupt Unit. The Interrupt Unit uses this signal to synchronise system inputs (e.g., interrupts and faults) to the MAS281 machine cycle and to control all other internal functions.

3.2.2 Timer Clock (TCLK)

Input. TCLK is a 100 KHz, user provided clock signal that drives the interval timers A and B, and the Bus Fault timer. TCLK is synchronised to the MAS281 machine cycle, via SYNCLKN, before being sent to the interval timers. This allows the IU to implement the Internal I/O Commands associated with timer operation.

The synchronised version of TCLK drives interval timer A, clocking it once every 10 microseconds. The synchronised TCLK is divided by 10 to provide a 10 KHz clock for driving interval timer B, clocking it once every 100 microseconds.

The unsynchronised TCLK is used to increment the Bus Fault watchdog timer. When DSN drops low, the Bus Fault timer is enabled to count and expires after two TCLK high-to-low transitions.

3.2.3 Trigger-Go Clock (TGCLK)

Input. This user provided clock drives the autonomous on-chip system watchdog timer. The Trigger-Go timer is incremented by the high-to-low transition of TGCLK.

3.3 Buses

Following is a discussion of the two communication buses connecting the Interrupt Unit to the rest of the three chip set. The AD Bus transfers 16-bit data and commands, while the M Bus communicates microcode control data.

3.3.1 Address/Data Bus (AD Bus)

Input/Output/Hi-Z. These signals comprise the multiplexed address and data bus. During internal bus operations, the AD Bus accommodates the transfer of Internal I/O commands and data from the MA17501 Execution Unit to the Interrupt Unit. It also accommodates the transfer of data from the Interrupt Unit to the Execution Unit in response to internal I/O commands. AD00 is the most significant bit position and AD15 is the least significant bit position of both the 16-bit data and 16-bit command. A high on this bus corresponds to a logic 1 and a low corresponds to a logic 0.

Commands on the AD Bus are passed through transparent latches during the low state of input/output SYNCLKN cycles and are latched at the low-to-high transition of SYNCLKN. Data on the AD Bus, is either clocked into the IU by the high-to-low transition of SYNCLKN or placed there by the IU during the low portion of SYNCLKN.

3.3.2 Microcode Bus Bits 4, 5 and 6 (M04, 05 & 06)

Inputs. M04, M05, M06 are bits 4, 5 and 6 of the 20-bit Microcode Bus and are coded in the 40-bit microcode instruction as bits 4, 5 and 6. These bits are latched into the IU at the SYNCLKN high-to-low transition and are decoded for commanding the Fault Register, the DMA interface, the NPU discrete, and for providing the 4-bit priority encoded interrupt vector to the EU. IU microcode command cycles are extended to six (EU)OSC cycles by INTREN low. Microcode bits 5 and 6 provide control of DDN during memory and external I/O cycles. The microcode bus is not latched during DMA or the Hold state (DMAKN or HLDAKN low).

3.4 Bus Control

The following is a discussion of the signals used to control the AD Bus and M Bus. They enable the respective busses at the proper time and control system access to the MAS281 System AD Bus.

3.4.1 Data Strobe (DSN)

Input. The Interrupt Unit receives DSN from the Execution Unit. The DSN high-to-low transition starts the Bus Fault watchdog timer and during successful bus data transfers, the low-to-high transition halts and resets the Bus Fault watchdog timer. DSN is also instrumental in controlling the DDN signal during MAS281 Read/Input bus cycles.

3.4.2 Memory/Input-Output (M/ION)

Input. The Interrupt Unit receives M/ION from the Execution Unit M/ION low enables I/O command decoding logic M/ION also selects the FT bit to set in response to a low on MPROEN and EXADEN.

3.4.3 Interrupt Unit Ready (IRDYN)

Output. The Interrupt Unit uses the IRDYN signal to cause the Execution Unit clock generation state machine to inject one wait state into Internal I/O machine cycles, thus causing the minimum five (EU)OSC period machine cycle to be extended to a six (EU)OSC period 50% duty cycle machine cycle. Internal I/O machine cycles occur during execution of the IU implemented I/O commands listed in Table 2.

3.4.4 Interrupt Unit Microcode Enable (INTREN)

Input. The Execution Unit provides INTREN to the Interrupt Unit to enable the microcode command interface. When INTREN is low, microcode instruction bits 4, 5 and 6 (latched into the IU microcode register at the SYNCLKN high-to-low transition, if HLDAKN and DMAKN are high) are decoded by the IU as commands for the FT, NPU discrete, internal DMA interface, and interrupt vectoring. INTREN low causes the EU to extend the machine cycle to six (EU)OSC periods.

3.4.5 Data Transceiver Direction (DDN)

Output. DDN is provided to control the directionality of the AD/Data Bus transceivers. DDN is high during data transfers from the MAS281 to the user system and when it is necessary to keep the transceivers from driving the MAS281 System AD Bus. DDN is low during transfers from the user system to the MAS281.

Cycles during which DDN is high include: memory writes, outputs, IU implemented Internal I/O command execution (except Read Configuration Word (RCW)), and all MA17504 MMU(BPU) implemented I/O command execution.

Cycles during which DDN is low include: memory reads (data portion), inputs (data portion), the Configuration Word read (identified by CONFWN, low), and during DMA and Hold cycles (to allow access to the MMU(BPU).

3.4.6 Control Transceiver Direction (CDN)

Output. CDN is provided to control the directionality of the Control Bus (consists of DSN, (EU)AS, M/ION, RD/WN, and IN/OPN) transceivers. CDN is high during all MAS281 directed machine cycles. CDN drops low only when DMAKN or HLDAKN is low, indicating the MAS281 has placed the control bus signals in the high-impedance state. (It is necessary to use transceivers to buffer the control bus, if a shared MMU(BPU) architecture is used, to allow the sharing device access to the MMU(BPU) functions.)

3.5 Interrupt Interface

The Interrupt Unit supports 16 levels of prioritised interrupts, nine of which are accessible to the user system. All user accessible interrupts are active low, are buffered with edge detectors to prevent repeat latching of the interrupt, and are latched into the Pending Interrupt register (PI) by the high-to-low transition of SYNCLKN.

The following interrupts do not have dedicated input pins on the MA17503. Level 1, Machine Error Interrupt, is driven by the ORed bits of the Fault register (FT). Levels 7 and 9 are driven by the overflow of Interval Timers A and B, respectively. The Internal I/O command, Set Pending Interrupt (SPI), is used to set interrupt levels 3, 5, and 6 (Floating-Point Overflow, Executive Call, and Floating-Point Underflow, respectively) via microcoded execution.

3.5.1 Power Down Interrupt (PWRDN)

Input. The PWRDN interrupt is the highest priority interrupt, level 0, and is latched into PI bit zero. It is non-maskable and cannot be disabled.

3.5.2 User Interrupts (INT02N, 08N, 10N, 11N, 13N & 15N)

Inputs. Each of these user definable interrupts is latched into the PI register bits 2, 8, 10, 11, 13, or 15, respectively. Level 2 is the highest priority and level 15 is the lowest. These interrupts are maskable and can be disabled.

3.5.3 I/O Registered Interrupts (IOI1N & IOI2N)

Inputs. Each of these interrupts is latched into the PI register bits 12 and 14, respectively. Level 12 is higher than level 14. These interrupts are maskable and can be disabled.

3.5.4 Fixed-Point Overflow (OVIN)

Input. This interrupt is driven by the MA17501 Execution Unit and is latched into the PI register bit 4. The OVIN interrupt is maskable and can be disabled.

3.5.5 Interrupt Request (IRN)

Output. This signal is the logical inclusive OR of the PI bits and is used to signal the MA17502 Control Unit that an interrupt request is pending.

3.6 Fault Interface

The Interrupt Unit supports 16 registered error condition flags. Eleven of the faults are directly accessible through dedicated input pins. A low on any of these fault inputs is latched into the Fault register (FT) by the high-to-low transition of SYNCLKN. Once a fault is latched, it can only be cleared by clearing the entire FT via Internal I/O command. The latching of any fault causes the level 1 interrupt to be set. Once set and subsequently cleared by the microcoded interrupt service routine, PI bit one cannot be set again until the FT is cleared via internal I/O command. Any unused fault inputs must be pulled-up to VDD.

3.6.1 Memory Protection Error (MPROEN)

Input. A low on this input is used to inform the MAS281 that an access fault, execute or write protection violation has been detected. When the MA17504 MMU(BPU) is used with the MAS281, the MPROEN fault input is provided by the MMU(BPU). FT bit 0 is set if a MAS281 directed memory cycle caused the error and bit 1 is set if a DMA device directed memory cycle caused the error.

Setting FT bit 0 causes PIFN to drop low. This aborts the MIL-STD-1750A instruction that was executing when the error occurred and branches execution to the machine error, level 1 interrupt service routine, if the interrupt is not masked. If the interrupt is masked, execution continues with the next instruction.

FT bit 0 is not latched during DMA or the Hold state (DMAKN or HLDAKN low).

3.6.2 Memory Parity Error (MPEN)

Input. A low on this input indicates a parity error has been detected during a memory transfer. This fault is latched into FT bit 2.

3.6.3 Programmed I/O Parity Error (PIOPEN)

Input. A low on this input indicates a parity error has been detected during an external I/O transfer. This fault is latched into FT bit 3.

3.6.4 DMA Parity Error (DMAPEN)

Input. A low on this input indicates a parity error has been detected during a DMA data transfer. This fault is latched into FT bit 4.

3.6.5 External Address Error (EXADEN)

Input. A low on this input indicates execution of an unimplemented or reserved I/O command has been attempted (M/ION low) and sets FT bit 5, or an attempt has been made to access an unimplemented memory address (M/ION high) and sets FT bit 8.

Provision for detection of these conditions has been made on the MA17503 in the form of a Bus Fault watchdog timer. If during an I/O or memory access cycle the system machine cycle completion circuitry or (EU)RDYN generation logic fails to provide the (EU)RDYN signal within the required amount of time, the Bus Fault watchdog timer will terminate the cycle by forcing IRDYN low and set the appropriate FT bit (FT5 if I/O, FT8 if memory). The minimum Bus Fault watchdog timeout period is one TCLK period, the maximum is two TCLK periods.

Setting FT bits 5 or 8 causes PIFN to drop low. This aborts the MIL-STD-1750A instruction during which the error occurred and branches execution to the machine error, level 1, interrupt service routine, if the interrupt is not masked. If the interrupt is masked, execution continues with the next instruction.

FT bit 5 and 8 are not latched during DMA or the Hold state (DMAKN or HLDAKN low).

3.6.6 Programmed I/O Transmission Error (PIOXEN)

Input. A low on this input indicates a user defined error has occurred during an I/O transfer. This fault is latched into FT bit 6.

3.6.7 Fault #7 (FLT7N)

Input. This is a user definable (spare) fault input. A low on this input sets FT bit 7.

3.6.8 System Fault (SYSFN)

Input. A low on this input indicates a system Built-In Test error has occurred. This fault is latched into FT bits 13 and 15.

3.6.9 Illegal Address (ILLADN)

Output. The high-to-low transition of this output is used to latch the appropriate data into the MA17504 memory Fault Status Register (MFSR) when a FT bit 5 or 8 is set.

FT bits 5 and 8 are set by a low on the EXADEN input or by the Bus Fault watchdog timer overflow. FT bits 5 and 8 are not latched, and ILLADN is held high during DMA or the Hold state (DMAKN or HLDAKN low).

3.6.10 Instruction Abort (PIFN)

Output. A low on this output effects a MIL-STD-1750A instruction abort. When a SYNCLKN high-to-low transition latches FT bit 0, 5, or 8, the following SYNCLKN high-to-low transition causes PIFN to drop low and remain low for one SYNCLKN period (except during DMA and the Hold state, i.e., DMAKN or HLDAKN low).

PIFN directs the MA17502 Control Unit to branch microcode execution to the interrupt vectoring routine for level 1 interrupt servicing. If the level 1 interrupt is masked, execution will resume with the next MIL-STD-1750A instruction.

PIFN causes the MA17501 Execution Unit to hold DSN and (EU)AS in their inactive state during the transition from error indication to the beginning of the interrupt servicing routine.

3.7 DMA Interface

The DMA Interface consists of the necessary handshake signals required to effect transfer of control from the MAS281 to a DMA controller and back again.

3.7.1 DMA Transfer Enable (DMAE)

Output. When this output is raised high via execution of the Internal I/O command DMAE, direct memory access requests will be acknowledged by the MAS281. If DMAE is low, direct memory access requests will not be acknowledged by the MAS281.

3.7.2 DMA Transfer Request (DMARN)

Input. A DMA controller pulls this input low to request control of the AD Bus and bus control signals for DMA transfers. DMARN is held low by the DMA controller for the duration of the DMA transfer, and the low-to-high transition indicates the DMA controller is finished using the AD Bus.

3.7.3 DMA Transfer Request Acknowledge (DMAKN)

Output. The Interrupt Unit responds to a low on DMARN, if DMAE is high, by dropping DMAKN low at the SYNCLKN high-to-low transition.

3.8 Inter-Chip Control

The Inter-Chip Control signals are used to halt the processor (the three-chip set) during the DMA and HOLD cycles and during microcode testing.

3.8.1 Processor Pause (PAUSEN)

Output. This output is low during DMA operations (DMAKN low). PAUSEN is used by the Interrupt Unit to reset and disable the Bus Fault Timeout circuitry. PAUSEN is also used by the MA17501 Execution Unit clock generation circuitry to produce an internal disable signal. This internal disable signal holds CLKPCN and SYSCLK1N low and CLK02N high, which halts processing, and places the DSN, AS, IN/OPN, RD/WN, and M/ION output buffers, and the AD bus I/O buffers in the high-impedance state, and drop DDN and CDN low to allow DMA controller access to the MMU(BPU) in shared MMU(BPU) systems.

3.8.2 Hold Acknowledge (HLDAKN)

Input. HLDAKN resets and disables the Bus Fault Timeout circuitry, causes DDN and CDN to be brought low, and prevents latching of microcode commands and decoding. The Execution Unit responds to a Hold state request (execution of BPT, or a low on HOLDN) by pulling HLDAKN low.

3.8.3 Microcode Stop (MSTOPN)

Input. MSTOPN allows microcode to be single-stepped during testing by Marconi Electronic Devices and should be pulled up to VDD in customer applications.

3.9 Timer Control

These Timer Control inputs allow external control of Timers A and B, the Trigger-Go Counter, and the Bus Fault Timeout circuitry.

3.9 1 Disable Timers (DTIMERN)

Input. A low to this input disables Timers A and B and the Trigger-Go counter, and also disables DMA access by forcing DMAE low and DMAKN high. Raising DTIMERN high causes Timers A and B and the Trigger-Go counter to resume counting where they were stopped, and also allows normal DMA operations.

3.9.2 Disable Bus-Fault Timeout (DTON)

Input. A low to this input will reset and disable the Bus-fault timeout circuitry.

2

3.10 Discretes

Four discrete outputs are provided for system use, all of which are enabled or disabled or both via internal I/O commands.

3.10.1 Trigger-Go Timer Overflow (TGON)

Output. This output drops low whenever the Trigger-Go counter overflows (rolls over to 0000). It returns high when the Trigger-Go counter is reset by software using the GO internal I/O command.

3.10.2 Normal Power-Up Indicator (NPU)

Output. This output is brought low via internal I/O command during module initialization as the first step of BIT. If BIT is completed successfully, NPU is raised high via microcode, and remains high until reset by software via the RNS internal I/O command.

Start-Up ROM Enable (SURE)

Output. This output is used to enable an externally implemented Start-Up ROM. SURE is brought high via the execution of the ESUR internal I/O command (done by microcode during initialization or by software), and remains high until it is reset by software by using the DSUR internal I/O command. While SURE is high, all memory reads shall access main memory. This feature is utilized via the MOV instruction to effect a non-volatile memory program transfer to faster program execution RAM.

Configuration Word Enable (CONFWN)

Output. This output is brought low during the data portion of an RCW (Read Configuration Word) internal I/O operation. It is used as an output enable strobe for the externally implemented Configuration Register. Because RCW is an internal I/O command, the read cycle is a fixed six (EU)OSC cycles and is terminated by IRDYN low. RDYN must not be asserted during execution of this command.

4.0 Operating Modes

The following discussions detail the MAS281 chip set operating modes from the perspective of the Interrupt Unit. The MAS281 operating modes involving the MA17503 are: (1) initialization, (2) instruction execution, (3) interrupt servicing, (4) fault servicing, (5) DMA support, (6) Hold support, and (7) timer operations.

4.1 Initialisation

A microcoded initialisation sequence is executed by the chip set in response to a hardware reset. This routine, as applicable to the Interrupt Unit, disables and masks interrupts, zeroes the Fault register, performs the MAS281 Integrated Built-In Test (BIT), raises the Start-Up ROM enable discrete (SURE), clears and starts timers A and B, resets the Trigger-Go counter, and disables DMA access. The resulting initialised state of the MA17503 is listed in Table 3.

The microcoded BIT exercises all legal microinstruction bit combinations and tests all internally accessible structures of the MAS281 chip set. For the Interrupt Unit this includes the MK, PI, and FT registers, Interrupt Enable/Disable, and Timers A and B. Table 4 details the tests performed by each of the five BIT routines.

If any part of BIT fails, an error code identifying the failed subroutine is loaded into FT bits 13-15, BIT is aborted with NPU left in the low state, initialization is completed, and instruction execution begins at address zero. The coding of the BIT results is shown in Table 4.

NOTE: To complete initialization and pass BIT, interrupt and fault inputs must be high for the duration of the initialization routine. In addition, timers A and B must be clocked for BIT success.

Item	Status
Fault (FT)	Zeroed
Pending Interrupt (PI)	Zeroed
Mask (MK)	Zeroed
Interrupts	Disabled
DMA Access	Disabled
Timer A	Reset and Started
Timer B	Reset and Started
Trigger-Go Timer	Reset and Started

Table 3. Interrupt Initialisation State

BIT	Test Coverage	BIT Fail Codes ($FT_{13, 14, 15}$)	Cycles
1	Microcode Sequencer IB Register Control Barrel Shifter Byte Operations and Flags	100	221
2	Temporary Registers (T0 - T7) Microcode Flags Multiply Divide	101	166
3	Interrupt Unit - MK, PI, FT Enable/Disable Interrupts	111	214
4	Status Word Control User Flags General Registers (R0 - R15)	110	154
5	Timer A Timer B	111	763
–	BIT Pass/Fail Overhead	–	26

Note: BIT pass is indicated by all zeros in FT bits 13, 14, and 15

Table 4. MAS281 BIT Summary

4.2 Instruction Execution

The MAS281 chip set will begin instruction execution upon the completion of initialization. The instruction execution operations that involve the Interrupt Unit are: (1) internal CPU cycles, (2) memory transfers, and (3) input/output transfers. Instruction execution can be interrupted at the end of any individual machine cycle by a DMA request (DMARN low with DMAE high) or at the conclusion of any given instruction by an Interrupt or Hold state request.

4.2.1 Internal CPU Cycles

Microcode controlled IU functions are classified as internal CPU cycles. The IU interprets the three microcode bits, 4, 5, and 6, as a three bit instruction used for control of the FT, internal DMA interface, NPU discrete, and the interrupt priority vector code. The command is latched into the IU at the SYNCLKN high-to-low transition and decoded into control signals if INTREN is low. During these machine cycles, SYNCLKN is six (EU)OSC periods long. During internal CPU cycles, DSN and M/ION are held high by the Execution Unit, causing the IU to hold DDN high. Microcode bits 4, 5, and 6 are not latched or decoded during DMA or the Hold state (DMAKN or HLDAKN low).

4.2.2 Memory Transfers

The IU takes a passive role during memory transfers, i.e., it only controls the DDN signal. Microcode bits 4, 5, and 6 are latched by the SYNCLKN high-to-low transition then bits 5 and 6 are decoded to control the DDN control signal in concert with DSN. If bits 5 and 6 are high (indicating a write), DSN is kept from affecting DDN, which remains high for the entire cycle. If either bit 5 or 6 is low, DSN is allowed to control DDN, which becomes a delayed version of DSN.

4.2.3 Input/Output Transfers

The IU monitors all AD Bus traffic and controls the DDN output as specified. During cycles where M/ION is low, the IU decodes the address/command portion (SYNCLKN high) of the machine cycle. If one of the commands listed in Table 2 is encountered, the specific action takes place at the following SYNCLKN high-to-low transition; the exceptions being "GO" and "RCW". "GO" resets the Trigger-Go Timer at the SYNCLKN low-to-high transition and "RCW" drops CONFWN low during DSN low.

The read and write status word commands ("RSW", "WSW") cause IRDYN to drop low to complete the EU/MMU(BPU) machine cycle. IU decoded I/O command cycles are six (EU)OSC periods long (except for "RCW", there are five (EU)OSC periods).

4.3 Interrupt Servicing

Nine user interrupt inputs and one dedicated input (OVIN) are provided for programmed response to asynchronous system events. A low on any of these inputs will be detected at the high-to-low transition of SYNCLKN and latched into the PI register on the following SYNCLKN high-to-low transition (with the exception of INT02N which is latched into PI when INT02N is first detected). This always occurs whether interrupts are enabled or disabled, or whether specific interrupts are masked or unmasked.

Each of the nine user interrupt inputs is buffered by a falling-edge detector to prevent repeat latching of requests held low longer than the first SYNCLKN high-to-low transition. An interrupt request input must go back to the high state before request on that input can be detected.

Command	M04, M05, M06
Load Fault Register From AD Bus	001
Read Interrupt Priority Vector Onto AD Bus	010
Raise Normal Power-up Discrete	011
Disable I/O Control of DMA Interface	100
Enable I/O Control of DMA Interface	101

Table 5. Interrupt Unit Microcode Commands

The output of the PI register is continually ANDed with the output of the MK register (level 0 interrupt is not maskable). If interrupts are enabled, and an unmasked interrupt is pending, the Interrupt Request (IRN) output to the Control Unit is asserted. This occurs when one or more interrupts are latched and unmasked. The unmasked pending interrupts are output to the priority encoder where the highest priority pending interrupt is encoded as a 4-bit vector.

After the currently executing MIL-STD-1750A instruction is completed, the Control Unit checks the state of the IRN input. If IRN is asserted, a branch is made to the microcode interrupt service routine. During this routine, the priority encoder's 4-bit vector is read into the Execution Unit, where the vector is used to calculate the appropriate interrupt linkage and service pointers (Table 6). When the EU reads the interrupt priority vector from the IU, the interrupt being serviced is cleared from the PI. If no other interrupts are pending, this also causes the IRN signal to be deactivated.

4.4 Fault Servicing

Eight external fault inputs are provided to the interrupt unit. A low on any of these inputs is latched into the FT register at the high-to-low transition of SYNCLKN. The capture of one or more of these faults immediately sets pending interrupt level 1 (machine error) of the PI.

Anti-repeat logic between the FT and PI prevents latching more than a single interrupt into the PI before the user interrupt service routine has cleared the FT. The microcoded interrupt service routine reads the interrupt priority vector from the Interrupt Unit and clears the serviced interrupt from the PI. At this point the PI is ready to latch another interrupt into this bit.

When this microcoded service routing acts on a level 1 interrupt, it clears the PI bit 1, but the FT maintains the interrupting fault bit(s). Therefore, a level 1 interrupt would be latched again if there was no anti-repeat logic to prevent a never ending loop of interrupts from occurring.

Interrupts are serviced at the end of the currently executing instruction if not masked and if interrupts are enabled. System software servicing level 1 interrupts must clear the FT via the RCFR internal I/O command at some point in the routine to allow subsequent faults to latch a level 1 interrupt request. A non-destructive read of the FT is provided by the internal I/O command RFR, but this command should be used carefully.

Faults caused by a low on EXADEN, MPROEN, or Bus Fault Timer expiration (FT 0, 5, 8) require that the currently executing MIL-STD-1750A instruction be aborted. In order to accomplish this, the latching of faults 0, 5, or 8 causes the Interrupt Unit to assert the instruction abort (PIFN) output to both the Execution Unit and the Control Unit Faults 0, 5, and 8 are not latched during DMA cycles or the Hold state (CDN low).

Interrupt Number	Function	Priority(1) Level	Maskable	Disability	Linkage Pointer	Service Pointer
0	Power Down	0	No	No	20	21
1	Machine Error	1	Yes	No	22	23
2	User 0	2	Yes	Yes	24	25
3	Floating Point Overflow	3	Yes	Yes	26	27
4	Fixed Point Overflow	4	Yes	Yes	28	29
5	Executive Call	5	No	No	2A	2B
6	Floating Point Underflow	6	Yes	Yes	2C	2D
7	Timer A	7	Yes	Yes	2E	2F
8	User 1	8	Yes	Yes	30	31
9	Timer B	9	Yes	Yes	32	33
10	User 2	10	Yes	Yes	34	35
11	User 3	11	Yes	Yes	36	37
12	I/O 1	12	Yes	Yes	38	39
13	User 4	13	Yes	Yes	3A	3B
14	I/O 2	14	Yes	Yes	3C	3D
15	User 5	15	Yes	Yes	3E	3F

Note: (1) Level 0 has highest priority, level 15 lowest.

Table 6. Interrupt Vector Assignments

4.5 DMA Support

DMA data transfers are performed over the system AD bus under the control of the IU DMA interface logic. The user signals that DMA requests will be honored by setting the DMAE output high via the DMAE internal I/O command. The DMA controller may request use of the AD bus by pulling DMARN low, but, unless DMAE is high, all such requests will be ignored. DMARN is acknowledged by raising DMAKN low. This occurs at the first SYNCLKN high-to-low transition after DMARN is pulled low.

When a DMA request is acknowledged (DMAKN low), DDN is dropped low to direct the system data bus transceivers to drive the local AD bus, and CDN is dropped low to disable the control signal buffers. (It is necessary to use transceivers to buffer the control bus if a shared MMU(BPU) architecture is used, to allow the sharing device access to the MMU(BPU) functions).

When the DMA controller relinquishes control of the AD bus (by raising DMARN high), DMA operations are ended by raising DMAKN high at the next SYNCLKN high-to-low transition, and DDN and CDN then resume normal operation.

4.6 Hold Support

The Hold interface is handled by the Execution Unit, but the Hold acknowledge (HLDAKN) line is monitored by the Interrupt Unit. When HLDAKN is active, the Interrupt Unit lowers DDN and CDN, resets and disables the Bus-Fault decoding (bits 4-6). When the Hold state is terminated, DDN and CDN resume normal operation.

4.7 Timer Operations

Interval Timers A and B, the Trigger-Go Counter and the Bus-Fault timer are all implemented in the Interrupt Unit.

4.7.1 Timers A and B

Timer A is clocked by the TCLK input (which is internally synchronised to SYNCLKN), whereas Timer B is clocked by an internally generated TCLK/10 (also internally synchronized to SYNCLKN). TCLK is required to be a 100-KHz pulse train by MIL-STD-1750A. If they are allowed to overflow. Timers A and B will set level 7 and level 9 interrupt requests, respectively. Each timer can be read, loaded, started, and stopped via internal I/O commands.

External control of Timers A and B can be accomplished by asserting the DTIMERN input. When DTIMERN is low, both timers will halt and all internally decoded internal I/O commands which would change their state are disabled (asserting DTIMERN low also disables DMA accesses by driving DMAE low and DMAKN high). Raising DTIMERN high allows normal operations to resume where they left off.

4.7.2 Trigger-Go Counter

The Trigger-Go Counter is clocked by the TGCLK input. DTIMERN low disables and enables counter operations in the same way as Timers A and B. When the Trigger-Go counter overflows, the output discrete TGON drops low and remains low until the counter is reset via the "GO" internal I/O command.

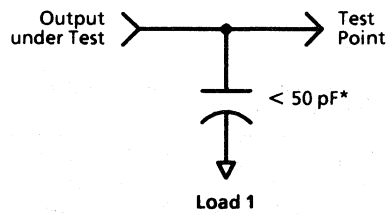
4.7.3 Bus-Fault Timer

This on-chip watchdog timer is provided to monitor all bus operations to ensure timely completion. This hardware timeout circuit is enabled at the start of each memory and I/O transfer (DSN high-to-low transition), and is reset on the following SYNCLKN high-to-low transition (an external ready (RDYN) must have been received by the Execution Unit for this to occur).

If this circuit is not reset within a minimum of one TCLK period or a maximum of two TCLK periods, either bit 3 (if a memory transaction) or bit 5 (if an I/O transaction) of the FT register is set. This causes the current MIL-STD-1750A instruction to be aborted as discussed above. This feature can be disabled externally by pulling DTON low and is not available during DMA or the Hold state (DMAKN or HLDAKN low).

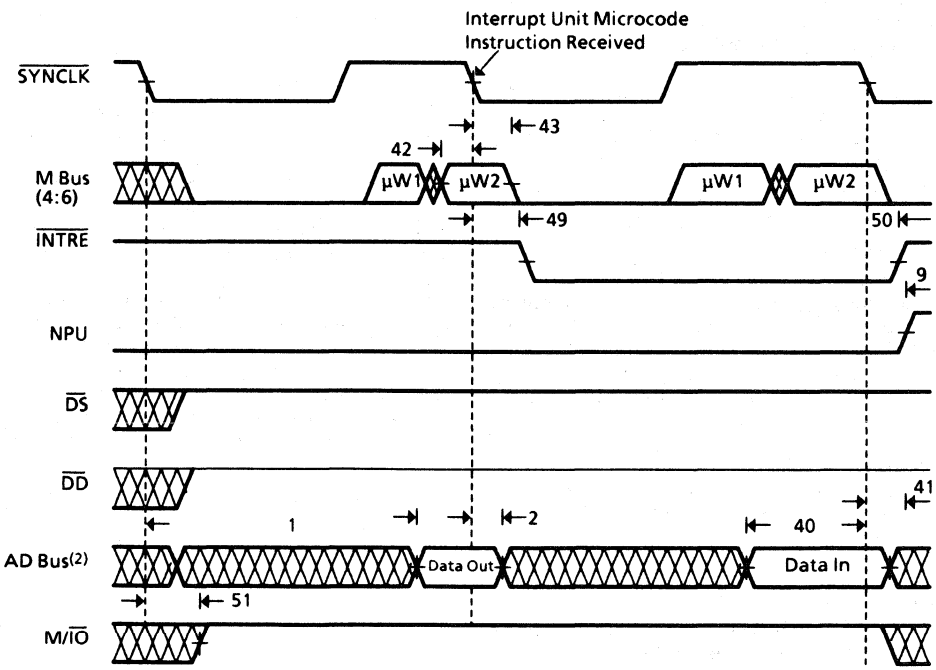
5.0 Timing Characteristics

This section provides the detailed timing specifications for the MA17503 Interrupt Unit. Figure 3 depicts the test loads used to obtain the timing data. Figures 4 through 15 depict the timing waveforms associated with various MA17503 signals. Table 7 lists values for the parameters specified in the timing waveforms. All timing values provided in Table 7 are valid over the full military temperature range (-55°C to +125°C), assume the recommended operating conditions, and are measured from 50% point to 50% point (50% of VDD supply voltage, unless otherwise specified). Crosshatching in Figures 4 through 15 indicates either a "don't care" state or indeterminate state.



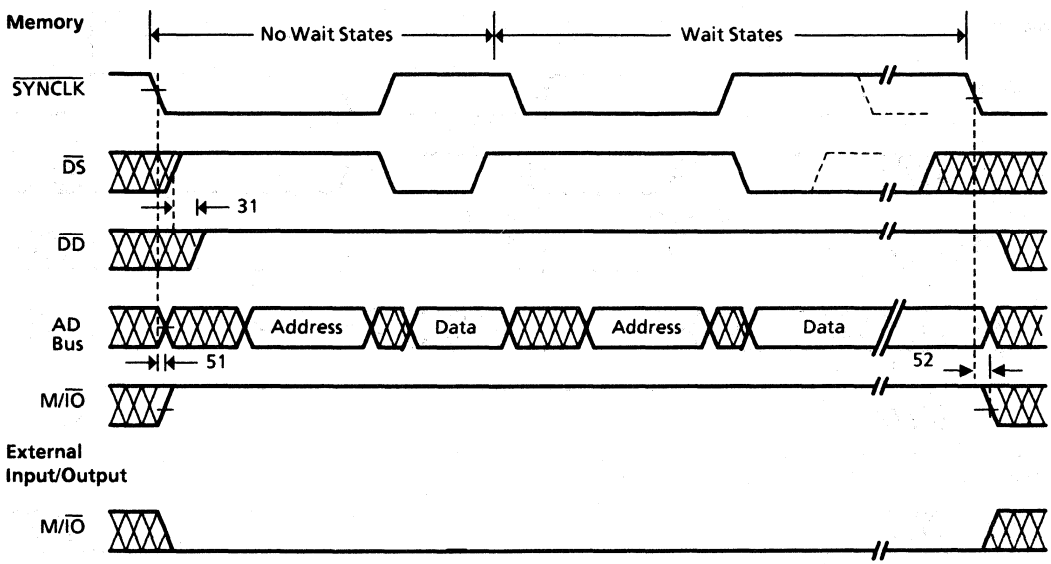
* Includes all jig and parasitic capacitance

Figure 3. Test Load



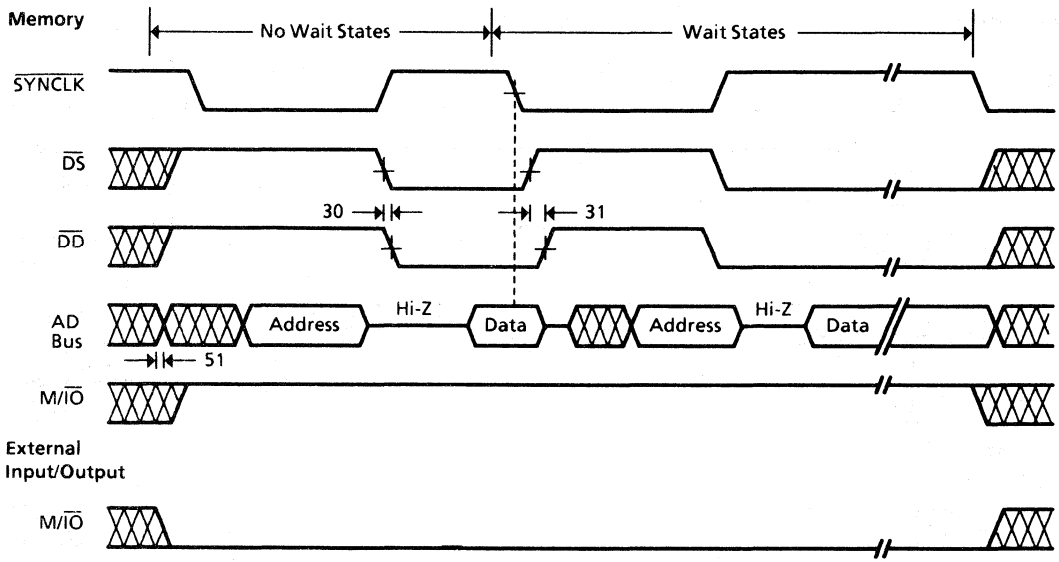
Notes:
1. Other outputs:
   IRDY = high
   CD = high
2. Data direction with reference to the Interrupt Unit

Figure 4. Microcode Operations



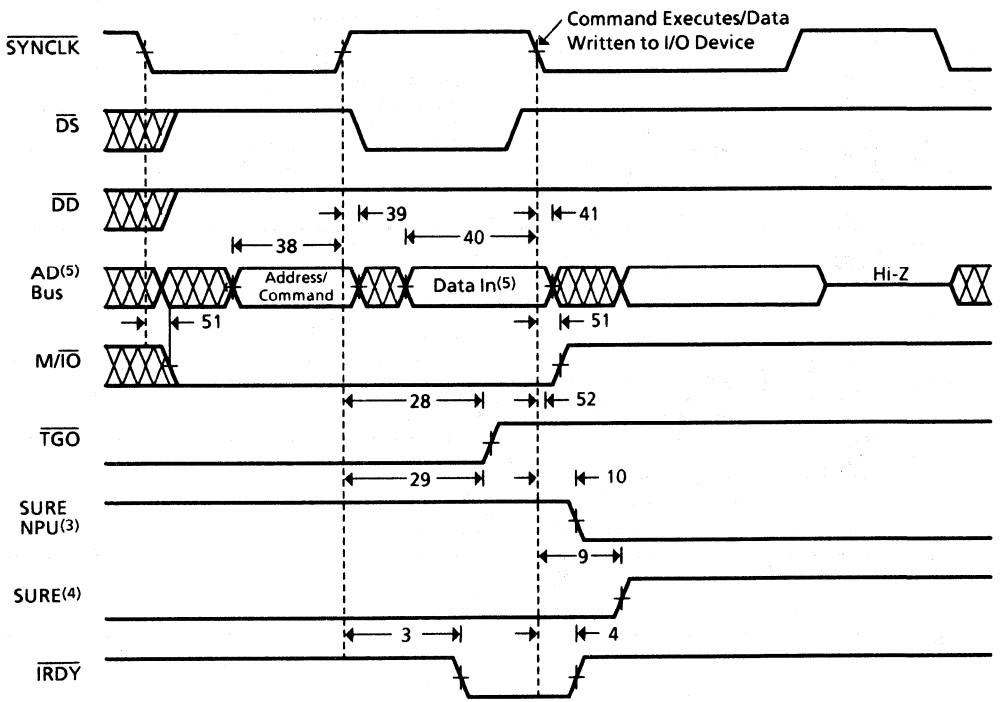
Notes:
1. Dashed timing lines indicate non-wait cycle timing.
2. Other output states:
   CD = high
   IRDY = high
   DMAK = high
   PAUSE = high
3. Other required input states:
   HLDAK = high
   DMAR = high

Figure 5. Write Transfer Timing



Notes:
1. Dashed timing lines indicate non-wait cycle timing.
2. Other output states:
   CD = high
   IRDY = high
   DMAK = high
   PAUSE = high
3. Other required input states:
   HLDAK = high
   DMAR = high

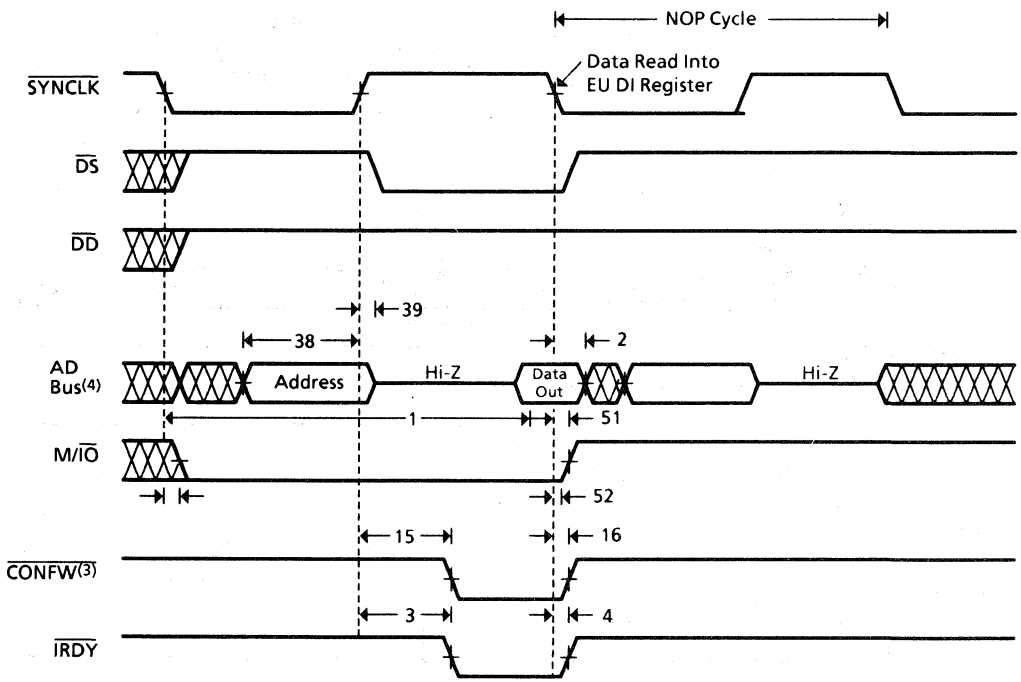
Figure 6. Read Transfer Timing



Notes:

1. Other output states:
   - CD = high
   - PAUSE = high
   - DMAK = high
2. Other required input states:
   - HLDAK = high
   - DMAR = high
   - RDY = high
3. XIO command, RNS.
4. XIO command, ESUR.
5. Data direction with reference to the Interrupt Unit.

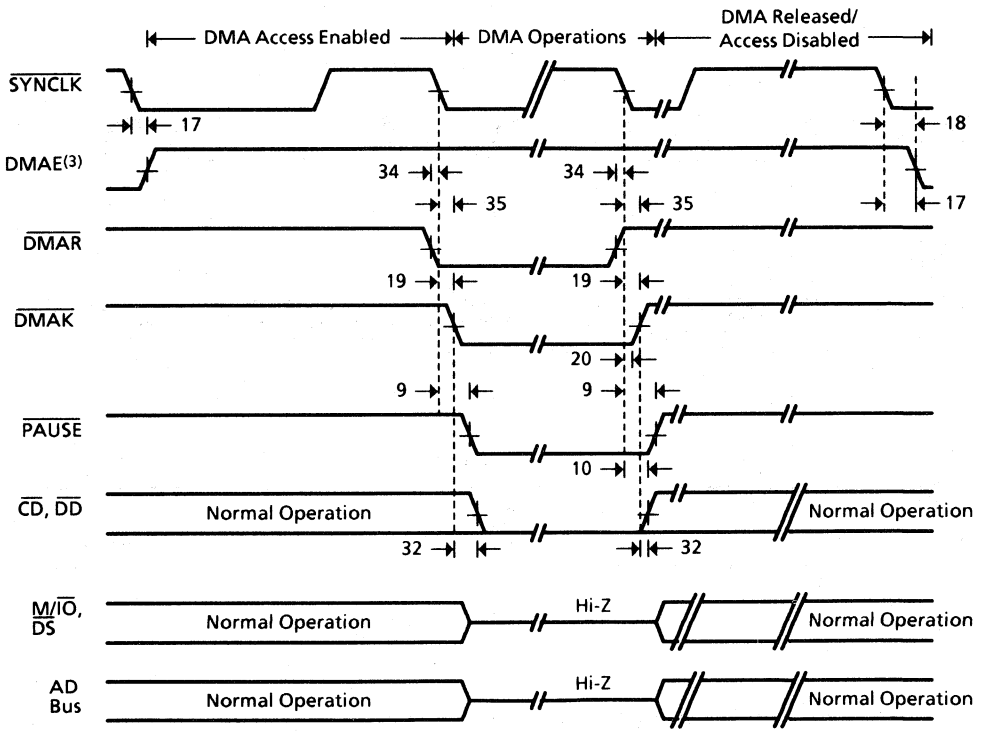
Figure 7. Internal I/O Timing - Write/Command



Notes:

1. Other output states:
   $\overline{CD}$ = high
   $\overline{PAUSE}$ = high
   $\overline{DMAK}$ = high
2. Other required input states:
   $\overline{HLDAK}$ = high
   $\overline{DMAR}$ = high
3. Active during RCW XIO only.
4. Data direction with reference to the Interrupt Unit.

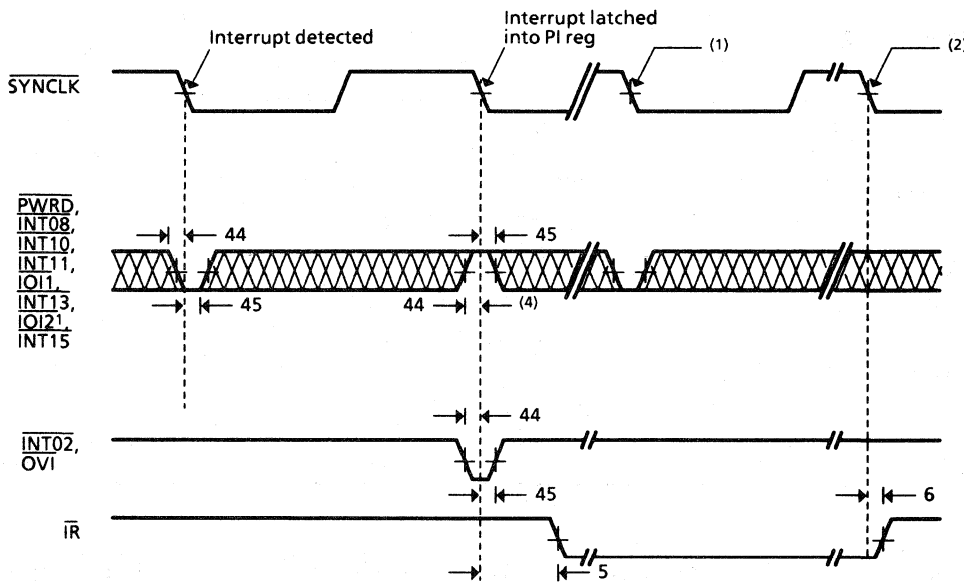
Figure 8. Internal I/O Timing - Read



Notes:

1. Other required input:
   $\overline{\text{DTIMER}}$ = high
2. Other output:
   $\overline{\text{IRDY}}$ = high
3. DMAE is enabled and disabled by XIO commands DMAE and DMAD respectively if the DMA interface has been enabled via microcode.

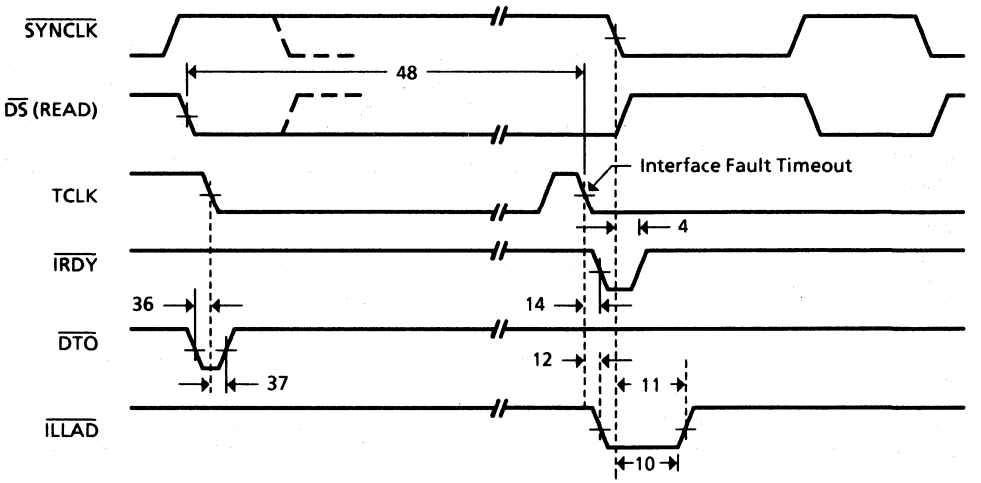
Figure 9. DMA Access/Release Timing



Notes:

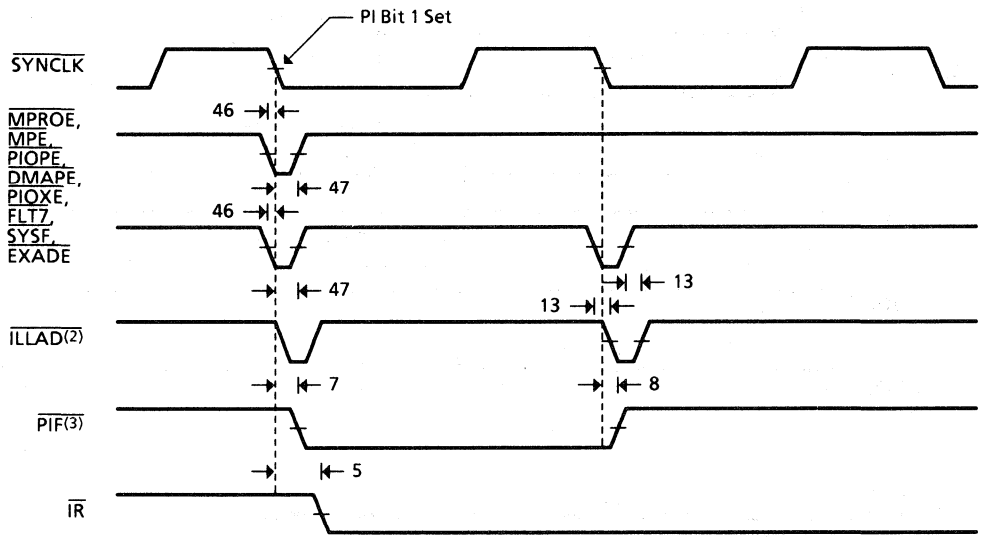
1. 1750A instruction completed, microcode interrupt handling routine begins.
2. 3rd machine cycle of microcode routine.
3. Other output:
   $\overline{IRDY}$ = high
   $\overline{CD}$ = high
   $\overline{DMAK}$ = high
   $\overline{PAUSE}$ = high
4. The interrupt input must be detected high by a SYNCLK high-to-low transition (after a low on the interrupt input) before a new interrupt on said input will be detected.

Figure 10. Interrupt Request Timing



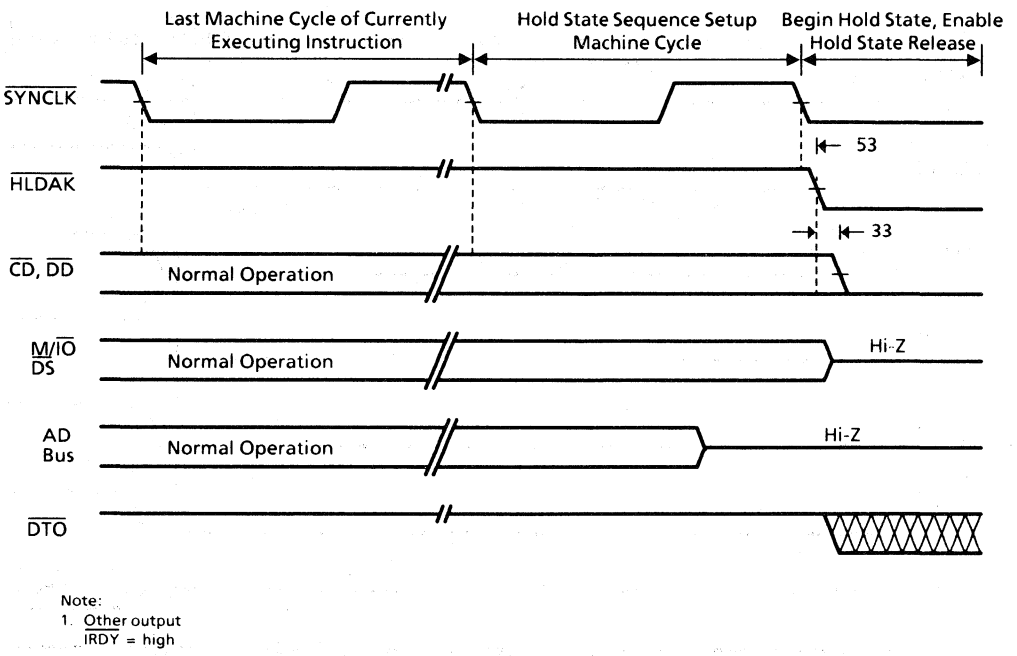
Notes:
1. 2TCLK ↓ edges during a continuous $\overline{DS}$ = low are necessary to cause a Bus Fault Timeout.
2. Other required input:
   $\overline{DTO}$ = high
3. Other output:
   $\overline{DMAK}$ = high
   $\overline{PAUSE}$ = high

Figure 11. Bus Fault Timeout Timing



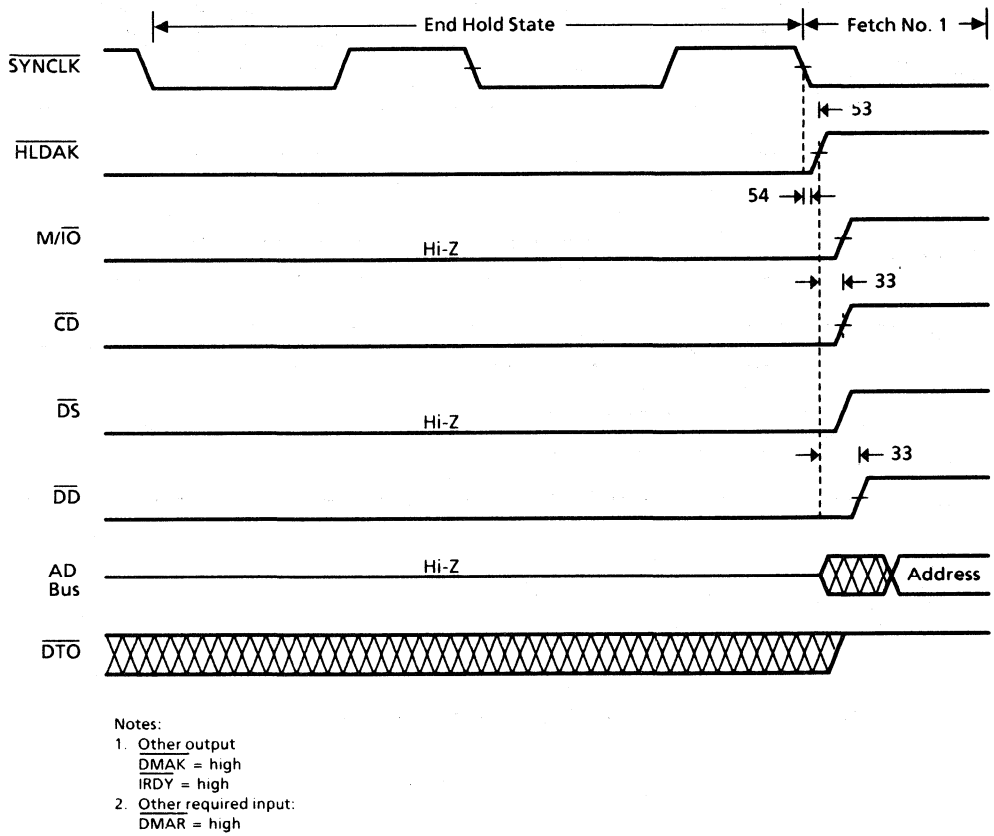
Notes:
1. Assumes only one fault input active at a time.
2. Buffered EXADE
3. Other output:
   IRDY = high
   CD = high

Figure 12. Fault Capture Timing



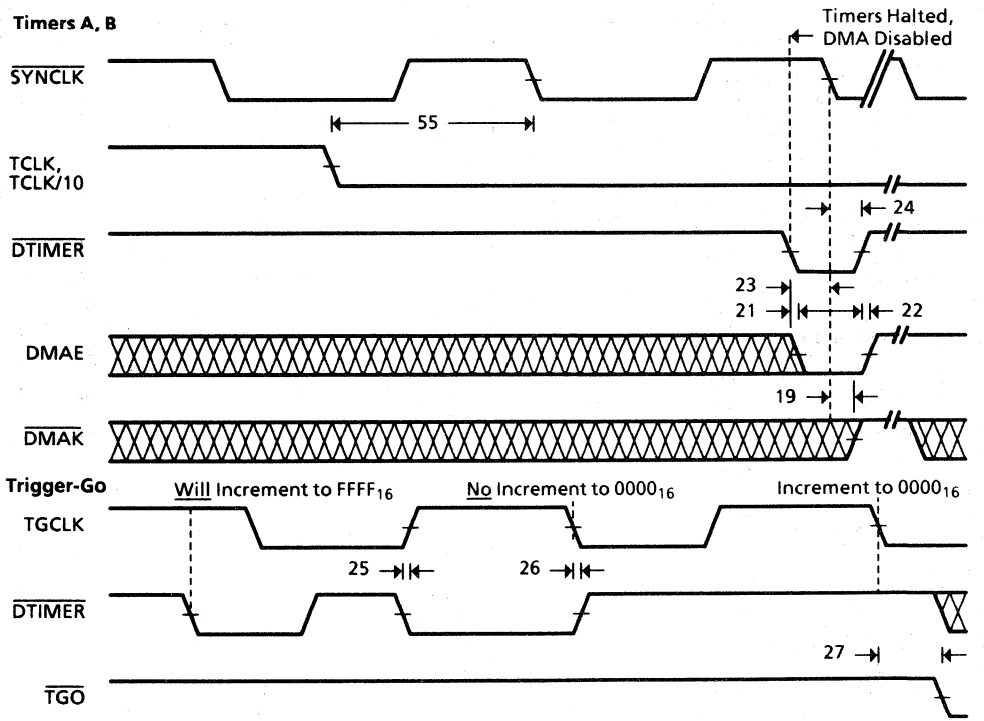
Note:
1. Other output IRDY = high

Figure 13. Hold State Generation Timing



Notes:
1. Other output
   DMAK = high
   IRDY = high
2. Other required input:
   DMAR = high

Figure 14. Hold State Termination Timing



Notes:
1. Other output
   IRDY = high
2. TCLK/10 is the internally derived Timer B clock.
3. Timers A and B are clocked on the second SYNC after TCLK setup time is satisfied.

Figure 15. Timer Operations

No.	Parameter	Test Condition(1)(2)	Min	Typ	Max(3)	Units
1	SYNCLKN ↓ to Data Valid	Load 1	-		3r + 100	ns
2	Data Valid after SYNCLKN ↓	Load 1	10		-	ns
3	SYNCLKN ↑ to IRDYN Valid	Load 1	-		50	ns
4	IRDYN Valid after SYNCLKN ↓	Load 1	10		-	ns
5	SYNCLKN ↓ to IRN Valid	Load 1	-		64	ns
6	IRN Valid after SYNCLKN ↓	Load 1	5		-	ns
7	SYNCLKN ↓ to PIFN Valid	Load 1	-		59	ns
8	PIFN Valid after SYNCLKN ↓	Load 1	5		-	ns
9	SYNCLKN ↓ to SURE, NPU, PAUSEN Valid	Load 1	-		85	ns
10	SURE, NPU, ILLADN, PAUSEN Valid after SYNCLKN ↓	Load 1	15		-	ns
11	SYNCLKN ↓ to ILLADN ↑	Load 1	-		85	ns
12	TCLK ↓ to ILLADN ↓ (Bus Timeout)	Load 1	-		85	ns
13	EXADEN to ILLADN Valid	Load 1	-		70	ns
14	TCLK ↓ to IRDYN ↓ (Bus Timeout)	Load 1	-		50	ns
15	SYNCLKN ↑ to CONFWN Valid	Load 1	-		85	ns
16	CONFWN Valid After SYNCLKN ↓	Load 1	10		-	ns
17	SYNCLKN ↓ to DMAEN Valid	Load 1	-		85	ns
18	DMAE Valid after SYNCLKN ↓	Load 1	5		-	ns
19	SYNCLKN ↓ to DMAKN Valid	Load 1	-		50	ns
20	DMAKN Valid after SYNCLKN ↓	Load 1	5		-	ns
21	DTIMERN ↓ to DMAEN ↓	Load 1	-		70	ns
22	DTIMERN ↑ to DMAEN ↑	Load 1	-		70	ns
23	DTIMERN Setup to SYNCLKN ↓		60		-	ns
24	DTIMERN Hold after SYNCLKN ↓		10		-	ns
25	DTIMERN Setup to TGCLK ↑		60		-	ns
26	DTIMERN Hold after TGCLK ↓		12		-	ns
27	TGCLK ↓ to TGON ↓	Load 1	-		150	ns
28	SYNCLKN ↑ to TGON ↑	Load 1	-		100	ns
29	TGON Valid after SYNCLKN ↑	Load 1	5		-	ns
30	DSN ↓ to DDN ↓	Load 1	10		35	ns
31	DSN ↑ to DDN ↑	Load 1	10		35	ns
32	DMAKN to DDN, CDN Valid	Load 1	-		50	ns
33	HLDAKN to DDN, CDN Valid	Load 1	-		50	ns
34	DMARN Setup to SYNCLKN ↓		30		-	ns
35	DMARN Hold after SYNCLKN ↓		10		-	ns
36	DTON Setup to TCLK ↓		60		-	ns
37	DTON Hold after TCLK ↓		10		-	ns
38	Address/Command Setup to SYNCLKN ↑		90		-	ns
39	Address/Command Hold after SYNCLKN ↑		0		-	ns
40	Data Setup to SYNCLKN ↓		90		-	ns
41	Data Hold after SYNCLKN ↓		0		-	ns
42	Microcode Setup to SYNCLKN ↓		10		-	ns
43	Microcode Hold after SYNCLKN ↓		15		-	ns
44	Interrupts Setup to SYNCLKN ↓		30		-	ns
45	Interrupts Hold after SYNCLKN ↓		10		-	ns
46	Faults Setup to SYNCLKN ↓		30		-	ns
47	Faults Hold after SYNCLKN ↓		10		-	ns
48	Bus Fault Timeout Interval (4)		1		2	TCLK
49	SYNCLKN ↓ to INTREN Valid	Load 1	-		60	ns
50	INTREN Valid after SYNCLKN ↓	Load 1	5		-	ns
51	SYNCLKN ↓ to M/ION Valid	Load 1	-		70	ns
52	M/ION Valid after SYNCLKN ↓	Load 1	5		-	ns
53	SYNCLKN ↓ to HLDAKN Valid	Load 1	-		20	ns
54	HLDAKN Valid after SYNCLKN ↓	Load 1	−7		-	ns
55	TCLK Setup to SYNCLKN ↓		30			ns
56	TCLK Hold after SYNCLKN ↓		10			ns

(1) T_A = + 25°C, -55°C and + 125°C tested at V_{DD} = 4.5V and 5.5V.
(2) Unless otherwise noted: VIL ≥ 0.0 V, VIH ≤ 4.0 V timing measured from 50% to 50% points.
(3) r = 1 OSC period. 0.5r implies 50% OSC duty cycle.
(4) Data obtained by characterization or analysis; not routinely measured.

Table 7. Timing Parameter Values

6.0 Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply voltage	-0.5	7	V
Input voltage	-0.3	V_{DD} + 0.3	V
Current through any pin	-20	20	mA
Operating temperature	-55	125	°C
Storage temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute Maximum Ratings

7.0 DC Electrical Characteristics

Symbol	Parameter	Condition	Total Dose Radiation Not Exceeding $3x10^5$ RAD (Si)			Units
			Min.	Typ.	Max.	
V_{DD}	Supply voltage	V_{SS} = 0	4.5	5.0	5.5	V
V_{IHC}	CMOS Input High Voltage (Note 1)	-	V_{DD}-1	-	-	V
V_{ILC}	CMOS Input Low Voltage (Note 1)	-	-	-	V_{SS} + 1	V
V_{IHT}	TTL Input High Voltage (Note 2)	-	2.0	-	-	V
V_{ILT}	TTL Input Low Voltage (Note 2)	-	-	-	0.8	V
V_{OHC}	CMOS Output High Voltage (Note 1)	I_{OH} = -1.4mA V_{DD} = 4.5V	4.0	-	-	V
V_{OLC}	CMOS Output Low Voltage (Note 1)	I_{OL} = 2.0mA V_{DD} = 5.5V	-	-	0.5	V
V_{OHT}	TTL Output High Voltage (Note 2)	I_{OH} = -1.4mA V_{DD} = 4.5V	3.5	-	-	V
V_{OLT}	TTL Input Output Low Voltage (Note 2)	I_{OL} = 2.0mA V_{DD} = 5.5V	-	-	0.4	V
I_I	Input Leakage Current (Note 3)	V_{DD} = 5.5V V_{IN} = 0V or 5.5V	-	-	±10	uA
I_{OZ}	Output Leakage Current (Note 3)	V_{DD} = 5.5V V_O = 0V or 5.5V	-	-	±50	uA
I_{DDOP}	Operating Supply Current	V_{DD} = 5.5V SYNCLKN = 4MHz	-	5	14	mA
I_{DDST}	Static Supply Current	V_{DD} = 5.5V SYNCLKN = 0MHz	-	3	10	mA

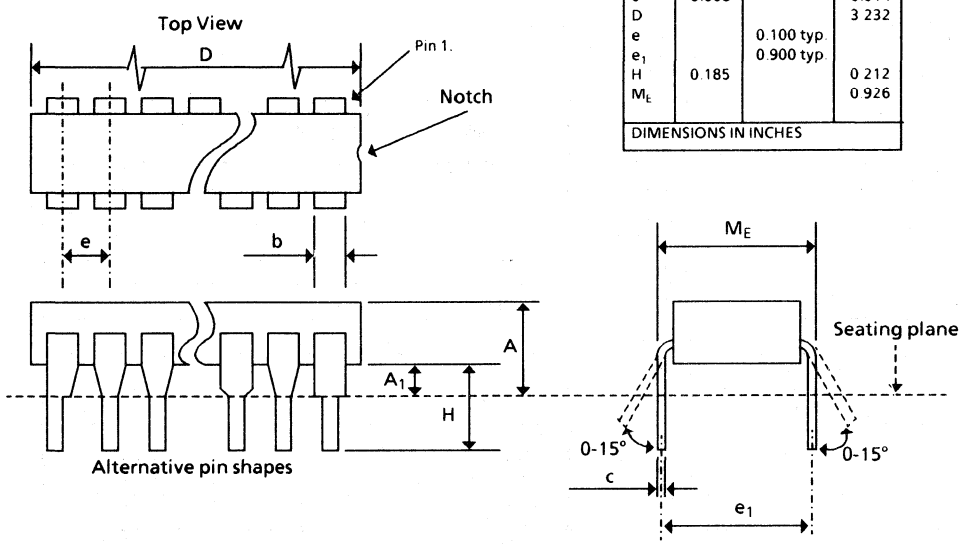
Notes:
1 The following signals are CMOS compatible:
  a. CMOS inputs: INTREN, Microcode Bus (M04, M05, M06), HLDAKN and SYNCLK.
  b. CMOS outputs: PIFN, IRN and IRDYN.
2 The following signals are TTL compatible:
  a. TTL inputs: DTIMEN, TGCLK, MPROEN, DMAPEN, EXADEN, PIOXEN, FLT7N, SYSFN, OVIN, PWRDN, INT02N, INT08N, INT10N, INT11N, INT12N/IOI1N, INT13N, INT14N/IOI2N, INT15N, DTON, DSN, M/ION, DMARN, TCK and TSTOPN
  b. TTL outputs: SURE, NPU, DDN, TGON, CDN, PAUSEN, ILLADN, CONFIG, DMAKN and DMAE
  c. TTL I/O signal: Address/Data Bus (AD00-AD15)
3 Worst case at T_A = + 125°C, guaranteed but not tested at T_A = -55°C

Table 9. Operating DC Electrical Characteristics

8.0 Packaging Information

Ceramic Dual-in-line
(Package type C)

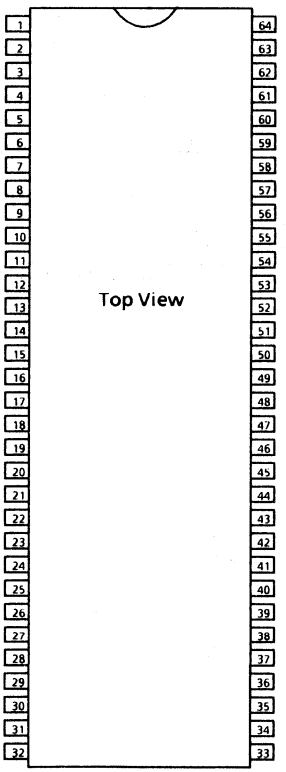
Ref.	Min.	Nom.	Max.
A			0.220
A_1	0.015		0.060
b	0.014		0.023
c	0.008		0.014
D			3.232
e		0.100 typ.	
e_1		0.900 typ.	
H	0.185		0.212
M_E			0.926
DIMENSIONS IN INCHES			



Figures 16a. Dimensioned Drawing

MA17503

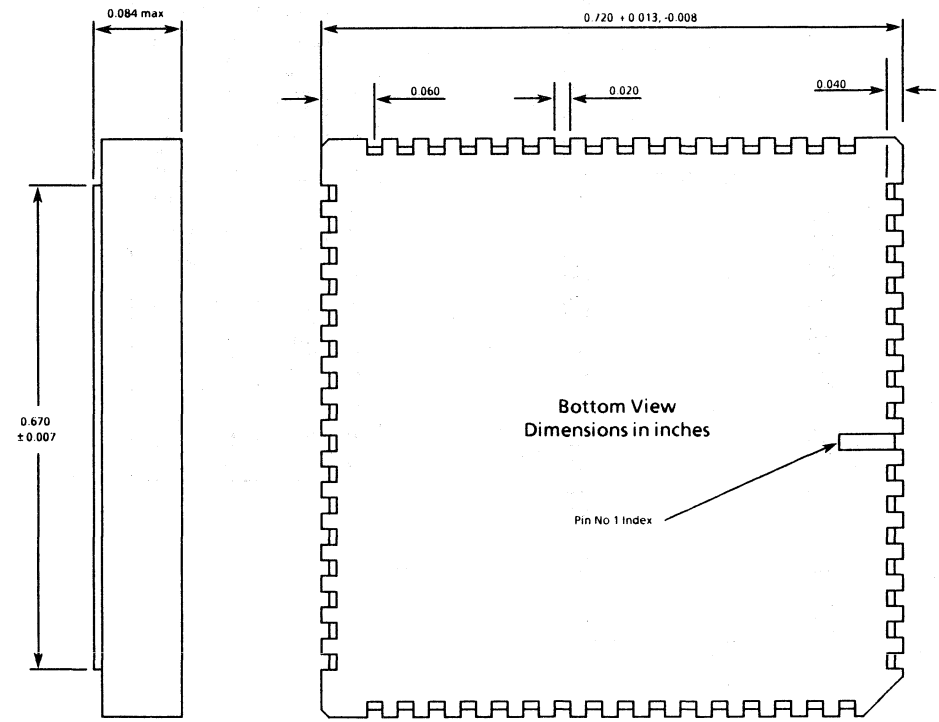
MIL-STD-1750A Interrupt Unit



1	ILLADN	33	MSTOPN
2	DTON	34	SURE
3	SYNCLKN	35	NPU
4	DSN	36	DDN
5	INTREN	37	DTIMERN
6	CONFWN	38	TGON
7	IRDYN	39	TGCLK
8	M/ION	40	CDN
9	DMAKN	41	PIFN
10	DMAE	42	MPROEN
11	DMARN	43	MPEN
12	M04	44	PIOPEN
13	M05	45	DMAPEN
14	M06	46	EXADEN
15	TCLK	47	PIOXEN
16	AD00	48	FLT7N
17	AD01	49	SYSFN
18	AD02	50	VDD
19	AD03	51	IRN
20	AD04	52	PAUSEN
21	AD05	53	OVIN
22	AD06	54	PWRDN
23	AD07	55	INT02N
24	AD08	56	INT08N
25	AD09	57	INT10N
26	AD10	58	INT11N
27	AD11	59	IOI1N
28	AD12	60	INT13N
29	AD13	61	IOI2N
30	AD14	62	INT15N
31	AD15	63	HLDAKN
32	GND	64	NC

Figures 16b. Pin Assignments

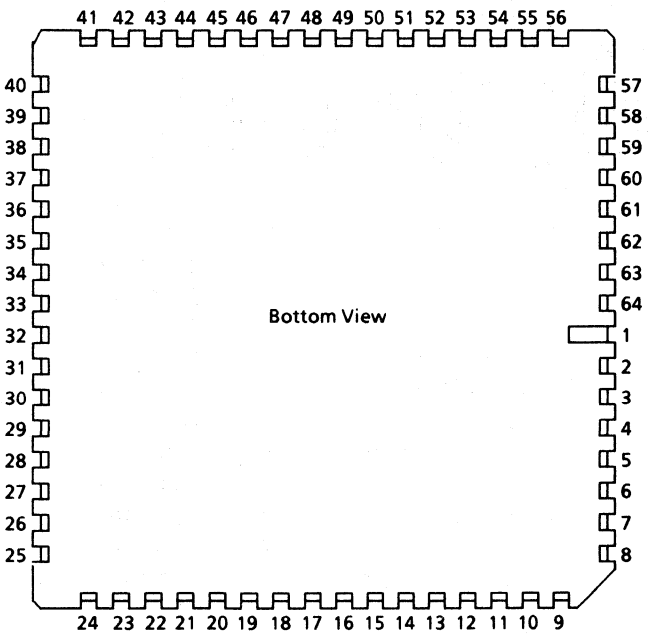
Leadless Chip Carrier
(Package type L)



Figures 17a. Dimensioned Drawing

MA17503

MIL-STD-1750A Interrupt Unit

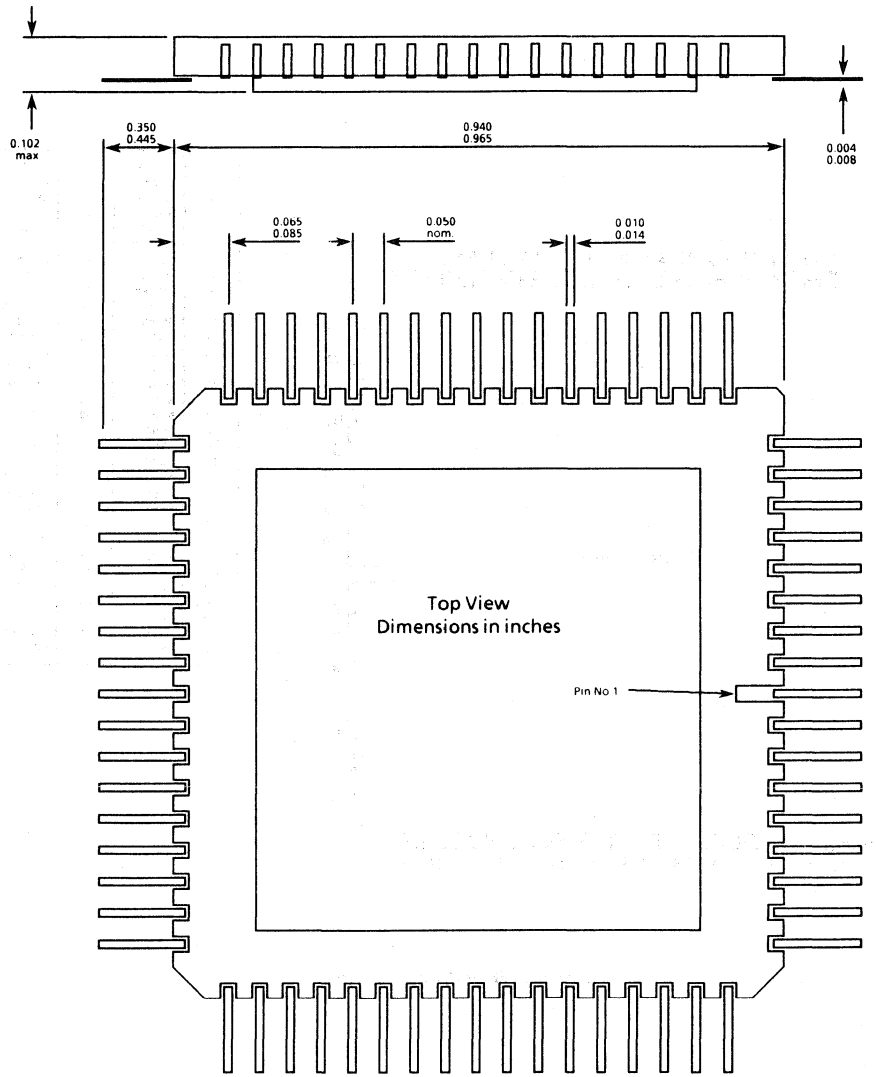


1	ILLADN	33	MSTOPN
2	DTON	34	SURE
3	SYNCLKN	35	NPU
4	DSN	36	DDN
5	INTREN	37	DTIMERN
6	CONFWN	38	TGON
7	IRDYN	39	TGCLK
8	M/IION	40	CDN
9	DMAKN	41	PIEN
10	DMAE	42	MPROEN
11	DMARN	43	MPEN
12	M04	44	PIOPEN
13	M05	45	DMAPEN
14	M06	46	EXADEN
15	ICLK	47	PIOXEN
16	AD00	48	FLT7N
17	AD01	49	SYSFN
18	AD02	50	VDD
19	AD03	51	IRN
20	AD04	52	PAUSEN
21	AD05	53	OVIN
22	AD06	54	PWRDN
23	AD07	55	INT02N
24	AD08	56	INT08N
25	AD09	57	INT10N
26	AD10	58	INT11N
27	AD11	59	IOI1N
28	AD12	60	INT13N
29	AD13	61	IOI2N
30	AD14	62	INT15N
31	AD15	63	HLDAKN
32	GND	64	NC

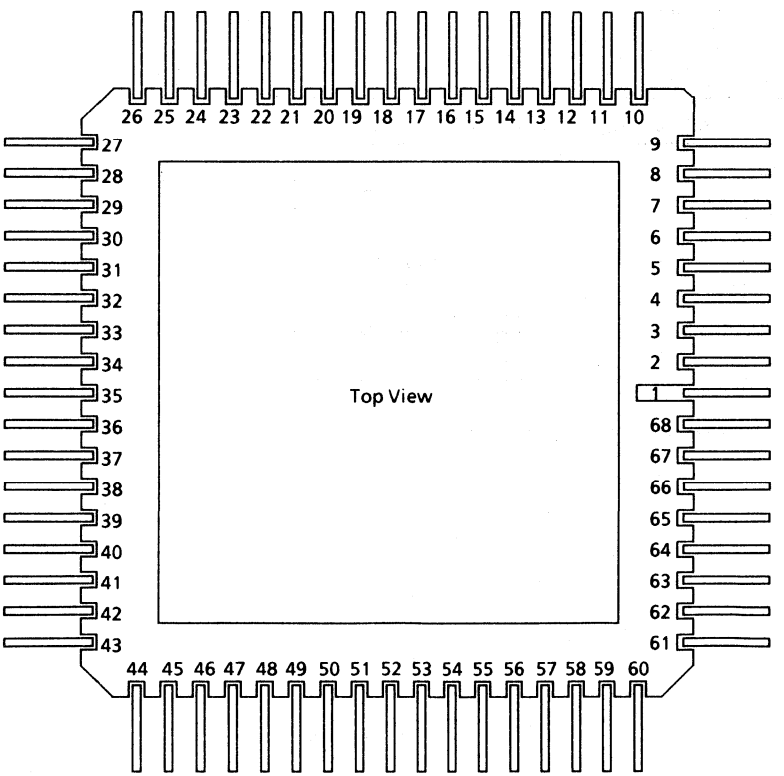
Figures 17b. Pin Assignments

GEC PLESSEY
SEMICONDUCTORS

Topbraze Flatpack
(Package type F)



Figures 18a. Dimensioned Drawing



1	NC
2	ILLADN
3	DTON
4	SYNCLKN
5	DSN
6	INTREN
7	CONFWN
8	IRDYN
9	M/ION
10	DMAKN
11	DMAE
12	DMARN
13	M04
14	M05
15	M06
16	TCLK
17	AD00
18	AD01
19	AD02
20	AD03
21	AD04
22	AD05
23	AD06
24	AD07
25	AD08
26	NC
27	AD09
28	AD10
29	AD11
30	AD12
31	AD13
32	AD14
33	AD15
34	NC
35	GND
36	MSTOPN
37	SURE
38	NPU
39	DDN
40	DTIMERN
41	TGON
42	TGCLK
43	CDN
44	PIFN
45	MPROLN
46	MPEN
47	PIOPEN
48	DMAPEN
49	EXADEN
50	PIOXEN
51	FLT7N
52	SYSFN
53	VDD
54	NC
55	IRN
56	PAUSEN
57	OVIN
58	PWRDN
59	INT02N
60	INT08N
61	INT10N
62	INT11N
63	IOI1N
64	INT13N
65	IOI2N
66	INT15N
67	HLDAKN
68	NC

Figures 18b. Pin Assignments

9.0 Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

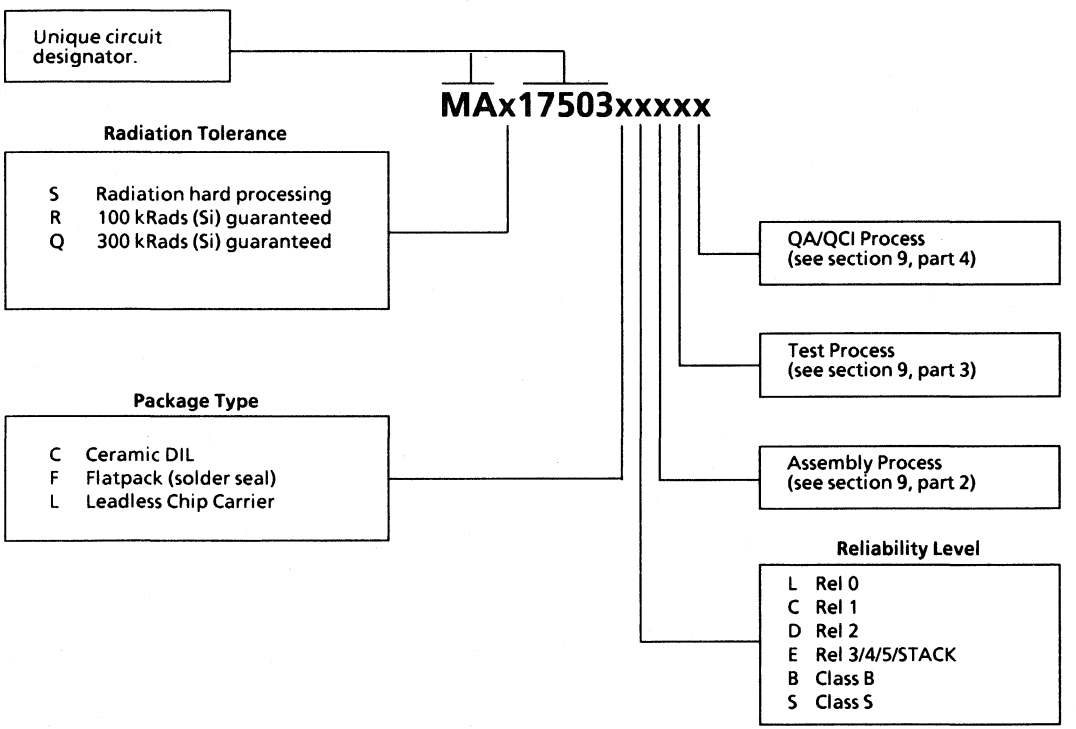
Total Dose (Function to specification, note 1)	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$1x10^{10}$ Rad(Si)/s
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/s
Neutron Hardness (Function to specification)	$1x10^{15}$ neutrons/cm2
Latch-up	Not possible
Single Event Upset (note 2)	$<10^{-10}$ errors/bit day

Note 1. Typical performance only, for guaranteed levels see ordering information.
2. GSO 10% Worst Case

MA17503
MIL-STD-1750A Interrupt Unit

10.0 Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



section 3

PERIPHERALS & SUPPORT CIRCUITS

GEC PLESSEY

SEMICONDUCTORS

S10212ADF Issue 1.1 December 1990

MA31751

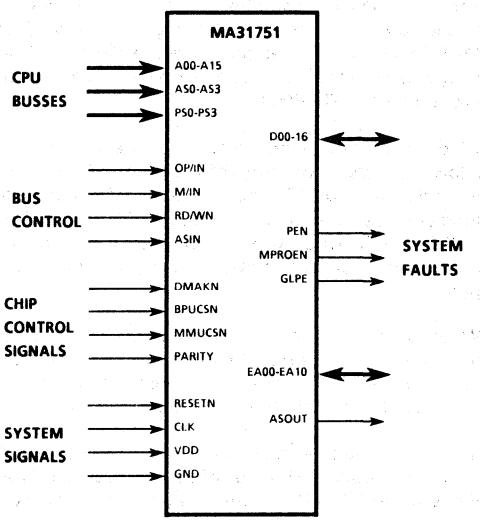
Memory Management Unit & Block Protect Unit

(Advanced data)

Features

- **MIL-STD-1750A/B compatible**
- **Radiation Hard CMOS/SOS Technology**
- **User Configurable as Either a Memory Management Unit (MMU) or a Block Protect Unit (BPU) or both**
- **Memory Management Unit Configuration**
  - **1M-Word Physical Address Space**
  - **Access Lock and Key of 4K-Word Blocks**
  - **Write/Execute Protection of 4K-Word Blocks**
- **Block Protect Unit Configuration**
  - **Protection of 1K-Word Blocks**
  - **Global Memory Write Protection during Initialisation**
- **Direct Memory Access Support**

Block Diagram



General Description

The Marconi Electronic Devices MA31751 Memory Management Unit / Block Protect Unit (MMU/BPU) is an optional chip which may be used to expand the capabilities of the basic MA31750 CPU.

User configurable, the MA31751 can perform as an MMU a BPU or both MMU and BPU, conforming to MIL-STD-1750A. MMU mapping and BPU protection for 1M words of memory is provided by the internal memory. Zero wait state operation is possible, with one wait state added when the CPU address crosses one or more page boundaries. Up to 16 MA31751 devices can be used to give 16M words of logical mapped onto 8M words of physical address space with protection in 1750B mode.

The MA31751 is designed to have a simple interface to both the CPU and the system bus with the minimal number of control lines. This minimises board space and simplifies system design.

The MA31750 traps the MMU and BPU XIO commands to program and read the logical to physical mapping and memory access control.This provides simple memory management as defined by the MIL-STD-1750A.

Memory Management Unit & Block Protect Unit

(Advanced data)

1 Device Operation

The MA31751 is a complex interface device designed to increase the memory addressing capability of the MA31750 CPU. It is user configured as either an MMU or a BPU conforming to the MIL-STD-1750A and the proposed MIL-STD-1750B.

When operated as an MMU the internal memory allows addressing of upto 1M words (MIL-STD-1750A). By using eight MA31751 devices, upto 8MWords of real memory may be addressed (proposed MIL-STD-1750B). Full access lock/key protection is provided in both modes together with write/execute protection on 4k pages.

When operated as a BPU the internal BPU memory allows up to 1M words of memory to be protected in 1K blocks(MIL-STD-1750A). Up to 8M words may be protected by multiple MMU/BPU units.

In 1750A mode one unit will act as both MMU and BPU for the maximum 1M words of address space. In 1750B mode up to 8 MA31751 units may be used to provide MMU and BPU functions. For any given physical memory location the MMU and BPU function may be split across two MA31751 devices depending on the logical to physical address mapping.

1.1 Initialisation

The MA31751 is initialised by the CPU BIT (Built in test) when a system reset occurs, initially all mappings are set to zero to give a linear 1M words logical to physical mapping, the BPU defaults to no protection on a reset and requires 256 clock cycles to set the internal BPU memory. The CPU recognises the presence of the MMU by the setting of bit s 0, 3 and 5 in the configuration register. The CPU may change the mapping and access protection when it is privileged instruction mode using XIO commands 4D00 to 52FF as defined in MIL-STD-1750A.

1.2 Direct Memory Access

The MA31751 supports DMA access within the expanded memory space, including translation and protection.

1.3 Address translation and protection

The MMU maps system memory into 4k word pages by the mechanism shown in figure 1. The 512 page registers are organized into 16 pairs of groups, one group for instruction memory space and one group for data memory space. Each group contains 16 page registers accommodating a total of 256 registers for each of data and instruction memory space.

The MMU also checks for protection violation by comparing the processor state (PS) to the access lock (AL) field in the page register. Protection is also provided by examining the write protect bit (W in operand page register) if data is to be written, or the execute protect bit (E in instruction page register) if an instruction is to be read. If a violation occurs, the memory protect output is asserted and the current instruction is aborted. Table 1 illustrates the Access Key mapping mechanism.

AL Code	Acceptable Access Key Codes
0	0
1	0,1
2	0,2
3	0,3
4	0,4
5	0,5
6	0,6
7	0,7
8	0,8
9	0,9
A	0,A
B	0,B
C	0,C
D	0,D
E	0,E
F	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F

Table 1: Access Lock and Key Mapping

When memory transactions are controlled by the MA31750, the AS0-AS3 and PS0-PS3 bits necessary to perform the address translation and access protection functions, respectively, are obtained from the processor. If a DMA controller is performing memory transactions, it must provide the proper AS0-AS3 and PS0-PS3 signal inputs to the MMU for address translation and access protection.

MA31751

Memory Management Unit & Block Protect Unit

(Advanced data)

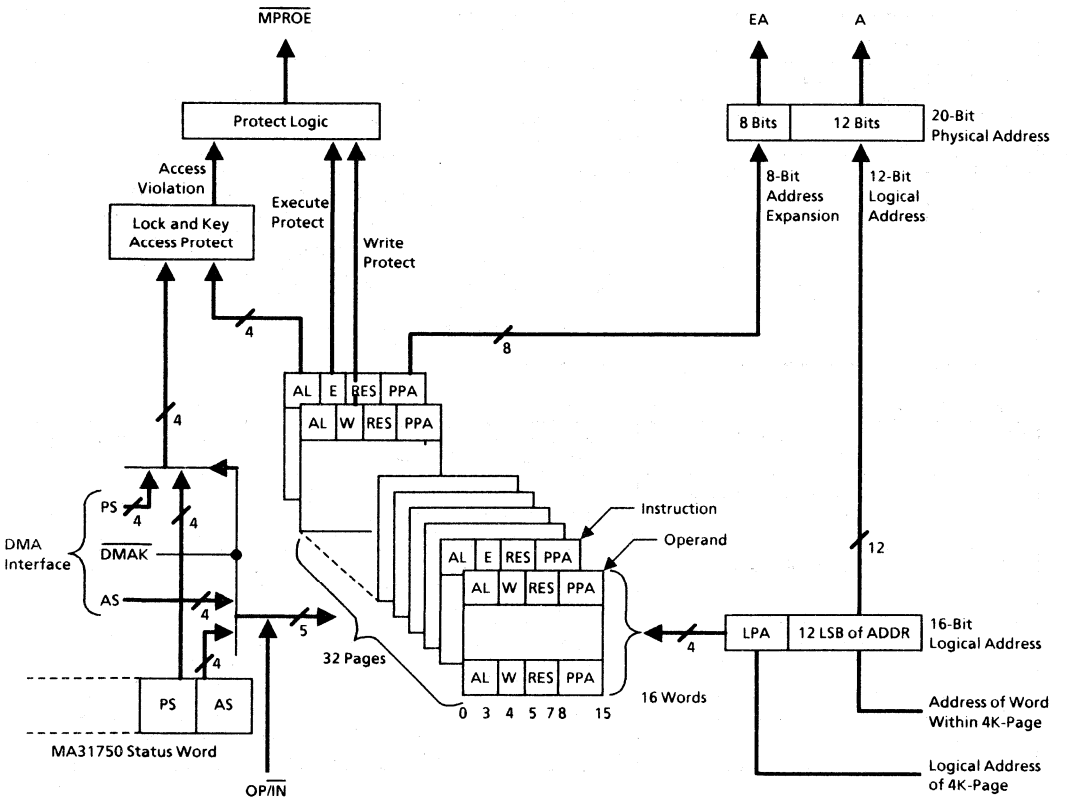


Figure 1: MMU Mapping Mechanism

2 Signal Definitions

Pin Name	Pin Nº	Function	Description
SYSTEM BUSSES			
A00-A15		Processor Address Bus	An active-high address bus for addresses and XIO commands. A15 is the LSB.
D00-D16		System Data Bus	Data bus used to transfer XIO data to and from the MMU/BPU. D15 is the LSB and D16 is the parity bit.
EA00-EA10		Extended Adress Bus	If the MMU section is selected (using MMUCSN) then EA00-EA10 provides the system extended address. This should be combined with A04-A15 from the processor to give the full 20 bit (1750A) or 23-bit (1750B) system address bus. During XIO transfers between the CPU and the MA31751 EA06 drops low to indicate that the MMU transfer has completed. When gated with M/ION low this signal may be used as a Ready indication to the CPU. During XIO transfers not involving the MMU/BPU, EA7-10 mimic A00-A03 to present the full processor address to the system. When the MMU is not selected, EA03-10 become inputs to allow the BPU to protect the appropriate section of extended memory.
BUS CONTROL			
ASIN		Address Strobe In	The rising edge of this active-high signal generated by the CPU or DMA controller indicates that a valid address is present on A00-15.
ASOUT		Extended Address Strobe	The rising edge of this active-high signal indicates that a valid and stable extended address is available from the MA31751. This pin becomes an input when no MMU is selected and should be driven from the system address strobe.
MION		Memory/IO Select	This input is used to select between normal operation and command transfer (XIO) mode. A high indicates memory whilst a low indicates IO. This signal is provided by the CPU or DMA controller.
RDWN		Read/Write Select	This input indicates the direction of data transfer on the data bus. A high level indicates that the processor is reading the bus whilst a low level indicates that the processor is driving the bus. This signal is provided by the CPU or DMA controller.
OPIN		Operand/Instruction Select	This input indicates the type of data which is currently on the data bus. A high level indicates operand data whilst a low level indicates the presence of instruction data. This signal is provided by the CPU or DMA controller.
EXTENDED MEMORY CONTROL			
AS0-AS3		Address State	Address state bus from either the MA31750 or an optional DMA controller. This is used in the MMU as part of the page selection operation. If no MMU function is required these inputs should be tied to GND.
PS0-PS3		Processor State	Processor state bus from either the MA31750 or an optional DMA controller. This is used in the MMU to provide lock and key protection on page accesses, and should be tied to GND if no MMU is required.

2 Signal Definitions (continued)

Pin Name	Pin No	Function	Description
ERROR INDICATION			
MPROEN		Memory Protect Error	This output is asserted low following an access fault, memory protect or write protect from the MMU, or a block protect error from the BPU.
PEN		Parity Error	This active-low output is asserted low if a parity error is detected during an MMU/BPU internal operation or an XIO command transfer.
MISCELLANEOUS			
RESETN		System Reset	Device reset input. Should be connected to system reset.
MMUCSN		MMU Chip Select	A low on this input indicates that the MMU function within the device is required. In a 1750A system this input should be tied to GND. In 1750B this input should be derived by decoding the PB0-3 bus from either the MA31750 or an optional DMA controller. Note that in 1750B mode one MA31751 device is required per implemented page bank.
BPUCSN		BPU Chip Select	A low on this input indicates that the BPU function within the device is required. In a 1750A system this input should be tied to GND or RW/WN. In 1750B this input should be derived by decoding the EA0-2 bus from the active system MMU. Note that the MA31751 can only support 1MWord of block protection internally; to protect the full 8MWord address space requires eight such devices.
DMAKN		DMA Acknowledge	This active-low input is used to select between the CPU and DMA page and protection registers within the MA31751, and should be asserted low when the CPU has relinquished control to a DMA controller on the system.
GLPE		Global Protect Enable	This active-high signal goes high in BPU mode following a system reset to indicate that the memory system is globally write-protected The signal is set low by the XIO MPEN command.
PARITY		Set internal parity	Sets the parity to odd or even on the internal BPU and MMU memory.
POWER			
VDD		Power supply	DC power supply input
GND		Ground	0V reference point.

3.0 Timing Considerations

The MA31751 gives zero wait state operation for memory translations when address changes do not cross a 4K page boundary. This is achieved by using two fast translation cache registers,one for instruction transfers and one for operand transfers. This is done because instruction and operand words often occur in different pages. The appropriate translation cache register is chosen by the operand/instruction (O/IN) signal. When either the instruction or the operand address crosses a page boundary one wait state is incurred while the translation cache register is updated from the internal memory. This system minimises the MMU overhead. Asimilar caching scheme is employed in the BPU section of the device to allow more rapid detection of access violations.

3.1 Block Protection

The BPU section of this device allows any 1K word block to be made unavailable to the system. Any attempt to read or write a protected block will result in an access violation being produced by the BPU if BPUCSN is low. If only write protection is required of the BPU then the BPUCSN should be qualified by the RDWN (read-write) signal from the CPU.

3.1 Timing Diagrams (continued)

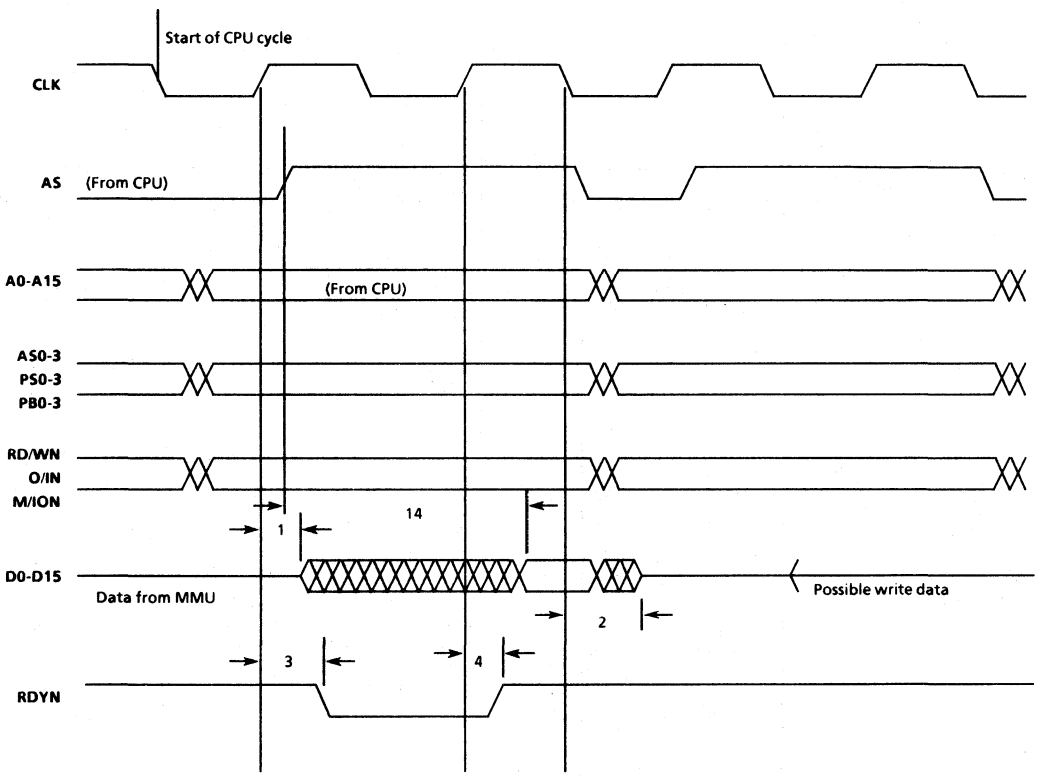


Figure 2: MMU internal XIO read

3.1 Timing Diagrams (continued)

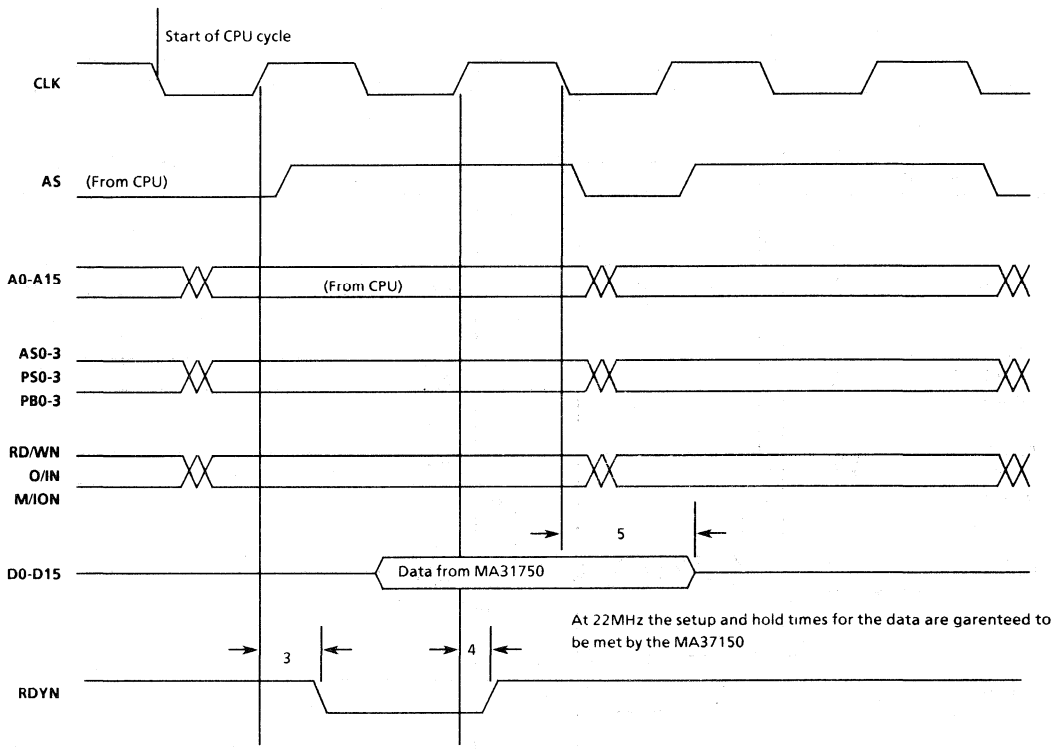


Figure 3: MMU internal XIO write

3.1 Timing Diagrams (continued)

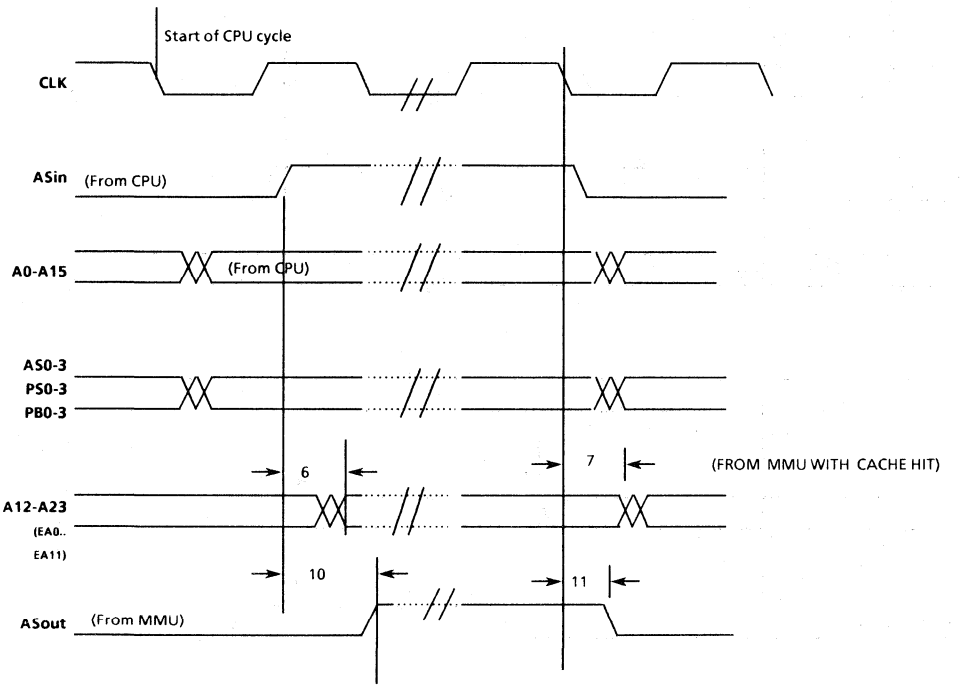


Figure 4: MMU Address translation from translation cashe

3.1 Timing Diagrams (continued)

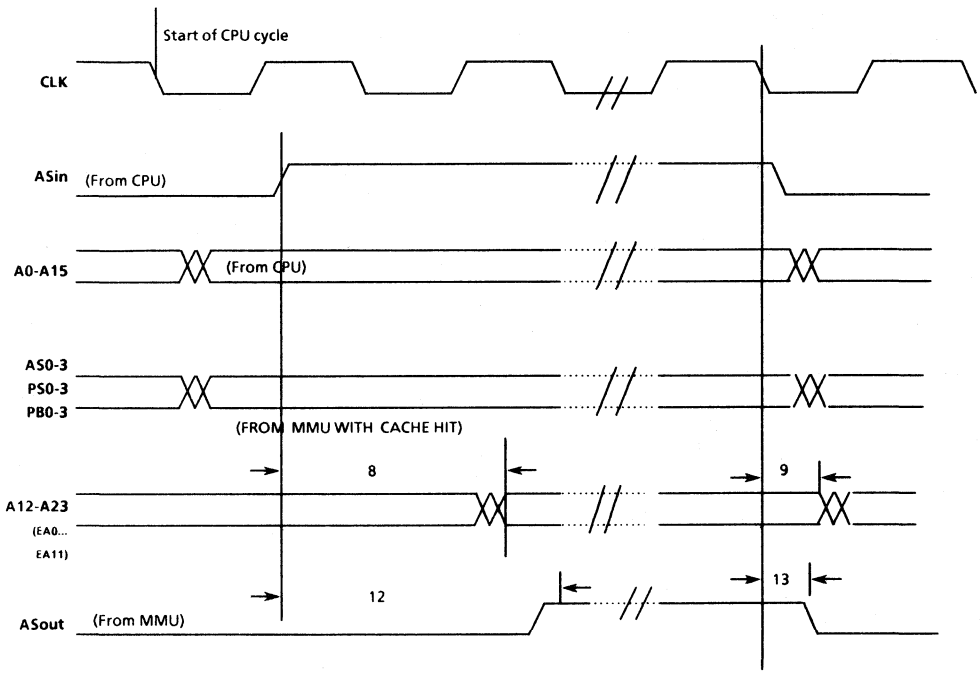


Figure 5: MMU Address translation from translation memory

4 Timing Parameters

No.	Parameter	Min.	Typ.	Max.	Units
1	CPU AS ↑ to data bus active	-	10	-	ns
2	Address hold after AS ↓	-	10	-	ns
3	CPU AS ↑ to RDYN ↓	-	5	-	ns
4	Min RDYN ↓ hold time	-	5	-	ns
5	Data bus active hold time	-	10	-	ns
6	CPU AS ↑ to address stable (with cache hit)	-	10	-	ns
7	Address hold time after CPU cycle (with a cache hit)	5	-	-	ns
8	CPU AS ↑ to address stable (with a cache miss)	10	-	-	ns
9	Address hold time after CPU cycle (with a cache miss)	-	5	-	ns
10	AS ↑ to ASOUT ↑ (with cache hit)	-	-	15	ns
11	AS ↑ hold time (with cache hit)	-	5	-	ns
12	AS ↑ to ASOUT ↑ (with a cache miss)	-	65	-	ns
13	AS ↑ hold time (with a cache miss)	-	5	-	ns
14	AS ↑ to data from MMU valid	-	45	-	ns

Table 2: Timing Parameters - PRELIMINARY INFORMATION ONLY

5 DC Electrical Characteristics

Symbol	Parameter	Condition	Total Dose Radiation Not Exceeding $3x10^5$ RAD (Si)			Units
			Min.	Typ.	Max.	
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	TTL Input High Voltage	-	2.0	-	-	V
V_{IL}	TTL Input Low Voltage	-	-	-	0.8	V
V_{OH}	TTL Output High Voltage	V_{DD} = 4.5V I_{OH} = -1.4mA	3.5	-	-	V
V_{OL}	TTL Output low Voltage	V_{DD} = 5.5V I_{OL} = 2.0mA	-	-	0.4	V
I_I	Input Leakage Current	V_{DD} = 5.5V V_{IN} = 0V or 5.5V	-	-	± 10	uA
I_{OZ}	Output Leakage Current	V_{DD} = 5.5V V_O = 0V or 5.5V	-	-	± 50	uA
I_{DDOP}	Operating Power Supply Current	V_{DD} = 5.5V AS = 10MHz	-	10	35	mA
I_{DDST}	Static Power Supply Current	V_{DD} = 5.5V	-	5	15	mA

V_{DD} = 5V ± 10%, over full operating temperature range.

Table 3: Operating DC Electrical Characteristics

6 Packaging Information

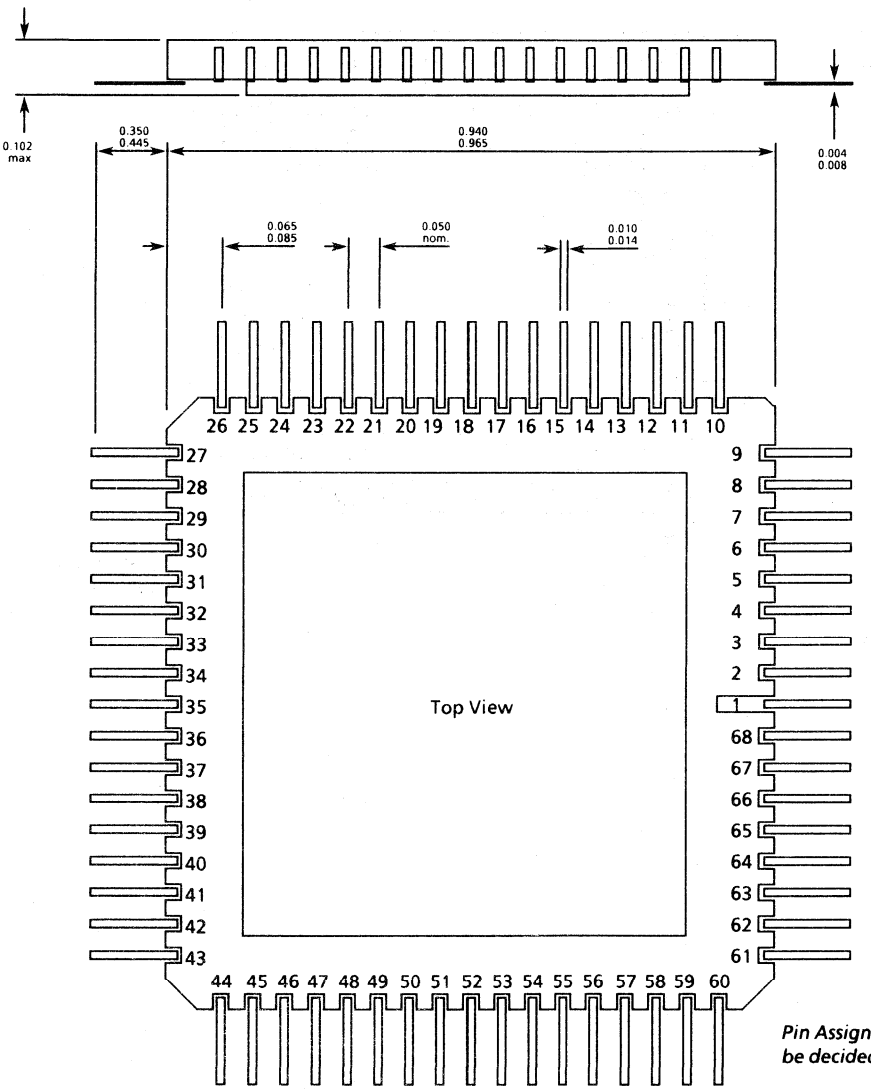
The MA31751 will initially be available in 68 pin, lead flatpack and pin grid array to compliment the MA31750.

MA31751

Memory Management Unit & Block Protect Unit

(Advanced data)

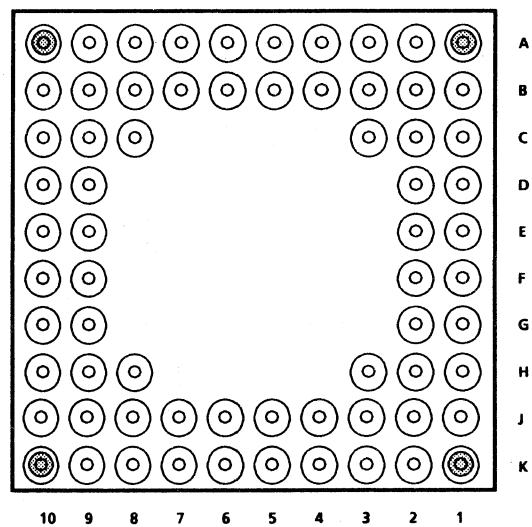
Lead Flatpack (Package type - F)



Pin Assignments to be decided

Dimensioned Drawing

Pin Grid Array



Pin Assignments to be decided

7 Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

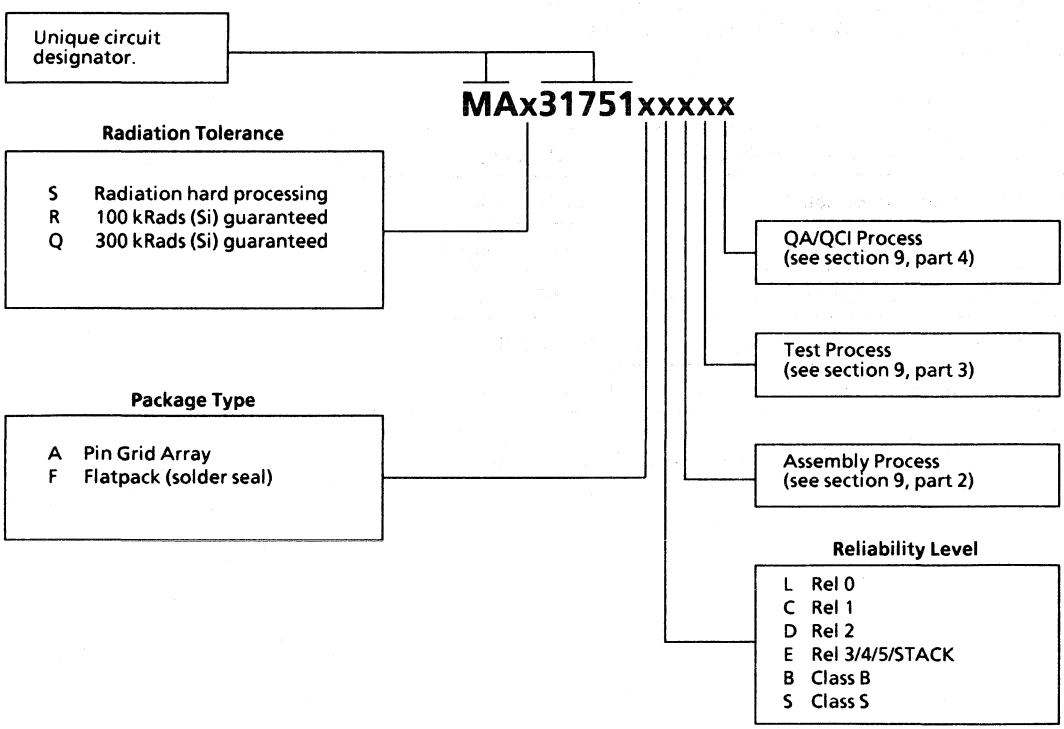
Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

Total Dose (Function to specification, note 1)	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$3x10^{10}$ Rad(Si)/s
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/s
Neutron Hardness (Function to specification)	$1x10^{15}$ neutrons/cm2
Latch-up	Not possible
Single Event Upset (note 2)	$<10^{-10}$ errors/bit day

Note 1. Typical performance only, for guaranteed levels see ordering information.
2. GSO 10% Worst Case

8 Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



S10208FDS Issue 1.3 October 1990

MA17504

MIL-STD-1750A Memory Management Unit/ Block Protect Unit

Features

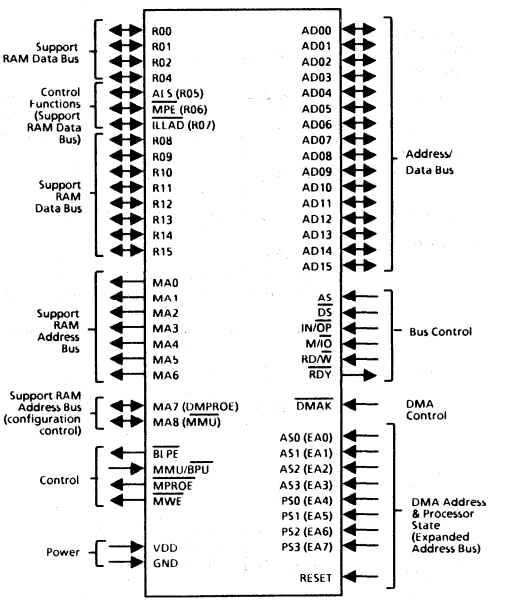
- Implements Expanded Address and Block Protect Options of the MIL-STD-1750A (Notice 1) Architecture
- Full Performance over Military Temperature Range (-55°C to + 125°C)
- Low Power, Radiation Hard CMOS/SOS Technology
- User Configurable as Either a Memory Management Unit (MMU) or a Block Protect Unit (BPU) or Use of Two Devices Provides Both MMU and BPU Capabilities
- Memory Management Unit Configuration
  - 1M-Word Physical Address Space Organized into 64K-Word pages
  - Access Lock and Key of 4K-Word Blocks
  - Write/Execute Protection of 4K-Word Blocks
  - Memory Fault Status Register
- Block Protect Unit Configuration
  - Write Protection of 1K-Word Blocks within 64K-Word Address Space On-Chip Capability
  - Global Memory Write Protection during Initialisation
- Direct Memory Access Support
- MAS281 Integrated BIT
- TTL Compatible Interface

General Description

The Marconi Electronic Devices MA17504 Memory Management Unit / Block Protect Unit (MMU/BPU) is an optional fourth chip which may be used to expand the capabilities of the basic MAS281 three chip set. User configurable, the MA17504 can perform as an MMU or a BPU or, two MA17504 units used together can provide both MMU and BPU capabilities.

The MAS281 is a module carrying 3 integrated circuits, an Execution Unit (EU), Control Unit (CU), and Interrupt Unit (IU) and constitutes a minimum CPU configuration providing the following:

Block Diagram



(1) Full implementation of the MIL-STD-1750A (Notice 1) instruction set, (2) 64K-word address space, (3) Interrupt and fault interfaces, (4) Two timers, (5) Trigger-go counter, (6) DMA interface, and (7) HOLD interface.

In addition to being available as the MAS281 module, the units are also available as individual chips and numbered MA17501 to MA17503 respectively. Figure 1 shows the relationship between the MAS281 chip set components and two MA17504's being used in MMU and BPU configurations.

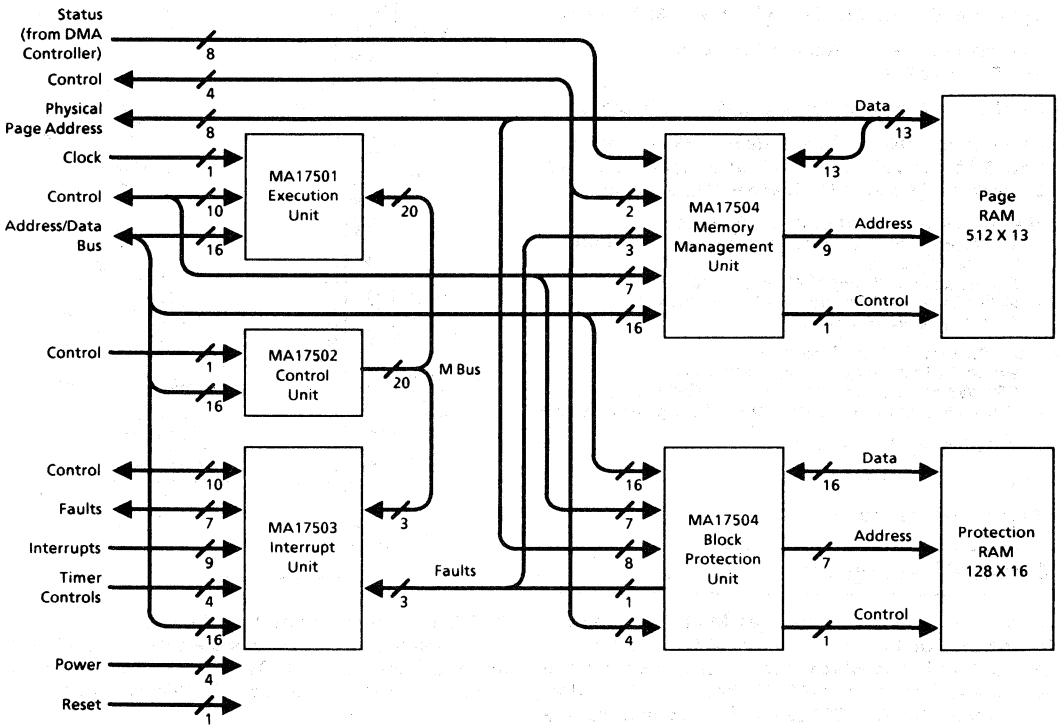


Figure 1. MAS281 Chip Set with Optional MA17504s and Support RAMs

MA17504

MIL-STD-1750A Memory Management Unit/ Block Protect Unit

1.0 System Considerations

Throughout this data sheet, active low signals are denoted either by a bar over the signal name or by an "N" following the signal name, e.g., DMAKN. In those cases where a signal has a dual function, both function names are separated by a "/". The function name to the left of the "/" is active high while the function to the right is active low with an "N" suffix, e.g., MPEN. When signal pins may perform as either an MMU or a BPU and are shown together, the BPU function is shown second and is enclosed in parentheses, e.g., AS0(EA0).

Configured as an MMU, the MA17504 expands the chip set address space to 1M-words while simultaneously providing both access lock and key and write protection of 4K-word blocks. Configured as a BPU, the MA17504 provides write protection down to 1K-word blocks. Two MA17504 devices may be incorporated into the same system to provide both MMU and BPU features simultaneously.

The MA17504 chip, when configured as an MMU, requires the following external support circuitry: (1) A 512-word by 13 bits/word memory to implement the memory mapping lookup tables, and (2) An 8-bit transparent latch (optional) to buffer the expanded address bits. When configured as a BPU in systems with 64K-words of memory or less, the chip needs no external support circuitry. In systems having between 64K-words and 1M-words of memory, the BPU requires an external 128-word by 16-bits/word memory.

The MA17504 utilises a single 5V power supply. All pins are protected against Electrostatic Discharge (ESD) and all signals are TTL compatible.

The use of silicon-on-sapphire technology significantly reduces parasitic capacitances in comparison to bulk technologies and, as a result, allows very fast circuits to be realised. Other advantages are immunity to latchup as well as intrinsically high resistance to transient radiation and single event upset.

1.1 Configuration Word

The 1750 chip set requires an external Configuration Register to indicate the presence of user optional hardware. Following removal of RESET, the MAS281 reads the configuration word from the external Configuration Register in order to initialize the hardware at the specified RESET state. In addition, this permits the start-up software to establish user-defined address translation and memory access protection criteria. The MAS281 also reads the configuration word when a Breakpoint (BPT) is encountered to determine the presence of a console. If a console is not implemented, the BPT executes as a NOP instruction.

The Configuration Register bits provide the configuration information as defined in Table 1 below.

Bit	Device
15	Console
14	MMU
13	BPU
12	Output Discrete Register
11-0	Unused

Table 1. Configuration Register Assignment

2.0 Operational Characteristics

MMU(BPU) operational characteristics may be broken down into initialisation, normal instruction execution, memory and IO support, and direct memory access support. These modes of operation are discussed below.

2.1 Initialisation

Upon application of power and removal of RESET, the CU will enter a microprogram sequence which initialises the MAS281 chip set, performs a Built-In Test (BIT), and effects a system restart.

The initialisation of the MMU, when implemented, activates "group 0" of the page registers, thereby creating a logical to physical map. In addition, the AL, W, and E fields of all page registers are zeroed. Since the Instruction Counter in the MAS281 is initialised to zero concurrently with the logical to physical address mapping initialisation, program execution will therefore begin with the instruction located at address zero. Alternatively, a Start-Up ROM may be defined to accept initial program control instead of beginning in local memory.

The initialisation of the BPU, when implemented, zeros the write protection table and activates the global memory protection. The global protect enable function protects the entire CPU/DMA memory space while software writes the protection tables to the block protect RAM. The global protect enable function (BLPEN signal) is disabled by the Memory Protect Enable (MPEN) software instruction.

The manner in which the MMU is exercised during power-up BIT is a function of the microcode stored in the CU chip. For a discussion of this BIT procedure refer to the MAS281 data sheet. Timing characteristics for the various signals mentioned in the initialisation sequence are also discussed.

2.2 Instruction Execution

The instruction set executed by the chip set is defined by the microcode stored in the CU and is in accordance with MIL-STD-1750A. For a discussion of this instruction set, refer to the MAS281 data sheet. A subsequent section of this data sheet entitled "Timing Characteristics" defines MMU/BPU signal timing associated with instruction execution.

2.3 Memory and IO

All interface transactions are monitored to ensure timely completion. A hardware time-out circuit is enabled at the start of each memory and input/output transaction. If the circuit is not reset within the allotted time by the successful completion of the current transaction (i.e., RDYN not asserted low), the circuit will time-out, terminate the current transaction, cause ILLADN to drop low, and set bit 8 of the fault register for a memory fault or bit 5 for an IO fault. In addition, the MIL-STD-1750A instruction is aborted and control passes to the level 1 interrupt service routine (if level 1 interrupts are unmasked). Time-outs are used to detect illegal IO operations or references to nonexistent memory locations. The time-out circuit may be disabled with Disable Time-Out (DTON) to allow transactions of longer duration to run to completion. However with the time-out circuitry disabled, the MAS281 CPU provides no protection against illegal transactions.

2.4 Direct Memory Access

During Direct Memory Access (DMA), the CPU enables the MMU and BPU for use by the DMA controller. Data transfers within expanded memory space, including address translation and protection, are accomplished through the DMA controller by providing the address state and processor state inputs AS and PS with the associated logical address.

DMA is supported by the MAS281. For a discussion of DMA control, refer to the MAS281 data sheet. The MMU, with its associated logic, supports the expanded memory systems, and the interface buffering for the data and address buses. The MMU also contains the memory fault status register.

MA17504

MIL-STD-1750A Memory Management Unit/ Block Protect Unit

3.0 Memory Management Unit

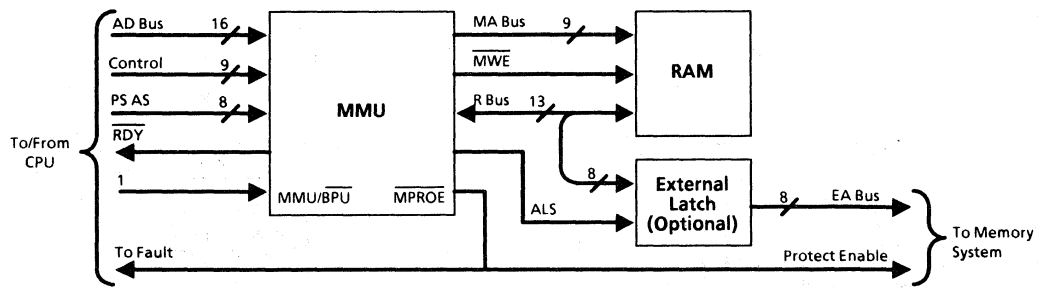


Figure 2. Memory Management Unit Configuration

3.1 Architecture

When used as an MMU (Figure 2) the chip requires 512 13-bit words of RAM to support the full complement of page registers. An external address latch may be used to latch the eight most significant bits of the expanded (20-bit) physical address, although the support RAMs for the MMU will provide that data for the remainder of the memory operation.

When configured for memory management, the MA17504 chip provides the following functions to support expanded memory systems:

3.1.1 Memory Space - Logical to physical address translation (20 bits of address) to permit access to 1,048,575 words of physical memory space.

3.1.2 Table Access - Look-up table access to 512 page registers of which 256 are instruction page registers and 256 are operand page registers.

3.1.3 Protection - Memory protection of 4K-word pages for both CPU and DMA references, which includes access protect, write protect, and execute protect.

The MMU uses a table look-up scheme to convert a logical memory address to a physical page address. An additional memory access delay is incurred in developing the expanded memory address. The added delay is a function of MMU logic and of the RAM memories used for the page registers.

3.2 Address Translation and Protection Mechanism

The MMU maps system memory into 4K-word pages. The mapping mechanism, shown in Figure 3, incorporates 512 page registers that are organized in 16 pairs of groups, one group for instruction memory space and one group for data memory space. Each group contains 16 page registers accommodating a total of 256 registers for data space and 256 registers for instruction space.

The memory address modification function can form any address to the page file. This function is implemented with the four-bit Address State (AS) and the Instruction/Operand (IN/OPN) discrete. The four AS bits select one of the 16 pairs of groups. The selection of the group within the pair is done by the IN/OPN. The page register within the group is selected by the four most significant bits of the address (AD00-AD03). The eight bits of the Physical Page Address (PPA) are then placed on the address lines to be used with the least significant 12 bits of the logical address to form the 20-bit physical memory address. The delay in developing the memory address is a function of the RAM memories used to hold the page registers.

The MMU also checks for protection violations by comparing the Processor State (PS) to the Access Lock (AL) field in the page register. Protection is also provided by examining the Write Protect bit (W in Operand page register) if data is to be written, or the Execute Protect bit (E in Instruction page register) if an instruction is to be read.

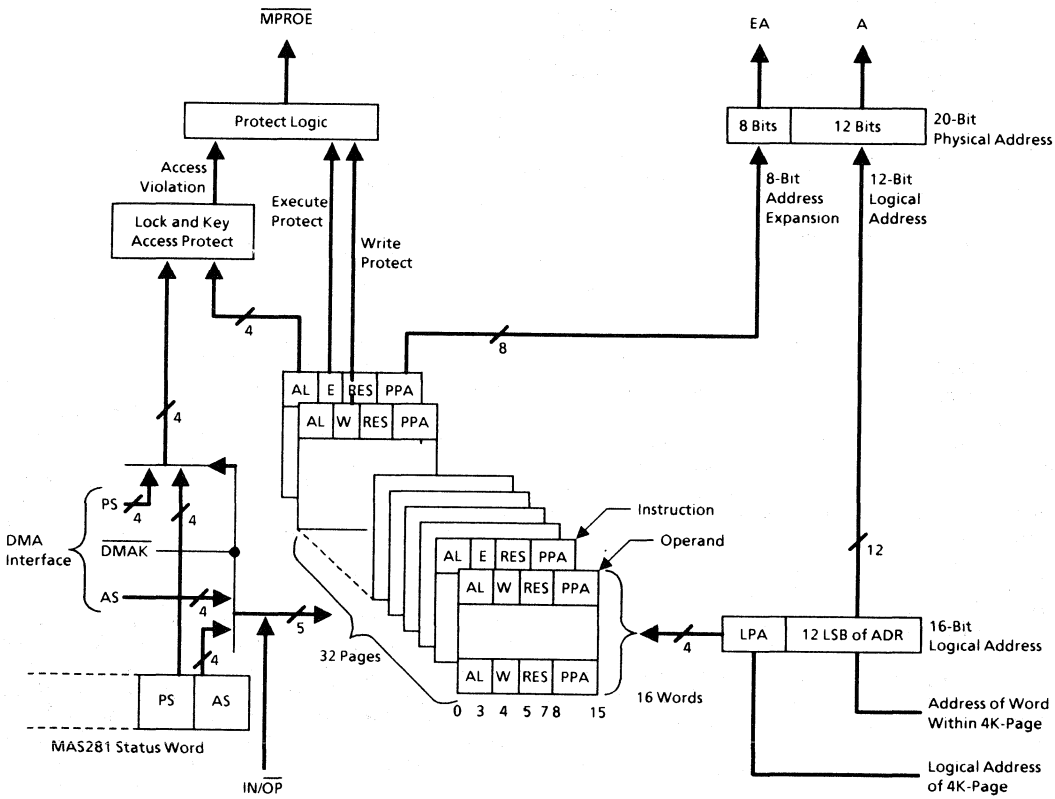


Figure 3. MMU Mapping Mechanism

AL Code	Acceptable Access Key Codes
0	0
1	0,1
2	0,2
3	0,3
4	0,4
5	0,5
6	0,6
7	0,7
8	0,8
9	0,9
A	0,A
B	0,B
C	0,C
D	0,D
E	0,E
F	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F

Table 2. Access Lock and Key Mapping

If a violation occurs, the memory protect output is asserted, the current instruction is aborted, and the Memory Fault Status Register (MFSR) is loaded. Table 2 illustrates the Access Key mapping mechanism.

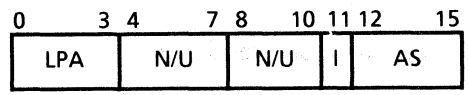
When memory transactions are controlled by the MAS281, the AS0-AS3 and PS0-PS3 bits necessary to perform the address translation and access protection functions, respectively, are obtained from a copy of the MAS281 status word AS and PS fields contained in the MMU(BPU). If a DMA controller is performing memory transactions, it must provide the proper AS0-AS3 and PS0-PS3 signal inputs to the MMU for address translation and access protection.

3.3 Memory Fault Status Register

The Memory Fault Status Register (MFSR) contains page register selection information captured when a memory fault occurs. Figure 4 defines the format of the MFSR. The register (physically located in the MMU) may be read by software through the IO command Read Memory Fault Status (RMFS) in order to interpret the page selection associated with the fault. When a memory access violation or write protect violation occurs, the MFSR will capture the appropriate page selection to identify to software the designators associated with the memory fault. The fault register status will identify the address of the page register, the page set selector (IN/OPN), and the address of the selected group.

3.4 Buses

A 16-bit multiplexed Address/Data (AD) bus provides a communications path between the MMU(BPU), the other components of the MAS281 chip set, and any other devices mapped into the address space of the chip set. During a typical addressed access, the 16-bit address is placed on the bus during AS high state while the 16-bit data word is presented during the low state of DSN. The AD bus, along with the necessary control signals, facilitates the asynchronous operation of memory and IO subsystems with the CPU.



Field	Bit	Description
LPA	0 - 3	Logical Page Address
N/U	4 - 7	Not Used (Always Zero)
N/U	8 - 10	Not Used (Always Zero)
I	11	Instruction/$\overline{\text{Operand}}$ Set
AS	12 - 15	Address of Group

Figure 4. Memory Fault Status Register Bit Assignments

Two RAM support buses provide the data and address links between the MMU(BPU) and its supporting RAMs. The MA bus provides addressing information to the support RAMs while the R bus supplies data information. In addition, bits R08 through R15 of the R bus provide the 8-bit expanded address information needed for creation of the full 20-bit physical address.

ALS(R05), MPEN(R06), and ILLADN(R07) are not considered part of the R bus when the chip is configured as an MMU and are explained in the following section.

4.0 MMU Signal Definitions

4.1 Pin Functions

All pin functions, with the exception of power and ground, are TTL compatible. In addition, each of these functions is provided with Electrostatic Discharge (ESD) protection. External buffering of output and normal ESD precautions are recommended.

A description of each pin function follows. The function name is presented first, followed by its acronym , its type, and its description. Function type is either input, output, high impedance (Hi-Z), or a combination thereof. Timing characteristics of each of the functions described is provided in Section 6.0.

4.1.1 Power and Ground (VDD & GND)

4.1.2 Address Strobe (AS) - Input. This active high input signal indicates that the Address/Data (AD) bus contains address information. The address information is assured stable at the high-to-low transition of this signal.

4.1.3 Data Strobe (DSN) - Input. This active low signal indicates that the Address/Data (AD) bus is being used for data transfers. The RD/WN function indicates the direction of transfer during DSN. The read state (RD) indicates input to the CPU or DMA device. The write state (WN) indicates output from the CPU or DMA device.

During read operations, data is placed on the data bus during the low state of DSN and must remain stable through the low-to-high transition of DSN. The low-to-high transition of DSN indicates the acceptance of the data by the CPU or DMA device.

During write operations, a low on the DSN input indicates that data is being input on the AD bus. The data will be assured stable at the low-to-high transition of the DSN input. Data sampling must occur just prior to, or coincident with, the low-to-high transition of DSN.

4.1.4 Read/Write (RD/WN) - Input. This input defines the direction of data flow on the address data flow on the address data bus (AD). A read operation by the CPU or DMA device is indicated by a high signal level. A write operation by the CPU or DMA device is indicated by a low signal level. The MMU uses this input to detect an execute protect fault or a write protect fault.

4.1.5 Memory/Input-Output (M/ION) - Input. This function defines the type of transaction currently utilizing the AD bus. A high level indicates a memory operation, and a low level indicates an input-output operation.

4.1.6 Instruction/Operand (IN/OPN) - Input. This function defines the type of operation on the AD bus during a memory access. A high on this input indicates an instruction access and a low indicates an operand access. The MMU requires this function for memory management to select between the group of 256 page registers for data space and the group of 256 page registers for instruction space.

4.1.7 Ready (RDYN) - Output. This function informs the CPU that the MMU(BPU) has completed the appropriate IO commands. RDYN is forced low by the MMU when DSN is active during an IO operation involving commands WIPR, WOPR, RMFS, RIPR, or ROPR. When more than one device in the system can drive the RDYN signal, the RDYN lines must be ANDed together externally and then sent to the MAS281. This will allow the appropriate device to drive RDYN low.

Signature	I/O	Definition
AD00-AD15	I/O	Bidirectional 16-Bit Address/Data Bus
AS	I	Address Strobe (Indicates Address is on AD Bus)
$\overline{BLPE}$	O	Block Protect Enable (Not used for MMU)
$\overline{DMAK}$	I	DMA Acknowledge (AD Bus to be used for DMA)
$\overline{DS}$	I	Data Strobe (Indicates Data is on AD Bus)
AS0-AS3	I	Address State Data (Provided by DMA Device)
PS0-PS3	I	Processor State Data (Provided by DMA Device)
IN/$\overline{OP}$	I	Instruction/Operand (Indicates Type of Memory Access)
MA0-MA8	O	Address Bus for Page RAMS
M/$\overline{IO}$	I	Memory/Input-Output (Indicates Type of AD Bus Transaction)
MMU/$\overline{BPU}$	I	MMU or BPU Selection (High for MMU)
$\overline{MPROE}$	O	Memory Protect Error (Indicates Access Errors)
$\overline{MWE}$	O	Memory Writes Enable (Write Strobe to Page RAMS)
RD/$\overline{W}$	I	Read/Write (Indicates Data Direction on AD Bus)
$\overline{RDY}$	O	Ready (Terminates MMU XIO Bus Cycle)
RESET	I	Reset (Triggers Device Initialisation)
R00-R04	I/O	5 Bits of Data Bus for Page RAMS
ALS	O	Address Latch Strobe (Optional Expanded Address Strobe)
$\overline{MPE}$	I	Memory Parity Error (Latches Data into MFSR)
$\overline{ILLAD}$	I	Illegal Address Error (Latches Data into MFSR)
R08-R15	I/O	8 Bits of Data Bus for Page RAMS (also Expanded Address Bits for Memory Management)
VDD	I	Power, + 5 Volts
VSS	I	Ground

Table 3. MMU Signal Definitions

4.1.8 Memory Write Enable (MWEN) - Output. This signal enables writing to support RAMs and is active coincident with DSN during WIPR and WOPR instructions.

4.1.8 Address/Data Bus (AD Bus) - Input/Output/Hi-Z. These signals comprise a bidirectional multiplexed address and data bus. This bus transfers address and data information among memory, the MAS281, and the MMU. AD00 is the most significant bit position and AD15 is the least significant bit position of both the 16-bit data and 16-bit address. A high on this bus corresponds to a logic '1' and a low corresponds to a logic '0'.

4.1.10 Memory Address Lines (MA Bus) - Output. These outputs serve as the 9 address lines to the support RAMs to allow up to 512 page registers to be accessed. During an IO operation, MA0-MA8 are controlled by AD15-AD7. During memory operations under MAS281 control, MA0-MA8 are controlled by AD3-AD0, AS (from the MAS281 status word copy), and IN/OPN respectively. During memory operations under a DMA device control, MA0-MA8 are controlled by AD3-AD0, EA3-EA0, and IN/OPN respectively. In this case, the DMA device must present the correct address state bits via the AS0-AS3 (AS0 is MSB) inputs and the access key to the MMU via the PS0-PS3 (PS0 is MSB) inputs.

4.1.11 Page RAM Data Lines (R00-R04 & R08-R15) - Input/Output/Hi-Z. These 13 bidirectional lines serve as the data bus for the MMU Page RAMs. The page register data is loaded (via WIPR and WOPR commands) and read (via RIPR and ROPR commands) across this bus. Page RAM output on R08-R15 (R08 is MSB) is used along with the 12 LSB of the logical address to form the 20-bit physical memory address. R00-R03 are the access lock bits of the page register and R04 is used as the execute protect or write protect bit (depending on which group of page registers is accessed).

4.1.12 Address Latch Strobe (ALS) - Output. This signal occurs coincident with the AS input. The Address Strobe is routed through the MMU and sent out on the ALS line.

4.1.13 Memory Protect Error (MPROEN) - Output. This active low output indicates when a memory protect error has occurred. MPROEN will never go low during an IO operation. During a memory operation, MPROEN is forced low when AS goes high, and MPROEN is forced back high when DSN goes low. An access fault, execute protect, or write protect error has occurred if MPROEN does not go back high when DSN drops low.

The MAS281 samples MPROEN after DSN goes low and before AS goes high. When a BPU and an MMU are both used in the same system with the same MAS281, the MPROEN signals from the BPU and MMU must be ANDed together externally and then sent to the MAS281. MPROEN is forced high whenever AS is low and RESET is high, or when DSN and M/ION are low.

As an output, this function may be used as a memory system inhibit for access faults, execute protect and write protect violations detected by the MMU.

4.1.14 Memory Parity Error (MPEN) - Input. This active low input signal indicating memory parity error from the CPU must be input to the MMU via MPEN. This must be done so the Memory Fault Status Register in the MMU can store the proper data when a memory parity error occurs.

4.1.15 Illegal Address (ILLADN) - Input. This active low input signal for illegal address error from the CPU must be input to the MMU via ILLADN. This must be done so the Memory Fault Register in the MMU can store the proper data when an illegal address error occurs.

4.1.16 Reset (RESET) - Input. A high on this input will set BLPEN to a high and when AS is low will set MPROEN to a high.

4.1.17 Block Protect Enable (BLPEN) - Output. This output signal is high whenever a RESET occurs and remains high when the chip is configured as an MMU. The MMU does not use this signal.

4.1.18 Memory Management/Block Protect Unit (MMU/BPUN) - Input. This input designates which mode the MMU/BPU is in. To be configured as an MMU, this signal must be pulled- up to VDD.

4.1.19 Direct Memory Access Acknowledge (DMAKN) - Input. A low on this input indicates that a DMA device is in control instead of the MAS281. This signal is also used by the MMU for access protection to select between processor state bits from the MAS281 status word copy or external processor state bits (PS0-PS3) from a DMA device.

4.1.20 External Address State Bits (AS0-AS3) - Input. In the MMU mode during a DMA operation, the controlling DMA device must input AS0-AS3 (AS0 is MSB) for the Address State bits to select the correct page register group.

4.1.21 External Processor State Bits (PS0-PS3) - Input. In the MMU mode during a DMA operation, the controlling DMA device must input the correct access key on PS0-PS3 (PS0 is MSB) for the Processor State bits.

5.0 Block Protection Unit

The BPU and the MMU have many operational similarities. Among them, which were discussed in the preceding MMU section, include: Buses, Power, Address Strobe, Data Strobe, Read/Write, Memory/Input- Output, Memory Write Enable, Address/Data Bus, and Reset.

5.1 Architecture

The BPU, with its associated logic, supports the block protection feature and the interface buffering for the data and address buses. Through external pin connections, this chip may be configured as a Block Protect Unit (BPU) to protect from 64K- to 1M-words of memory. When configured as a BPU for more than 64K-words of memory, additional memory chips are needed to contain the memory protect RAM. However, the chip does contain sufficient memory to provide memory protect RAM for up to 64K-words of memory. Figure 1 depicts the relationship between the MMU(BPU) components.

When used as a block protect controller, the MMU(BPU) can be used in one of two configurations. When configured as a block protect controller for systems with 64K-words of memory or less (Figure 5), the block protect function is self-contained and includes eight 16-bit write lockout registers.

When configured with an MMU in systems requiring more than 64K-words of memory (Figure 6), the block protect function requires additional RAM space (128-words of 16-bit RAM) to provide the full complement of write lockout bits.

When configured for memory protection, the MMU(BPU) chip provides the following features to support the use of memory subsystems:

Write Protection - In 1K-page blocks for up to 1M-words of CPU memory space.

Write Protection - In 1K-page blocks for up to 1M-words of DMA memory space.

Global Memory Protection - At initialisation until software initiates the MPEN XIO command.

3

A 128-word RAM provides a look-up table in which bits represent 1K-word pages of CPU and DMA memory space. RAM words 0 through 63 provide CPU write protect while words 64 through 127 provide DMA write protect. The most significant bit of the RAM word represents the lowest numbered block and the least significant bit represents the highest numbered block. Bit 0 of word 0 protects the 1K-block of locations 0 through 1023 while bit 15 of word 0 protects the 1K-block from location 15360 through 16383. A 1 in the bit position provides write lockout protection and a 0 permits writing to any word in the referenced 1K-block.

When a memory access is made, the six most significant bits of the address and the DMAKN signal will select the protect register. The next four bits of the address will select the proper bit of the register and, when ANDed with the MPROEN and RD/WN during a memory operation, will detect a memory protect error (unless DMPROEN is high).

During the start-up of the microprocessor, the reset signal will clear the block protect RAM and leave it in the disabled condition. A global protect enable provides write protection to all CPU/DMA memory space at initialisation to allow software to write the desired protection table to the block protect RAM. Three IO commands are decoded in the BPU mode: the Load Memory Protect (LMP) RAM command, the Read Memory Protect (RMP) RAM command, and the Memory Protect Enable (MPEN) command. The load or read commands will switch the address multiplexer to allow the IO command to address the RAM.

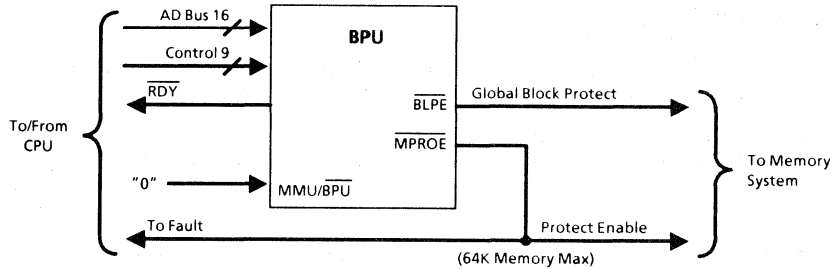


Figure 5. Normal Block Protect Unit Configuration

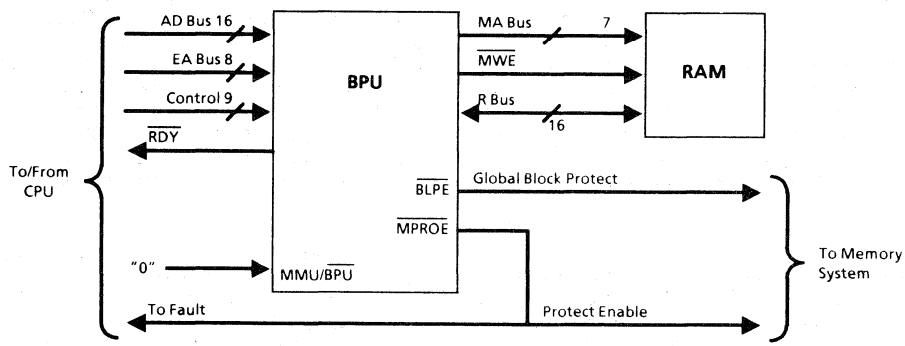


Figure 6. Block Protect Unit Configuration with MMU

5.2 Memory Fault Status Register

The memory fault status register contained in the MMU(BPU) is not used when configured as a BPU.

5.2.1 Instruction/Operand (IN/OPN) - Input. This input is not used by the MA17504 when it is configured as a BPU.

5.2.2 Ready (RDYN) - Output. This output function informs the MAS281 that the MMU(BPU) has completed the appropriate IO commands. RDYN is forced low by the BPU when DSN is active during an IO operation involving commands MPEN, LMP, or RMP. When more than one device in the system can drive the RDYN signal, the RDYN lines must be ANDed together externally and then sent to the MAS281. This will allow the appropriate device to drive RDYN low.

5.2.3 Memory Address Lines (MA Bus) - Output. These serve as the 7 address lines to the protection RAMs to allow one of up to 128 16-bit registers to be selected. Each bit of the 16-bit word selected will protect a 1K-page block of memory. Therefore, up to 1M-words of write protection in 1K-page blocks for CPU memory space and up to 1M-words of write protection in 1K-page blocks for DMA memory space is provided. The registers are loaded via the LMP command. The MPEN command must be executed to enable sensitive block protection. The RMP command inputs the appropriate memory protect word into register RA.

During an IO operation, MA0-MA6 are driven by AD15-AD9 respectively. During a memory operation, MA0-MA6 are driven by EA5-EA0, and DMAKN respectively.

5.2.4 Memory Address Lines (MA0,1 & 6) - Output. In the normal BPU mode (write protect for up to 64K-words in CPU memory space and up to 64K-words in DMA memory space), MA0, MA1, and MA6 are driven by EA5, EA4, and DMAKN respectively to address one of eight built-in 16-bit registers; four for DMA write protection; and four for CPU write protection.

MA6 always selects between the CPU or DMA memory space (if MA6 is high, DMA memory space protect registers are selected and if MA6 is low, CPU memory space protect registers are selected). MA0 and MA1 select one of the four 16-bit protect registers. In this mode, EA4 and EA5 are driven externally by AD00 and AD01 respectively and, because DMAKN drives MA6, they provide proper selection of one of the 8 built-in protect registers.

5.2.5 Memory Data Lines (R Bus) - Input/Output/Hi-Z. In the BPU configuration with more than 64K-word protection, these 16 lines serve as the data bus for the support RAMs. Each 16-bit data word serves as a block protect register for memory protection of 16K-word blocks. The block protect registers are loaded via the LMP command and are read via the RMP command. This data bus is not used in the normal BPU mode.

5.2.6 Expanded Address Lines (EA Bus) - Input. When the BPU is used in the expanded block protect mode (MMUN is high), the 8 most significant bits of the 20-bit physical address must be input into the BPU so block protection can be checked. EA0 is the MSB of these 8 bits.

5.2.7 Expanded Address Lines (EA4 & 5) - Input. When the BPU is used in the normal block protect mode (MMUN is low; up to 64K-block protection), AD00 and AD01 must be tied to EA4 and EA5 respectively so the correct built-in page register is selected to determine block protection.

5.2.8 Block Protection Enable (BLPEN) - Output. This active low signal signifies that selective block protection is implemented and global protection is no longer provided. With BLPEN high, global block protection is provided while write protection tables are sent to the block protect RAMs via software. This signal is high whenever a RESET occurs and remains high until the rising edge of DSN when the MPEN command is being executed. Therefore, this signal should be used to provide global block protection until an MPEN instruction occurs to allow selected block protection. With BLPEN high, no block protect error is indicated.

5.2.9 Memory Protect Error (MPROEN) - Output. This active low output indicates that a memory protect error has occurred. During a memory operation with DMPROE low, MPROEN is forced low when AS goes high, and MPROEN is forced back high when DSN goes low. A block protect error has occurred if MPROEN does not go back high when DSN drops low. The MAS281 samples MPROEN after DSN goes low and before AS goes high.

When a BPU and a MMU are both used in the same system with the same MAS281, the MPROEN signals from the BPU and MMU must be ANDed together externally and then sent to the MAS281. MPROEN is forced high whenever AS is low and RESET is high. MPROEN will never go low after RESET during a memory operation when DMPROE is high or during an IO operation. MPROEN will always go back high when DSN goes low if BLPEN is high (i.e., no memory protect error can occur during global block protection).

As an output, this function may be used as a memory system inhibit for write violations to protected blocks detected by the BPU.

5.2.10 Memory Management Unit/Block Protect Unit (MMU/BPUN) - Input. This input must be tied low when the MMU(BPU) chip is to be configured as a BPU.

5.2.11 Disable Memory Protect Error (DMPROE) - Input. This input must be driven high or low. If DMPROE is driven high, no memory protect error appears so MPROEN remains high. If DMPROE is driven low, MPROEN is allowed to drop low and remain low for the remainder of the cycle if an error occurs.

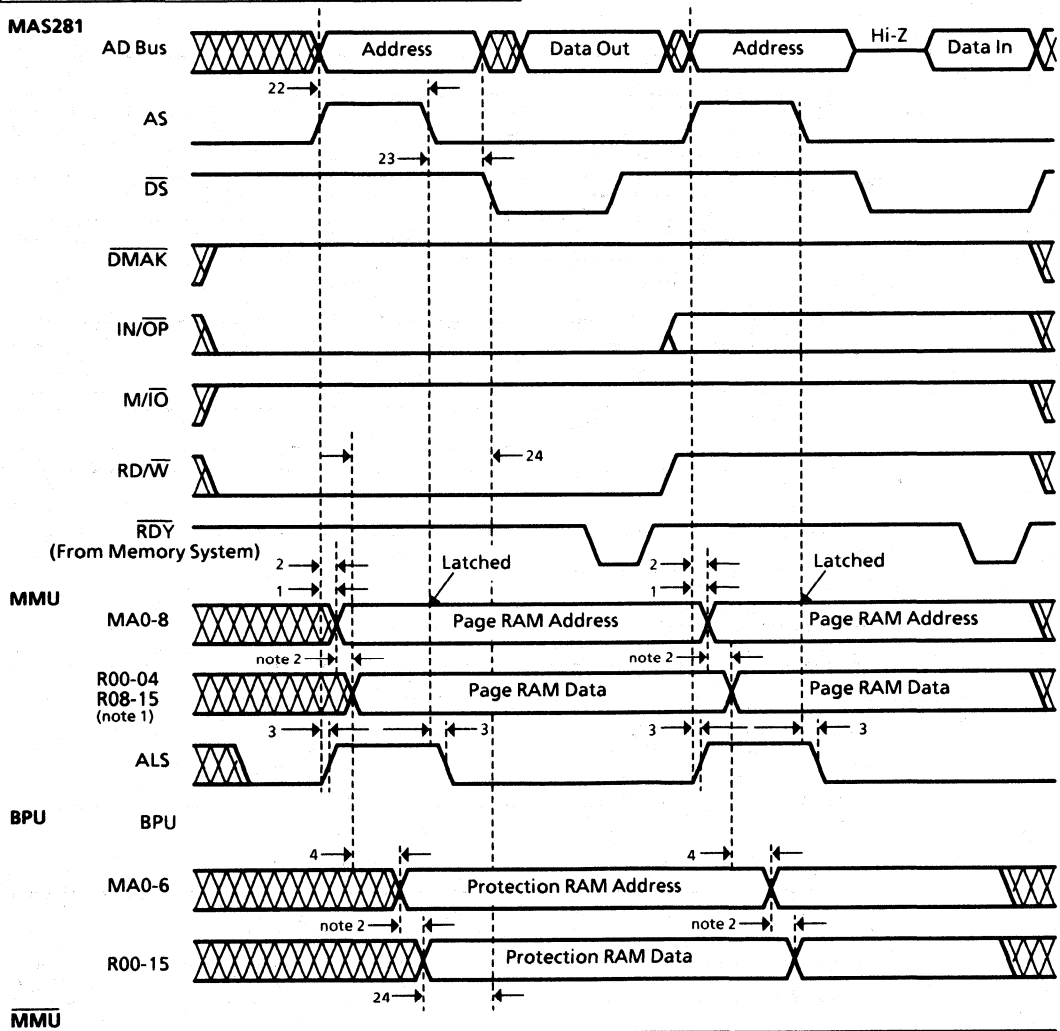
5.2.12 Memory Management Unit (MMUN) - Input. The MMUN input allows the user to select between use of an on-chip look-up table RAM or an off-chip table RAM, with MMUN high selecting the on-chip table. The on-chip look-up table is 8-words by 16-bits per word, provides write protection for up to 64K-words of memory space, 64K- words in DMA space, and should be used when no MMU is present in the system. The off-chip look-up table may be up to 128-words by 16-bits per word and must be used if write protection of greater than 64K-words (memory and DMA) is desired. The latter case also requires the use of an MMU to provide the necessary memory access.

5.2.13 Direct Memory Access Acknowledge (DMAKN) - Input. A low on this input indicates that a DMA device is in control instead of the MAS281. DMAKN is also used during IO operations to distinguish between CPU and DMA memory space write protection. It is routed through the MMU(BPU), where it is inverted, and sent out as MA6.

Signature	I/O	Definition
AD00-AD15	I/O	External 16-Bit Address/Data Bus
AS	I	Address Strobe (Indicates Address is on AD Bus)
$\overline{\text{BLPE}}$	O	Block Protect Enable (Global Protection)
$\overline{\text{DMAK}}$	I	DMA Acknowledge (AD Bus to be used for DMA)
$\overline{\text{DS}}$	I	Data Strobe (Indicates Data is on AD Bus)
EA0-EA7	I	Expanded Address Bus
IN/$\overline{\text{OP}}$	I	Instruction/Operand (Indicates Type of Memory Access)
MA0-MA6	O	Address Bus for Protector RAMS
DMPROE	I	Disables Block Protect Error Indication
$\overline{\text{MMU}}$	I	BPU Configuration Control (Normal or Expanded Mode)
M/$\overline{\text{IO}}$	I	Memory/Input-Output (Indicates Type of AD Bus Transaction)
MMU/$\overline{\text{BPU}}$	I	MMU or BPU Selection (Low for BPU)
$\overline{\text{MPROE}}$	O	Memory Protect Error (Indicates Block Protection Errors)
$\overline{\text{MWE}}$	O	Memory Write Enable (Write Strobe to Protection RAMS)
RD/$\overline{\text{W}}$	I	Read/Write (Indicates Data Direction on AD Bus)
$\overline{\text{RDY}}$	O	Ready (Terminates BPU XIO Bus Cycle)
RESET	I	Reset (Triggers Device Initialisation)
R00-R15	I/O	Data Bus for Protection RAMS
VDD	I	Power, + 5 Volts
GND	I	Ground

Table 4. BPU Signal Definitions

6.0 Timing Characteristics

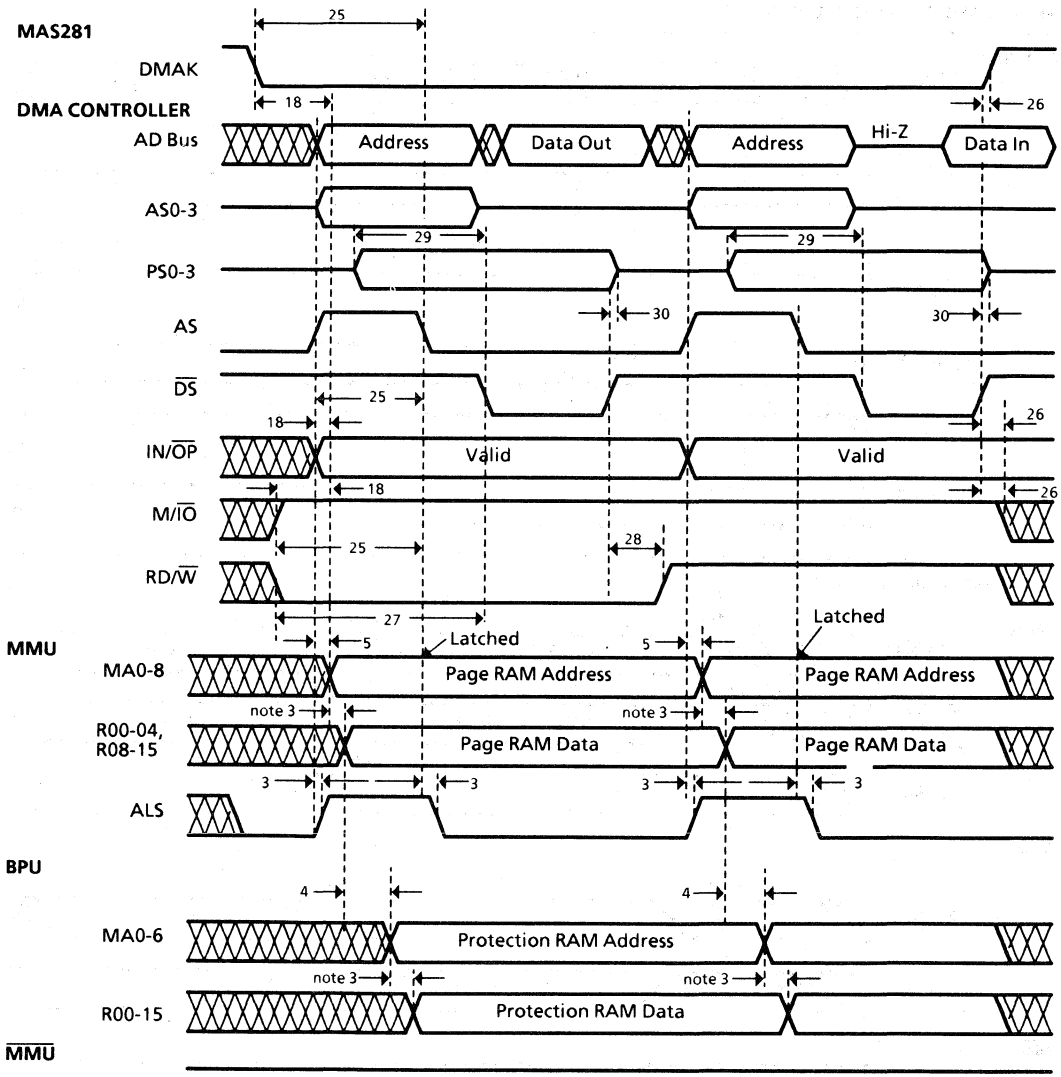


Notes

1 The MMU Page RAM R Bus supplies 8 expanded address bits. These 8 address bits are sent to the BPU (when a BPU is used with a MMU) via the EA Bus. The BPU creates the protection RAM Address bus MA0-MA6 by concatenating the DMAKN input of EA0-EA5 respectively.

2 Support RAM access time.

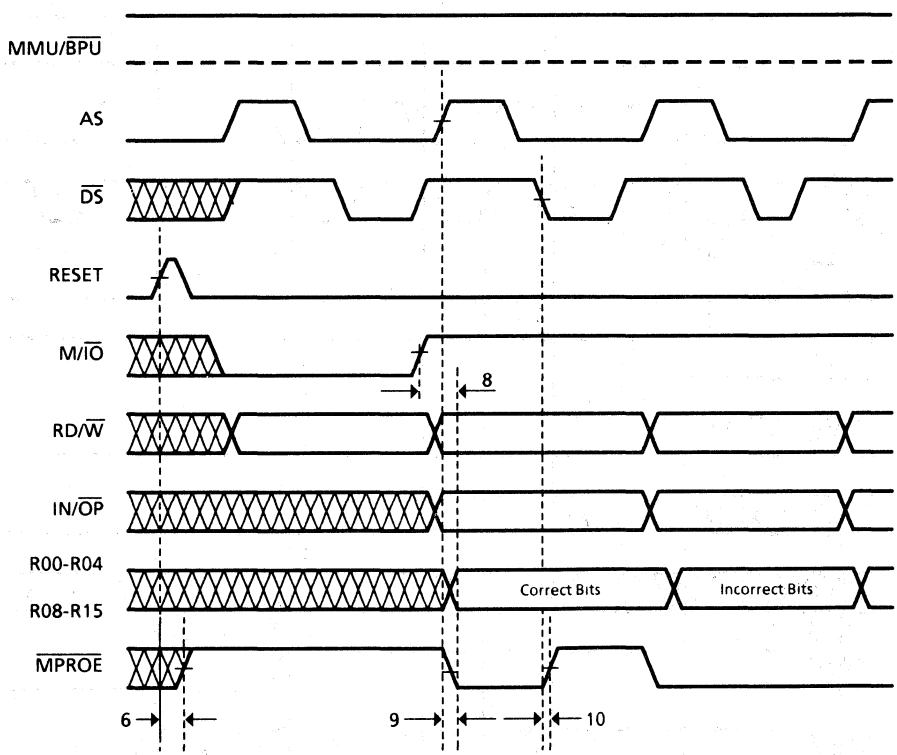
Figure 7. Expanded Memory with Block Protection Transaction Timing



Notes

1 The MMU Page RAM R Bus supplies 8 expanded address bits These 8 address bits are sent to the BPU (when a BPU is used with a MMU) via the EA Bus. The BPU creates the protection RAM Address bus MA0-MA6 by concatenating the DMAKN input of EA0-EA5 respectively.
2 DMA controller and memories must be selected to meet MMU/BPU timing requirements shown above.
3 Support RAM access time.

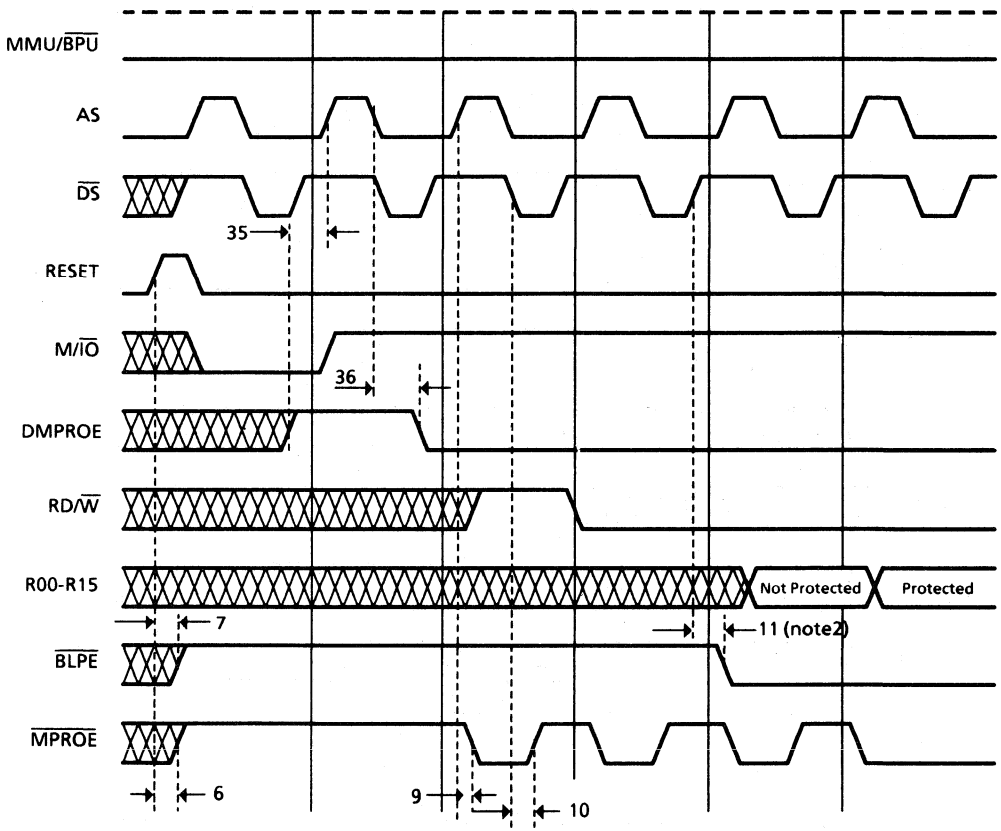
Figure 8. DMA Expanded Memory with Block Protection Transaction Timing



Notes

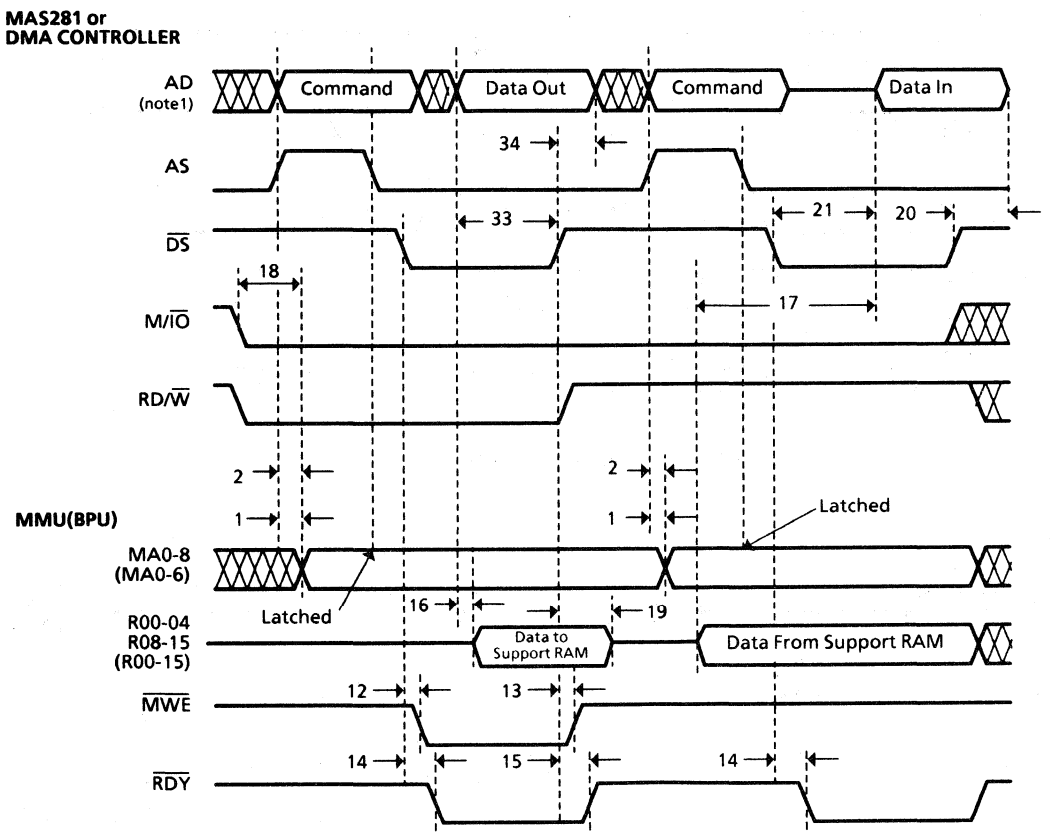
1 Definition of incorrect bits on the R bus is when the AL bits (R00-R03) do not match the processor state bits (from the status word or supplied by DMA) or when the E, W bit (R08) is high at the wrong time.
2 A memory protect error has occurred when MPROEN doesn't go high within propagation delay 10 of DSN.
3 MPROEN is reset high during RESET = 1 or when DSN = 0 and M/ION = 0.

Figure 9. MMU Memory Protect Error Generation



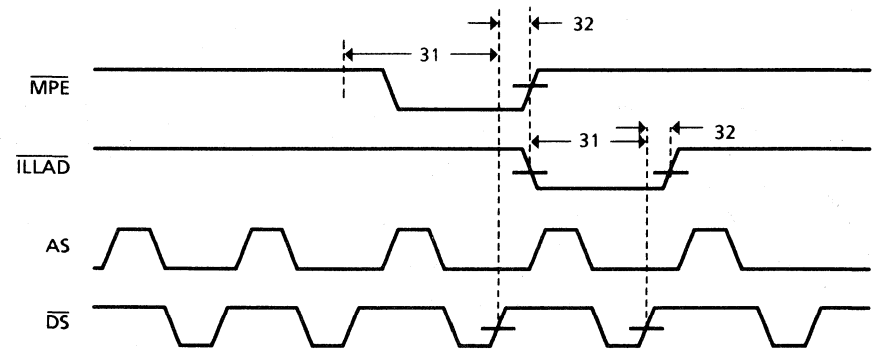
Note
1 A memory protect error has occurred if MPROEN doesn't go high within t of DSN ↓
2 The transition occurs during execution of the MPEN XIO command.

Figure 10. BPU Memory Protect Error Generation



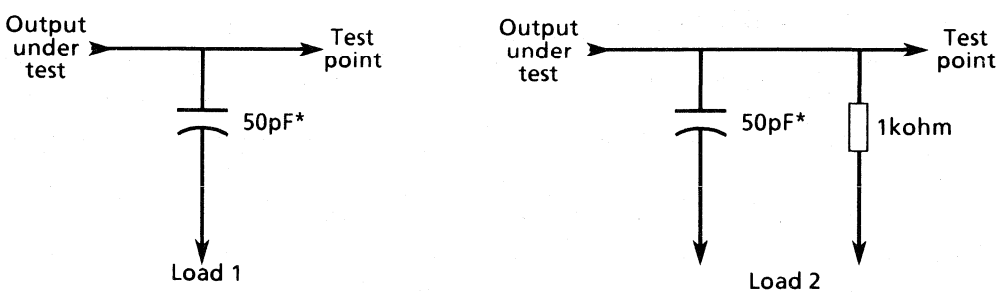
Note
1 Data direction with reference to the MAS281.

Figure 11. IO Transition Timing



Notes
1 Data is latched into the memory fault status register immediately after DSN ↑ when a memory protect error, a memory parity error, or an illegal address has occurred.

Figure 12. Memory Fault Status Register Loading



*Includes all jig and parasitic capacitance

Figure 13. Test Loads (see table 5)

No	Parameter (note 3)	Test Load (notes 1 & 2)	Min.	Max	Units
1	AS ↑ to MA[0-8]	1	-	65	ns
2	Address to MA[0-8]	1	-	55	ns
3	AS to ALS (MMU)	1	-	75	ns
4	EA [0-5] (BPU) to MA[0-6] (BPU)	1	-	50	ns
5	AS[0-3] to MA[0-8] (MMU)	1	-	60	ns
6	RESET ↑ to MPROEN ↑	1	-	60	ns
7	RESET ↑ to BPLEN ↓	1	-	35	ns
8	M/ION ↑ to MPROEN ↓	1	-	40	ns
9	AS ↑ to MPROEN ↓	1	-	40	ns
10	DSN ↓ to MPROEN ↑	1	-	50	ns
11	DSN ↑ to BPLEN ↓	1	-	35	ns
12	DSN ↓ to MWEN ↓	1	-	45	ns
13	DSN ↑ to MWEN ↑	1	-	40	ns
14	DSN ↓ to RDYN ↓	1	-	30	ns
15	DSN ↑ to RDYN ↑	1	10	35	ns
16	Data to R[0-4, 8-15] (MMU), R[0-15] (BPU) (I/O Write)	1	-	60	ns
17	R[0-4, 8-15] (MMU), R[0-15] (BPU) to Data (I/O Read)	1	-	65	ns
18	M/ION, IN/OPN, DMAKN to MA[0-8]	1	-	65	ns
19	DSN ↑ to R[0-4, 8-15] (MMU), R[0-15] (BPU) Hi-Z (I/O Write) (note 4)	2	-	35	ns
20	DSN ↑ to AD Bus Hi-Z (I/O Read) (note 4)	2	-	25	ns
21	DSN ↓ to AD Bus Active (I/O Read)	1	10	-	ns
22	Address Setup to AS ↓	-	10	-	ns
23	Address Hold after AS ↓	-	10	-	ns
24	R[0-4, 8-15] (MMU), R[0-15] (BPU) Setup to DSN ↓	-	30	-	ns
25	M/ION, IN/OPN, DMAKN Setup to AS ↓	-	5	-	ns
26	M/ION, IN/OPN, DMAKN Hold after DSN ↑	-	0	-	ns
27	RD/WN Setup to DSN ↓	-	5	-	ns
28	RD/WN Hold after DSN ↑	-	0	-	ns
29	PS[0-3] (MMU) Setup to DSN ↓	-	5	-	ns
30	PS[0-3] (MMU) Hold after DSN ↑	-	0	-	ns
31	MPEN, ILLADN (MMU) Setup to DSN ↑	-	10	-	ns
32	MPEN, ILLADN (MMU) Hold after DSN ↑	-	25	-	ns
33	Data Setup to DSN ↑ (I/O Write)	-	35	-	ns
34	Data Hold after DSN ↑ (I/O Write)	-	10	-	ns
35	DMPROE (BPU) Setup to AS ↑	-	0	-	ns
36	DMPROE (BPU) Hold after AS ↓	-	35	-	ns

Notes:
1. Unless otherwise noted: $V_{IL} \geq 0.0V$, $V_{IH} \leq 4.0V$, timing measured from 50% to 50% points.
2. -55°C, + 25°C, and + 125°C tested at $V_{DD} = 4.5V$ and 5.5V.
3. '(MMU)' indicates MMU configuration (MMU/BPUN high), '(BPU)' indicates BPU configuration (MMU/BPUN LOW). The parameter is valid for both configurations unless otherwise indicated.
4. High impedance measured by 20% (of VDD) voltage change using 1kohm pulldown resistor.

Table 5. MMU (BPU) Timing Characteristics

6.0 Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply voltage	-0.5	7	V
Input voltage	-0.3	V_{DD} + 0.3	V
Current through any pin	-20	20	mA
Operating temperature	-55	125	°C
Storage temperature	-65	150	°C

Table 6. Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.0 DC Electrical Characteristics

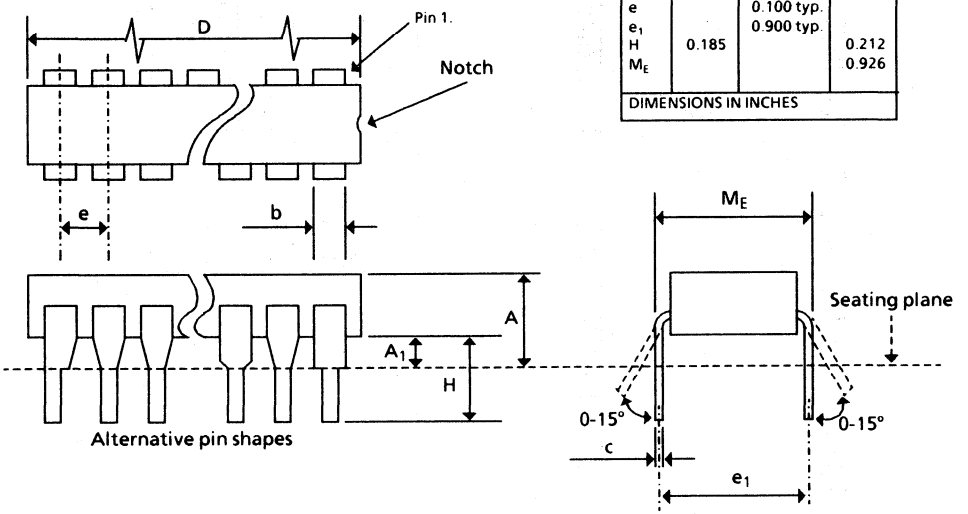
Symbol	Parameter	Condition	Total Dose Radiation Not Exceeding $3x10^5$ RAD (Si)			Units
			Min.	Typ.	Max.	
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	TTL Input High Voltage	-	2.0	-	-	V
V_{IL}	TTL Input Low Voltage	-	-	-	0.8	V
V_{OH}	TTL Output High Voltage	V_{DD} = 4.5V I_{OH} = -1.4mA	3.5	-	-	V
V_{OL}	TTL Output low Voltage	V_{DD} = 5.5V I_{OL} = 2.0mA	-	-	0.4	V
I_I	Input Leakage Current	V_{DD} = 5.5V V_{IN} = 0V or 5.5V	-	-	± 10	uA
I_{OZ}	Output Leakage Current	V_{DD} = 5.5V V_O = 0V or 5.5V	-	-	± 50	uA
I_{DDOP}	Operating Power Supply Current	V_{DD} = 5.5V AS = DSN = 10MHz	-	10	14	mA
I_{DDST}	Static Power Supply Current	V_{DD} = 5.5V	-	5	10	mA

V_{DD} = 5V ± 10%, over full operating temperature range.

Table 7. Operating DC Electrical Characteristics

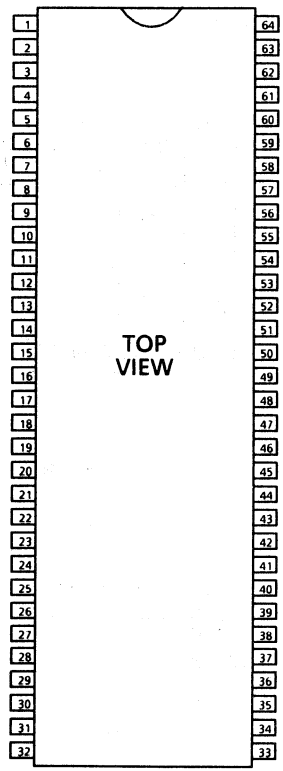
8.0 Packaging Information

Ceramic Dual-in-line (Package type C)



Ref.	Min.	Nom.	Max.
A			0.220
A_1	0.015		0.060
b	0.014		0.023
c	0.008		0.014
D			3.232
e		0.100 typ.	
e_1		0.900 typ.	
H	0.185		0.212
M_E			0.926
DIMENSIONS IN INCHES			

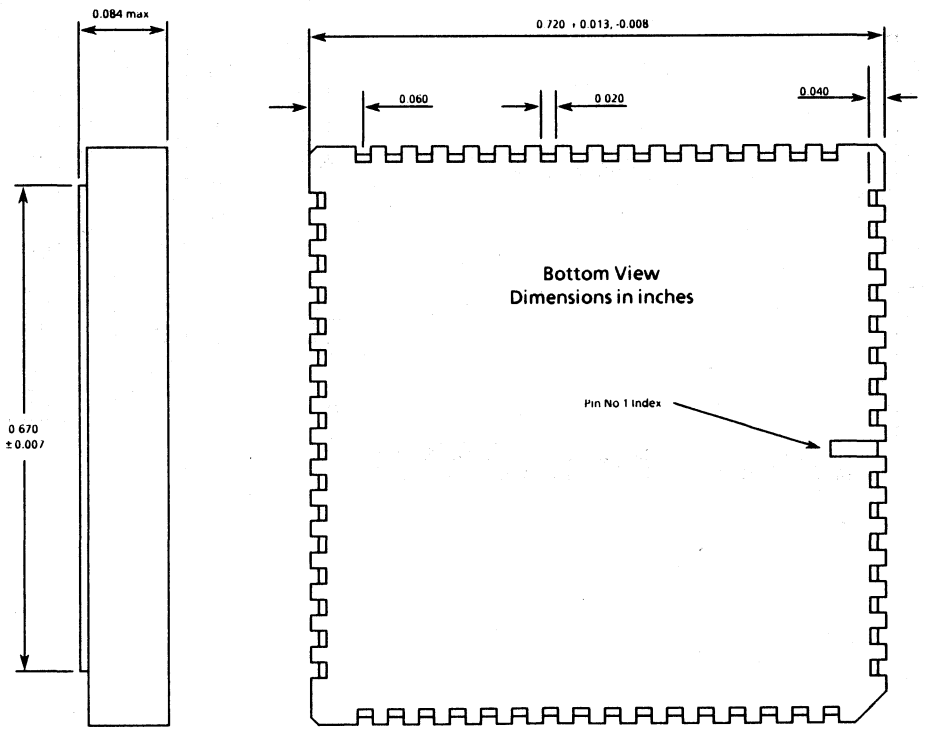
Figures 14a. Dimensioned Drawing



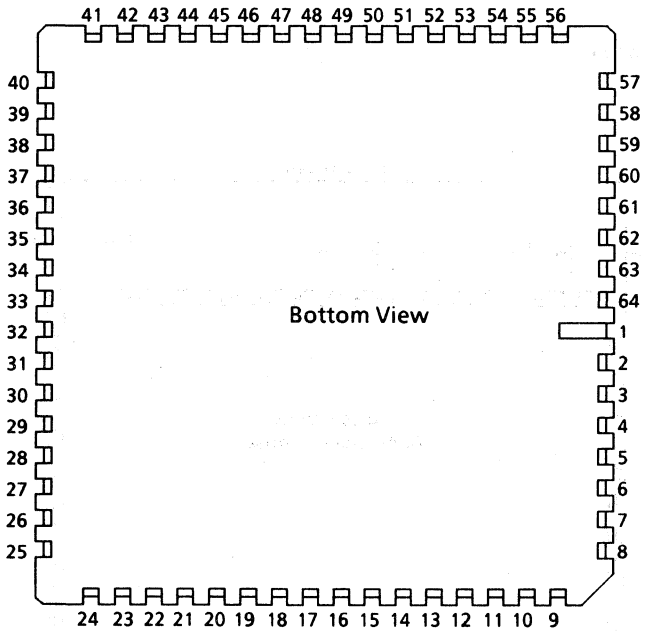
1	AD07	33	GND
2	AD06	34	RDYN
3	AD05	35	RESET
4	AD04	36	MMU/BPUN
5	AD03	37	M/ION
6	AD02	38	DSN
7	AD01	39	AS
8	AD00	40	R15
9	MA8	41	R14
10	MA7	42	R13
11	MA6	43	R12
12	MA5	44	R11
13	MA4	45	R10
14	MA3	46	R09
15	MA2	47	R08
16	NC	48	VDD
17	MA1	49	ILLADN
18	MA0	50	MPEN
19	AS0	51	ALS
20	AS1	52	R04
21	AS2	53	R03
22	AS3	54	R02
23	PS0	55	R01
24	PS1	56	R00
25	PS2	57	AD15
26	PS3	58	AD14
27	BLPEN	59	AD13
28	MPROEN	60	AD12
29	RD/WN	61	AD11
30	IN/OPN	62	AD10
31	MWEN	63	AD09
32	DMAKN	64	AD08

Figures 14b. Pin Assignments

Leadless Chip Carrier (Package type L)



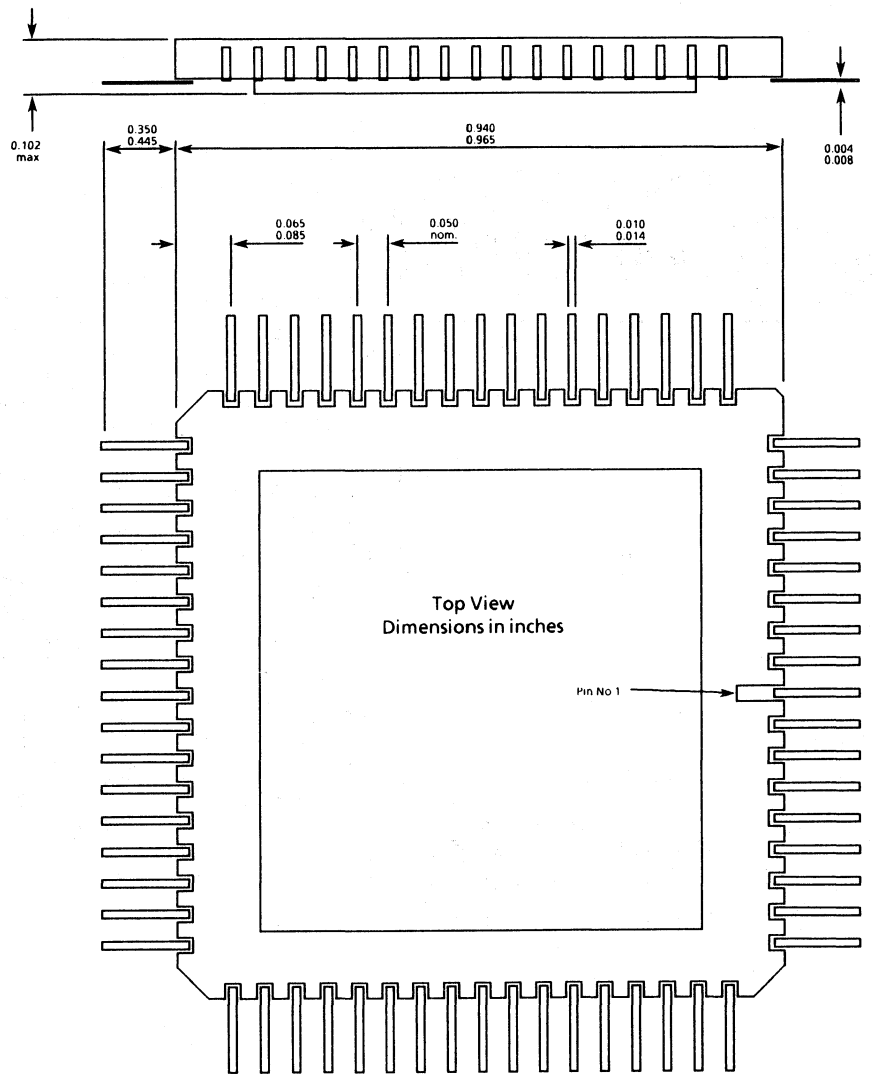
Figures 15a. Dimensioned Drawing



1	AD07	33	GND
2	AD06	34	RDYN
3	AD05	35	RESET
4	AD04	36	MMU/BPUN
5	AD03	37	M/ION
6	AD02	38	DSN
7	AD01	39	AS
8	AD00	40	R15
9	MA8	41	R14
10	MA7	42	R13
11	MA6	43	R12
12	MA5	44	R11
13	MA4	45	R10
14	MA3	46	R09
15	MA2	47	R08
16	NC	48	VDD
17	MA1	49	ILLADN
18	MA0	50	MPEN
19	AS0	51	ALS
20	AS1	52	R04
21	AS2	53	R03
22	AS3	54	R02
23	PS0	55	R01
24	PS1	56	R00
25	PS2	57	AD15
26	PS3	58	AD14
27	BLPEN	59	AD13
28	MPROEN	60	AD12
29	RD/WN	61	AD11
30	IN/OPN	62	AD10
31	MWEN	63	AD09
32	DMAKN	64	AD08

Figures 15b. Pin Assignments

Topbraze Flatpack (Package type - F)



Figures 16a. Dimensioned Drawing

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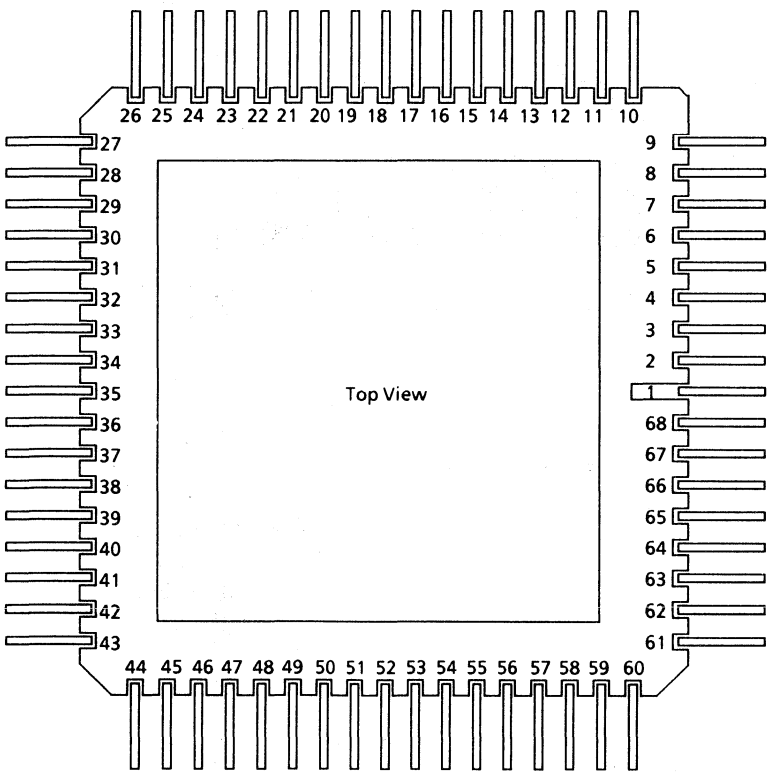

1	AD07	35	GND
2	AD06	36	RDYN
3	AD05	37	RESET
4	AD04	38	MMU/BPUN
5	AD03	39	M/ION
6	AD02	40	DSN
7	AD01	41	AS
8	AD00	42	R15
9	NC	43	NC
10	MA8	44	R14
11	MA7	45	R13
12	MA6	46	R12
13	MA5	47	R11
14	MA4	48	R10
15	MA3	49	R09
16	MA2	50	R08
17	NC	51	VDD
18	MA1	52	ILLADN
19	MA0	53	MPEN
20	AS0	54	ALS
21	AS1	55	R04
22	AS2	56	R03
23	AS3	57	R02
24	PS0	58	R01
25	PS1	59	R00
26	NC	60	NC
27	PS2	61	AD15
28	PS3	62	AD14
29	BLPEN	63	AD13
30	MPROEN	64	AD12
31	RD/WN	65	AD11
32	IN/OPN	66	AD10
33	MWEN	67	AD09
34	DMAKN	68	AD08

Figures 16b. Pin Assignments

9.0 Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

Total Dose (Function to specification, note 1)	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$3x10^{10}$ Rad(Si)/s
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/s
Neutron Hardness (Function to specification)	$1x10^{15}$ neutrons/cm2
Latch-up	Not possible
Single Event Upset (note 2)	$<10^{-10}$ errors/bit day

Note 1. Typical performance only, for guaranteed levels see ordering information.
2. GSO 10% Worst Case

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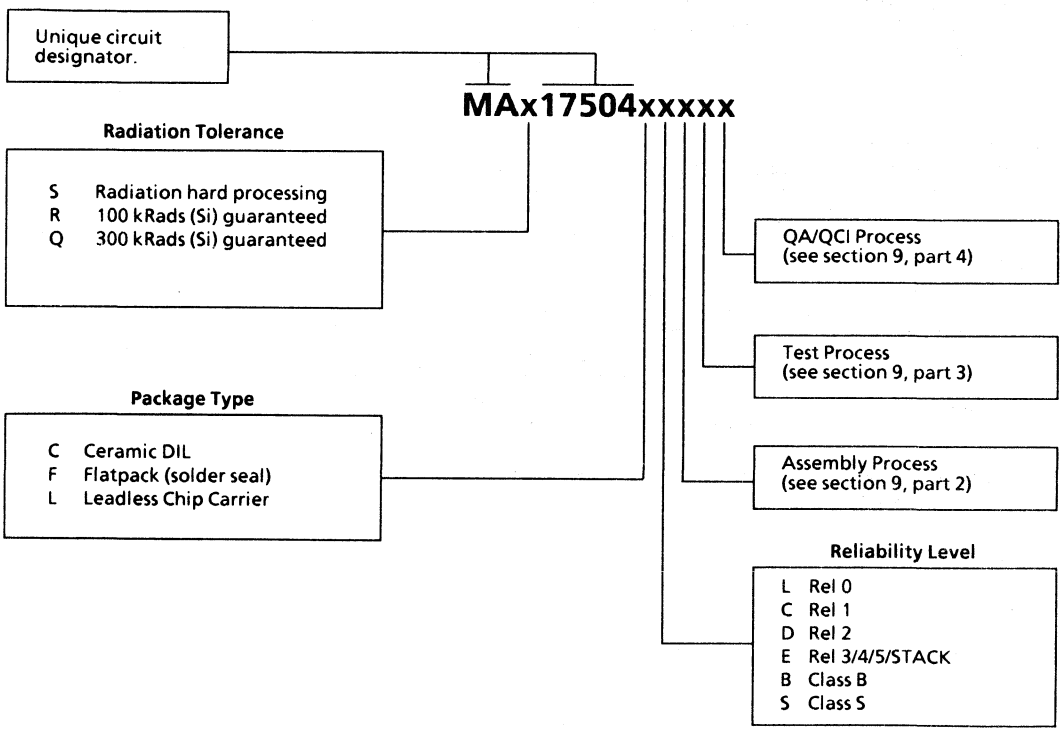
10.0 Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



GEC PLESSEY

SEMICONDUCTORS

S10203FDS Issue 2.4 October 1990

MA28137

Radiation Hard Programmable DMA Controller

Features

- **Radiation hard to 1 MRad (Si)**
- **High SEU immunity, latch-up free**
- **CMOS Silicon-on-Sapphire Technology**
- **MAS281 MIL-STD-1750A compatible**
- **Four independent DMA channels**
- **Independent autoinitialisation of all channels**
- **Enable/Disable control of individual DMA requests**
- **Memory-to-memory, I/0-to-memory and memory-to-I/0**
- **Memory block initialisation**

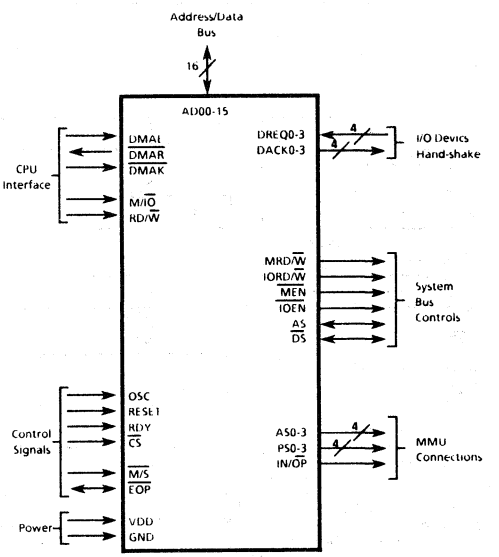


Figure 1: DMA Controller Connections

1 General Description

The MA28137 Direct Memory Access (DMA) controller is a peripheral interface circuit designed for MAS281 based microprocessor systems. It enhances system performance by allowing two way data transfer between external devices and the system memory, and between two memories. The MA28137 offers a wide variety of programmable control features to enhance system optimisation and to allow dynamic reconfiguration under program control.

The four independent channels may be expanded by cascading additional controller chips. Each channel can be individually programmed to autoinitialise to its original condition following an End of Process (EOP).

Three basic transfer modes are offered; read, write and verify.

A Memory Management Unit (MMU) can be used in conjunction with the MA28137 to extend addressing capability to 1M word.

2 Block Diagram

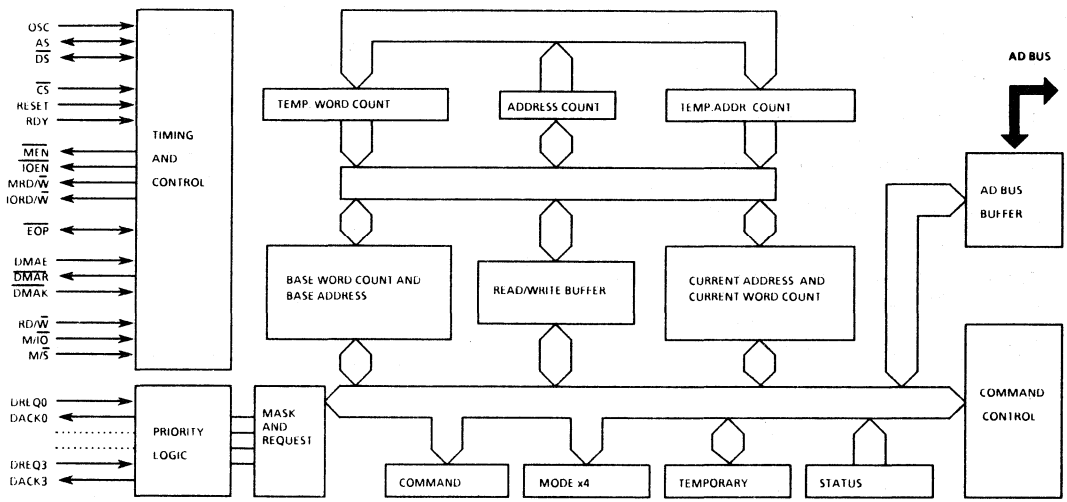


Figure 2: DMA Controller Principal Functional Blocks

3 Functional Description

The MA28137 provides four independent DMA channels, configurable under software control. Further DMA channels can be added by cascading two or more DMA controllers (see 4.2.4). Separate memory and I/O control signals are provided to allow direct I/O to memory and memory to I/O transfers. For memory to memory transfers, data passes through a 16-bit temporary register. Each channel has an associated MMU status register. Data held in these registers is output during DMA transfers to provide address status, instruction or operand status, and process status information to the memory management unit.

The major functional blocks and the principlal data paths of the DMA controller are shown in figure 2. The device contains three important blocks of control logic; the timing control block which generates internal timing and external control signals, the priority encoder block which resolves priority contention between DMA channels requesting service simultaneously, and the program command control block which decodes commands given to the MA28137 by the microprocessor and, while servicing a DMA request, decodes mode control words . The function and CPU access to each register in the set, is detailed in section 5.

4 DMA Operation

The MA28137 has two cycles of operation called the idle and active cycles. Each cycle comprises a number of states, each of which is one full OSC/2 internal clock period in length. For more detail see section 7.

When there is no DMA request pending the MA28137 enters the idle cycle. Although in the idle cycle, and thus inactive, the DMA controller may still be programmed by the processor. The control signals MENN, IOENN, MRD/WN and IORD/WN are generated by decoding the signals M/ION and RD/WN received from the MAS281. Whilst in the idle cycle the DMA controller repeats Si states until it enters the active cycle and the S0 state.

The MA28137 issues a DMA request to the processor and waits for a DMA acknowledge to be returned. When the acknowledge is received, the DMA transfer begins, however, until the acknowledge is received, the MA28137 remains programmable, and the M/ION and RD/WN signals continue to be decoded.

States S1, S2, S3 and S4 are the normal working states of a DMA transfer. If more time is needed to complete a transfer, wait states can be inserted by the MA28137 ready signal, between states S3 and S4.

During movements of data from memory to memory, each transfer word is temporarily stored in the DMA controller's temporary register. States S1, S2, S3 and S4 read the data word into the temporary register and and then transfer it from the temporary register to its new location. During the transfer all necessary bus control signals are driven by the DMA controller. For more detail see section 5.

When transferring data between memory and I/O, the temporary register is not used and data is passed directly from the source to the destination. The DMA controller passes through states S1, S2, S3 and S4 to complete a transfer (see figure 5).

4.1 Idle Cycle

When none of the channels are requesting service, the MA28137 will enter the idle cycle and perform Si states. In this cycle the MA28137 will sample the DREQ lines every clock cycle, to determine if any of the channels are requesting a DMA service. The device will also sample CSN, looking for an attempt by the microprocessor to write or read the MA28137's internal registers. When CSN is low and DMAK is high, the MA28137 enters the program condition and the CPU can establish, change, or inspect the internal definition of the device by reading from, or writing to, the internal registers. The four low-order address/data lines AD15-AD12, select which register is to be accessed. The RD/WN and DSN lines are used to select and time reads or writes.

There are two special software commands which can be executed by the MA28137 when in the program condition. These commands are decoded as sets of address with CSN and RD/WN. The commands Master Clear and Clear Mask do not make use of the data bus.

4.2 Active Cycle

When the MA28137 is in the idle cycle and a non-masked channel requests a DMA service, the device will output a DMAR to the microprocessor and enter the active cycle. In this cycle a DMA service will take place, in one of the four modes below.

4.2.1 Single Transfer Mode

In single transfer mode the device is programmed to make one transfer only. The word count will be decremented, and the address decremented or incremented following each transfer. The channel can be programmed to enable a Terminal Count (TC) to cause an autoinitialise when the word count 'rolls over' from zero to $FFFF_H$.

DREQ will not be recognised if it is allowed to go inactive before DACK becomes active. If DREQ is held active throughout the single transfer, DMARN will go inactive and release the bus to the system. Upon receipt of a new DMAK after the single tarnsfer, DMARN will once again go active, allowing another transfer to take place.

4.2.2 Block Transfer Mode

In block transfer mode the device is instructed by DREQ to continue making transfers during the service until a terminal count, caused by the word count going to $FFFF_H$, or an external end of process is encountered. DREQ need only be held active until DACK becomes active. Again, if the channel has been programmed, an autoinitialisation will occur at the end of the service.

4.2.3 Demand Transfer Mode

In demand transfer mode the device is programmed to continue making transfers until a terminal count or external EOP is encountered or until DREQ goes inactive. Thus transfers may continue until the I/O device has exhausted its data capacity.

After the I/O device has had a chance to catch up, the DMA service is re-established by means of a DREQ. During the time between services when the microprocessor is allowed to operate, the intermediate values of address and word count are stored in the MA28137 current address and current word count registers. Only an EOP can cause an autoinitialise at the end of the service: EOP is generated either by TC or by an external signal.

4.2.4 Cascade Mode

This mode is used to cascade more than one MA28137 together for simple system expansion. The DMAR and DMAK signals from the additional controller are connected to the DREQ and DACK signals of a channel on the initial MA28137. This allows the DMA requests of the additional device to propagate through the priority network circuitry of the processing device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests.

In a system with only one DMA controller, the controller generates the system control signals MENN, IOENN, MRD/WN and IORD/WN from the incoming signals M/ION and RD/WN during periods when DMAKN is high (i.e. no transfers occurring). This allows the same control signals to be used during both DMA and non-DMA modes.

In a multi-level DMA system during non-DMA periods only one controller must generate the four system control lines, to prevent contention. The master/slave (M/SN) pin enables (master) or disables (slave). The generation of these control lines during non-DMA mode and allows one level 1 controller to be designated a master (with all other controllers as slaves).

The cascade channel of the master MA28137 is used only to prioritise the slave device, it does not produce any address or control signals of its own. These could conflict with the address and control signals of the slave device. The master MA28137 will respond to DREQ and DACK but all other outputs except DMARN will be disabled.

Figure 3 shows two slave devices cascaded into the master device using two of its channels. This forms a two level DMA system. More MA28137s could be added at the second level by using the remaining channels of the first level. Additional devices can also be added by cascading into the channels of the second level devices, forming a third level.

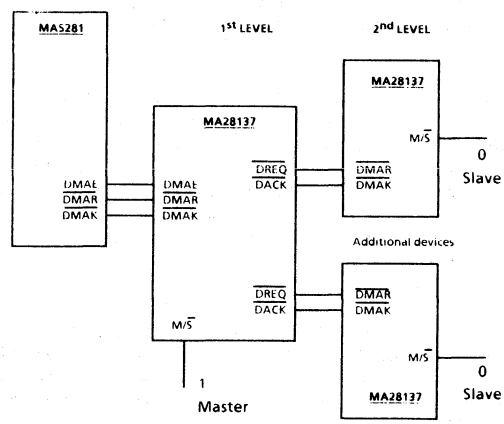


Figure 3: Connections of Cascaded DMA Controllers

4.3 Transfer Types

Each of the active transfer modes can perform three different types of transfer. These are read, write and verify.

Write transfers move data from an I/O device to memory by making MRD/WN low, IORD/WN high and toggling DSN. Similarly read transfers move data from memory to an I/O device by making MRD/WN high, IORD/WN low and toggling DSN.

Verify transfers are pseudo transfers. The MA28137 operates as in read or write transfers generating addresses and responding to EOPN, etc. However, the memory and I/O control lines all remain inactive. Verify mode is not permitted during memory to memory operation.

4.4 Memory-to-Memory

To perform block moves of data from one area of memory to another, with a minimum of program effort and time, the MA28137 includes a memory-to-memory transfer feature. Programming bit 15 in the command register selects channels 0 and 1 to operate as memory-to-memory transfer channels.

The transfer is initiated by setting the software DREQ for channel 0. The MA28137 requests a DMA service in the normal manner. After DMAKN is true, the device using eight-state transfers in block transfer mode, reads data from the memory. The channel 0 current address register is the source for the address used and is decremented or incremented in the normal manner. The data word read from the memory is stored in the MA28137 internal temporary register.

Channel 1 then writes the data from the temporary register to memory using the address in its current address register and incrementing or decrementing it in the normal manner. The channel 1 current word count is decremented. When the word count of channel 1 becomes equal to $FFFF_H$, a terminal count is generated causing an EOP output terminating the service.

Channel 0 may be programmed to retain the same address for all transfers allowing a single word to be written to a block of memory.The MA28137 will respond to external EOP signals during memory-to-memory transfers. Data comparators in block search schemes may use this input to terminate the service when a match is found. DMAKN signals are not active during memory to memory transfers.

4.5 Auto-initialisation

By programming bit 11 in the mode register a channel may be set up as an auto-initialise channel. During auto-initialise, the original values of the current address and current word count registers are automatically restored from the base address and base word count registers of that channel following EOP. The base registers are loaded when the current registers are loaded by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not set when the channel is in auto-initialise. Following auto-initialise the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected.

4.6 Priority

The MA28137 has two types of priority encoding available as software selectable options. The first is fixed priority, which fixes the channels in priority order based upon the descending value of their number. The channel with the lowest priority is 3, followed by 2, 1 and 0. After the recognition of any one channel for service, the other channels are prevented from interfering with that service until it is completed.

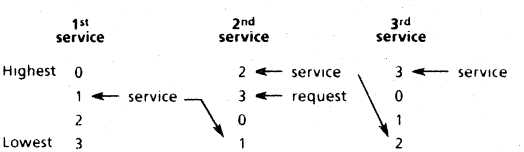


Figure 4: DMA Servicing Sequence with Rotating Priority

The second scheme is rotating priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly. With rotating priority in a single chip DMA system any device requesting service is guaranteed to be recognised after no more than three higher priority services have occurred. This prevents any one channel from monopolising the system.

5 Register Descriptions

Name	Size	Number
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current address registers	16 bits	4
Current word count registers	16 bits	4
Temporary address register	16 bits	1
Temporary word count register	16 bits	1
MMU status register	11 bits	4
Status register	8 bits	1
Temporary register	16 bits	1
Mode registers	8 bits	4
Command register	6 bits	1
Mask register	4 bits	1
Request register	3 bits	1

Table 1: Register Summary

5.1 Base Address and Base Word Count Registers

Each channel has a pair of base address and base word count registers. These 16-bit registers store the original value of their associated current registers, and are used to restore the original values to the current register after an autoinitialisation. The base registers are written simultaneously with their corresponding current register. These registers cannot be read by the microprocessor.

5.2 Current Address Register

Each channel has a 16-bit current address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the current address register during the transfer. This register is restored to its original value by an autoinitialise. Autoinitialise takes place only after an EOP.

5.3 Current Word Count Register

Each channel has a 16-bit current word count register. This register determines the number of transfers to be performed. The actual number of transfers will be one more than the number programmed in the current word count register (i.e. programming a count of 100 will result in 101 transfers). The word count is decremented after each transfer. The intermediate value of the word count is stored in the register during the transfer. When the value in the register goes from zero to $FFFF_H$, a terminal count will be generated. Following the end of a DMA service it may also be reinitialised to its original value by an autoinitialisation, however, this may only occur when an EOP occurs. If it is not autoinitialised this register will hold a count of $FFFF_H$ after TC.

5.4 MMU Status Register

Each channel has an 11-bit register associated with it which holds process and address status information for use by an MMU. During DMA transfer, the contents of this register are placed on lines AS0-3 and PS0-3 to allow the correct memory page to be selected and accessed. In addition, the signal IN/OPN is produced to select the instruction or operand page register set. The entire register is cleared by a reset.

During memory to I/O, or I/O to memory transfers, the AS and PS fields associated with the selected channel are placed on the appropriate output lines. During memory-to-memory transfer the AS and PS fields alternate between those programmed into channels 0 and 1 to allow transfers between different address states.

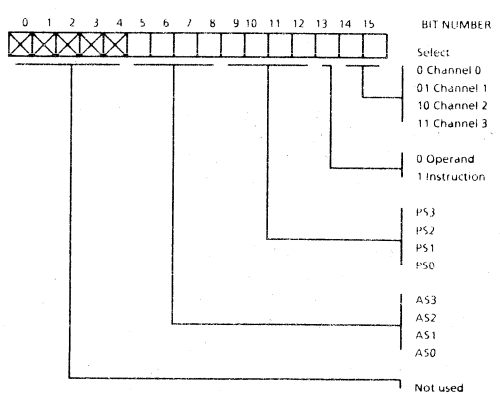


Figure 5: MMU Status Register

5.5 Status Register

The MA28137 contains a status register which can be read by the microprocessor. It contains information about the status of the device indicating which channels have reached a terminal count and which channels have pending DMA requests. Bits 15-12 are set every time a terminal count is reached by the corresponding channel or an external EOP is applied. These bits are cleared upon reset and on each status read. Bits 11-8 are set whenever their corresponding channel is requesting service.

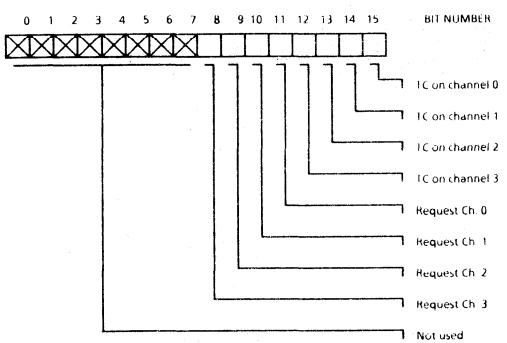


Figure 6: Status register

5.6 Temporary Register

The temporary register is used to hold data during memory-to-memory transfers. When in the program condition following the completion of a transfer, the last word transferred can be read by the microprocessor. The temporary register always contains the last word transferred in the previous memory-to-memory operation, unless cleared by a reset.

5.7 Mode Register

Each channel has an associated 8-bit mode register. When the register is being written to by the microprocessor in the program condition, bits 14 and 15, determine which channel is being addressed.

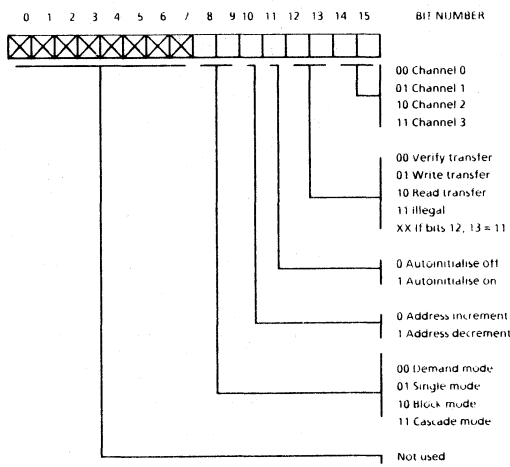


Figure 7: Mode Register

5.8 Command Register

This 6-bit register controls the operation of the MA28137. It is programmed by the microprocessor in the program condition and is cleared by Preset or a Master Clear instruction. Table 2 lists the function of the command bits (see section 6).

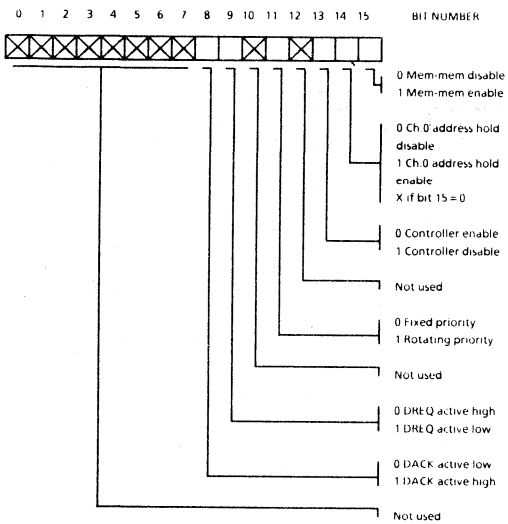


Figure 8: Command Register

5.9 Mask Register

Each channel has a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an EOP unless the channel has been programmed for autoinitialise. Each bit of the 4-bit mask register may also be set or cleared separately under software control. The entire register is also set by a Preset. Reset also disables all DMA requests until a clear mask register instruction. The instruction to separately set or clear the mask bits is similar in form to that used with the request register. All four bits of the mask register may also be written to with a single command.

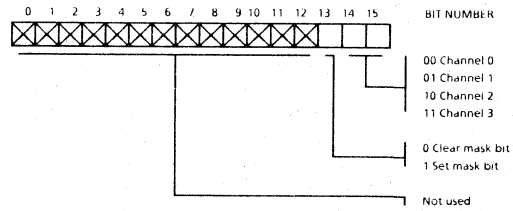


Figure 9: Mask register

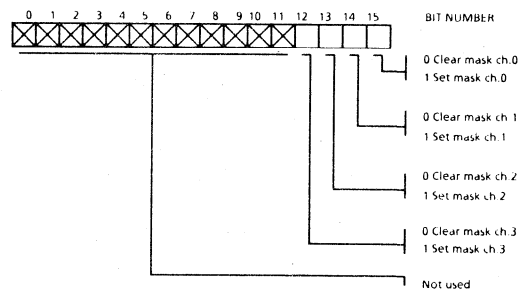


Figure 10: Mask register 4-bit write

5.10 Request Register

The MA28137 can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the request register. These are non-maskable and subject to prioritisation by the priority encoder network. Each register bit is set or reset separately under software control or is cleared upon generation of a TC or external EOP. The entire register is cleared by a reset. To set or reset a bit, the software loads the proper form of the data word. In order to make a software request, the channel must be in block mode.

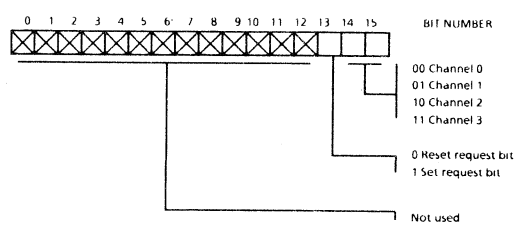


Figure 11: Request register

6 Programming

The MA28137 will accept programming from the host processor when DMAKN is inactive; this is true even if DMAR is active. The responsibility of the host is to assure that programming and DMAKN are mutually exclusive. Note that a problem can occur if a DMA request occurs on an unmasked channel while the MA28137 is being programmed. For instance, the CPU may be starting to reprogam the address register and word count of channel 1 when channel 1 receives a DMA request. If the MA28137 is enabled ie bit 13 in the command register is 0, and channel 1 is unmasked, a DMA service can occur when the address register only, has been reprogrammed. This can be avoided by disabling the controller by setting bit 13 in the command register, or masking the channel before programming any other registers. Once this is complete, the controller can be enabled or un-masked.

After power-up it is suggested that all internal locations, especially the mode registers, be loaded with some valid value. This should be done even if some channels are unused.

6.1 Software Commands

Master Clear and Clear Mash are two special software commands which can be executed in the program condition. They do not depend on any specific data bus bit pattern.

Master Clear: Has the same effect as the hardware reset. The command status, request and temporary registers are cleared and the mask register is set. The MA28137 will enter the idle cycle.

Clear Mask: Clears the mask bits of all four channels, enabling them to accept DMA requests.

Signals					Operation
A12	A13	A14	A15	RD/W	
0	0	0	0	1	Read current address register chan 0
0	0	0	0	0	Write current address register chan 0
0	0	0	1	1	Read current word count register chan 0
0	0	0	1	0	Write current word count register chan 0
0	0	1	0	1	Read current address register chan 1
0	0	1	0	0	Write current address register chan 1
0	0	1	1	1	Read current word count register chan 1
0	0	1	1	0	Write current word count register chan 1
0	1	0	0	1	Read current address register chan 2
0	1	0	0	0	Write current address register chan 2
0	1	0	1	1	Read current word count register chan 2
0	1	0	1	0	Write current word count register chan 2
0	1	1	0	1	Read current address register chan 3
0	1	1	0	0	Write current address register chan 3
0	1	1	1	1	Read current word count register chan 3
0	1	1	1	0	Write current word count register chan 3
1	0	0	0	1	Read status register
1	0	0	0	0	Write command register
1	0	0	1	1	Illegal
1	0	0	1	0	Write request register
1	0	1	0	1	Illegal
1	0	1	0	0	Write single mask register bit
1	0	1	1	1	Illegal
1	0	1	1	0	Write mode register
1	1	0	0	1	Illegal
1	1	0	0	0	Write MMU status
1	1	0	1	1	Read temporary register
1	1	0	1	0	Master Clear
1	1	1	0	1	Illegal
1	1	1	0	0	Clear mask register
1	1	1	1	1	Illegal
1	1	1	1	0	Write mask register lists

Table 2: Register Addressing

7 Pin Descriptions

7.1VDD & GND (Power & Ground)

7.2 OSC (Clock Input)
This input signal is used to generate the timing for the MA28137 internal operations and rate of data transfer. The maximum clock input is 20MHz. The internal clock OSC/2 is derived from this signal.

7.3 RDY (Ready)
A logic high on this input signal allows the MA28137 to complete the machine cycle. A low is used to extend the data strobe signal from the MA28137 to accommodate slow memories or I/O peripheral devices.

7.4 DMAE (DMA Enable)
The active high input signal DMA enable from the Central Processing Unit (CPU) indicates that DMA requests from the controller will be acknowledged.

7.5 DMAKN (DMA Acknowledge)
The CPU sets DMAKN low to indicate it has relinquished control of the system busses.

7.6 DMARN (DMA Request)
The DMA Controller requests control of the system bus from the CPU by setting DMARN low. If the corresponding mask bit is clear, the presence of a valid request causes the MA28137 to issue the DMARN to the processor. After DMARN goes active at least one clock cycle must occur before DMAKN goes active.

7.7 AD00 - AD15 (Address / Data Bus)
These connections carry multiplexed addresses and data when the MA28137 has bus control.

7.8 DSN (Data Strobe)
This is a 3-state active low signal. When DMAKN is high, the DSN signal is generated by the system processor. When the DMAKN line is low, the DMA controller produces this signal. In both cases the rising edge of DSN indicates that valid data is present on the AD bus.

7.9 AS (Address Strobe)
This 3-state active high signal functions in a similar way to DSN, except its falling edge indicates the presence of a valid address on the AD bus.

7.10 CSN (Chip Select)
Chip select is an active low input used to select the MA28137 as an I/O device during the idle cycle. This allows the CPU to communicate with the DMA Controller across the data bus.

7.11 RESET (Reset)
Reset is an active high input which clears the command, status, request and temporary registers, and sets the mask register. Following a reset the device is in the idle cycle.

7.12 DREQ 0-3 (DMA Request)
The DMA request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service The polarity of DREQ lines is programmable. Reset initialises them to active high. In fixed priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of the DREQ signal. Polarity of DREQ must be maintained until the corresponding DACK goes active.

7.13 DACK 0-3 (DMA Acknowledge)
DMA Acknowledge outputs are used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines is programmable. They are initialised to active low by Reset.

7.14 EOPN (End of Process)
End of process is an active low bidirectional signal.

The MA28137 allows an external EOP signal to terminate an active DMA service. This is accomplished by pulling the EOPN line low. The MA28137 also generates a pulse when the terminal count (TC) for an channel is reached. This generates an EOP signal which is output through the EOPN line.

The reception of EOP, either internal or external, will cause the MA28137 to terminate the service, reset the request, and, if autoinitialise is enabled, to write the base registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by EOP, unless the channel is programmed for autoinitialise. In that case, the mask bit remains clear. During memory-to-memory transfers, EOP will be output when the TC for channel 1 occurs. EOPN should be tied high with a pull-up resistor if it is not used to prevent erroneous end of process inputs.

7.15 RD/WN (Read/Write)
This input signal indicates the direction of data flow to and from the CPU. A logic '1' signifies a read by the processor.

7.16 M/ION (Memory or I/O)
This is an input from the CPU and indicates the type of instruction currently being executed by the processor.

7.17MENN (Memory Enable)
When low, this output signal enables access to the system memory.

7.18 IOENN (Input/Output Enable)
When low, this output signal enables access to the system I/O.

7.19 MRD/WN (Memory Read/Write)
This output signal defines the direction of data transfer to and from the system memory. A logic 1 implies a read from memory, logic 0 a write to memory.

7.20 IORD/WN (Input/Output Read/Write)
This output signal defines the direction of data transfer to and from the system I/O. A logic 1 implies a read from I/O, logic 0 a write to I/O.

7.21M/SN (Master/Slave Mode)
When this output is set to a logical 1 and no DMAK has been issued the controller is in master mode and will generate the system control signals MENN, IOENN, MRD/WN and IORD/W from the incoming signals M/ION and RD/WN. A logical 0 places these outputs in a high impedance state, allowing another controller to drive these lines. See the section on cascade mode for further information.

7.22 AS0-AS3 (Address Status)
These 3-state outputs are used by an MMU during expanded memory access to define the page register set used during DMA transfers.

7.23 PS0-PS3 (Process Status)
These 3-state outputs are used by an MMU during expanded memory access to provide page access protection during DMA transfers.

7.24 IN/OPN (Instruction/Operation)
This is a 3-state output used by an MMU to select the correct page register set.

8 Application Information

Figure 12 shows an example of a DMA system configned with a MA28137 controller and a MAS281 microprocessor. The multimode DMA controller issues a DMAR to the processor whenever there is at least one valid DMA request from a peripheral device. When the processor replies with a DMAK signal, the MA28137 takes control of the address/data bus and the control bus.

The system control signals MENN, IOENN, MRD/WN and IORD/WN are produced by the DMA controller during DMA access. During normal processor action these signals are decoded from M/ION and RD/WN (MAS281 signals) by the MA28137 to reduce the requirement for extra logic.

In this example only one DMAC is shown and this is designated the master DMAC (M/SN pin is tied to logic 1). In a multi-DMAC system only one DMAC would be the master controller, generating the control signals outlined above.

Figure 13 shows the use of the MA28137 in the MAS281 system in combination with a MA17504 MMU/BPU.

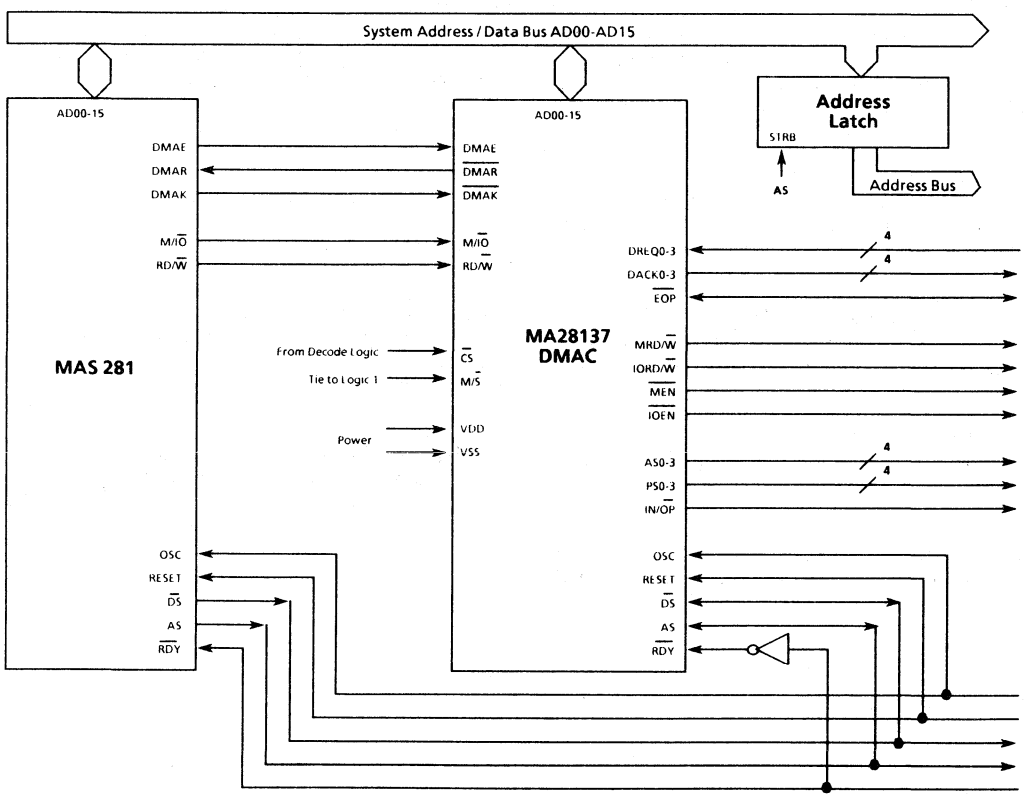


Figure 12: MA28137 - MAS281 System interfacing

MA28137

Radiation Hard Programmable DMA Controller

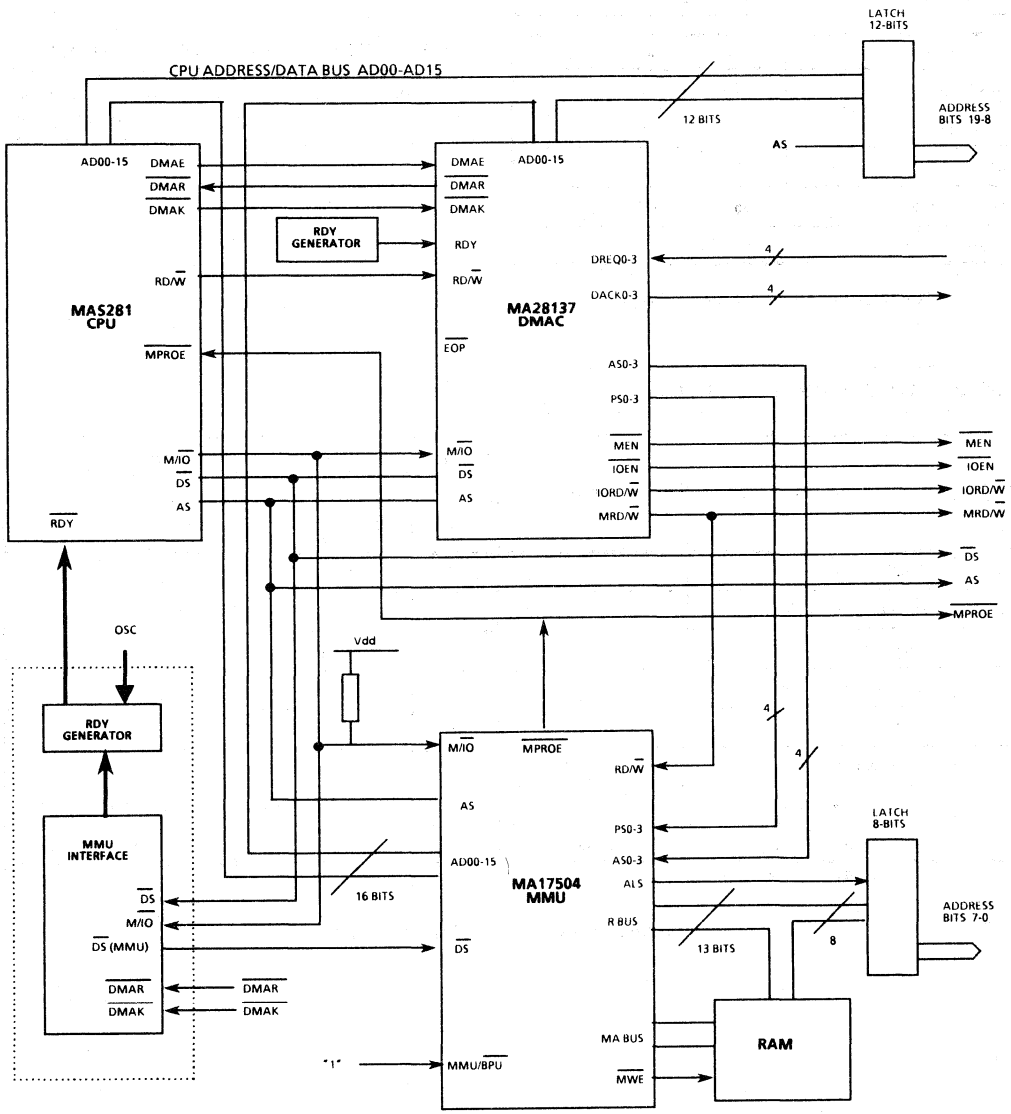


Figure 13: MA28137 - MAS281 with MMU System interfacing

9 Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Supply voltage	-0.5	10	V
Input voltage	-0.3	V_{DD} + 0.3	V
Current through any pin	-20	20	mA
Operating temperature	-55	125	°C
Storage temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

10 DC Electrical Characteristics

Symbol	Parameter	Conditions	Total dose radiation not exceeding $3x10^5$ Rad (Si)			Total dose $>3x10^5$ Rad (Si)		Units
			Min.	Typ.	Max.	Min.	Max.	
V_{DD}	Supply voltage	-	4.5	5.0	5.5	4.5	5.5	V
V_{IH}	Input high voltage	-	2.0	-	-	2.0	-	V
V_{IL}	Input low voltage	-	-	-	0.8	-	0.3	V
V_{OH}	Output high voltage	I_{OH} = -0.8mA	2.4	-	-	2.4	-	V
V_{OL}	Output low voltage	I_{OL} = 2.0mA	-	-	0.4	-	0.4	V
I_{IL}	Input leakage current	$V_{IN} = V_{SS}$ or V_{DD}	-	-	± 10	-	± 100	uA
I_{OL}	Output leakage current	$V_{OUT} = V_{SS}$ or V_{DD}	-	-	± 50	-	± 100	uA
I_{DD}	Power supply current	Static	-	-	1.0	-	10.0	mA

V_{DD} = 5V ± 10%, over full operating temperature range.

Table 4: Operating DC Electrical Characteristics

11 AC Electrical Characteristics

Number	Parameter	Min.	Max.	Units
t_1	V_{DD} applied to RESET falling	100	-	us
t_2	RESET pulse width	100	-	ns
t_3	RESET to first Program	100	-	ns
t_4	Address strobe width	70	-	ns
t_5	Data strobe width	70	-	ns
t_6	Address setup to AS lo (write)	20	-	ns
t_7	Address hold after AS lo (write)	0	-	ns
t_8	Data setup to DS hi (write)	20	-	ns
t_9	Data hold after DS hi (write)	0	-	ns
t_{10}	Chip Select lo to AS lo setup time	50	-	ns
t_{11}	Address setup to AS lo (read)	20	-	ns
t_{12}	Address hold after AS lo (read)	0	-	ns
t_{13}	NOT USED	-	-	-
t_{14}	Data valid after DS lo (read)	38	90	ns
t_{15}	Data valid after DS hi (read)	12	32	ns
t_{16}	RD/W lo to MRD/W, IORD/W lo (Non-DMA)	-	42	ns
t_{17}	M/IO lo to MEN, IOEN lo (Non-DMA)	-	37	ns
t_{18}	DREQ active to OSC hi	-	45	ns
t_{19}	Osc hi to DMAR lo	-	50	ns
t_{20}	Osc hi to DMAR hi	-	50	ns
t_{21}	Osc hi to DACK active	-	52	ns
t_{22}	Osc hi to DACK inactive	-	52	ns
t_{23}	Dmakn lo to Osc hi	-	40	ns
t_{24}	AS hi-Z to AS hi after Osc hi	-	55	ns
t_{25}	Osc hi to AS lo	-	55	ns
t_{26}	Osc hi to AS hi	-	55	ns
t_{27}	DS hi-Z to DS lo after Osc hi	-	55	ns
t_{28}	Osc hi to DS lo	-	55	ns
t_{29}	Osc hi to DS hi	-	55	ns
t_{30}	Osc hi to MEN lo	-	48	ns
t_{31}	Osc hi to MEN hi	-	48	ns
t_{32}	Osc hi to IOEN lo	-	40	ns

Table 5: AC Electrical Characteristics

Number	Parameter	Min.	Max.	Units
t_{33}	Osc hi to IOEN hi	-	40	us
t_{34}	Osc hi to MRD/W lo	-	48	ns
t_{35}	Osc hi to MRD/W hi	-	48	ns
t_{36}	Osc hi to IORD/W hi	-	48	ns
t_{37}	Osc hi to IORD/W lo	-	48	ns
t_{38}	Osc hi to Address valid (first AS)	-	110	ns
t_{39}	Osc hi to Address valid (thereafter)	-	60	ns
t_{40}	Osc hi to Address hi-Z	-	75	ns
t_{41}	Osc hi to EOPB lo	-	60	ns
t_{42}	Osc hi to EOPB hi-Z	-	60	ns
t_{43}	Osc hi to EOPB lo	-	90	ns
t_{44}	Osc hi to Address valid (first AS)	-	110	ns
t_{45}	Osc hi to Address hi-Z	-	60	ns
t_{46}	Data-in valid to Osc hi	0	-	ns
t_{47}	Osc hi to Data-in hi-Z	10	-	ns
t_{48}	Osc hi to MRD/W lo	-	50	ns
t_{49}	Osc hi to DS hi	-	55	ns
t_{50}	Osc hi to DS hi	-	55	ns
t_{51}	Osc hi to Address valid	-	110	ns
t_{52}	Osc hi to Address hi-Z	-	75	ns
t_{53}	Osc hi to Data-out valid	-	65	ns
t_{54}	Osc hi to Data-out hi-Z	-	80	ns
t_{55}	READY lo to Osc hi	8	-	ns
t_{56}	READY hi to Osc hi	8	-	ns

Table 5: AC Electrical Characteristics cont.

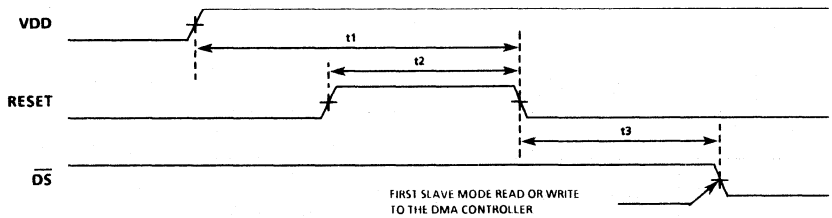


Figure 14: RESET timing

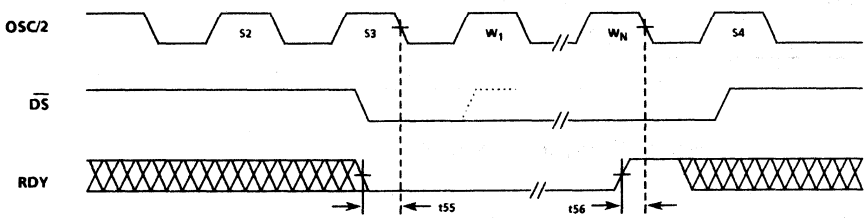


Figure15: READY Timing

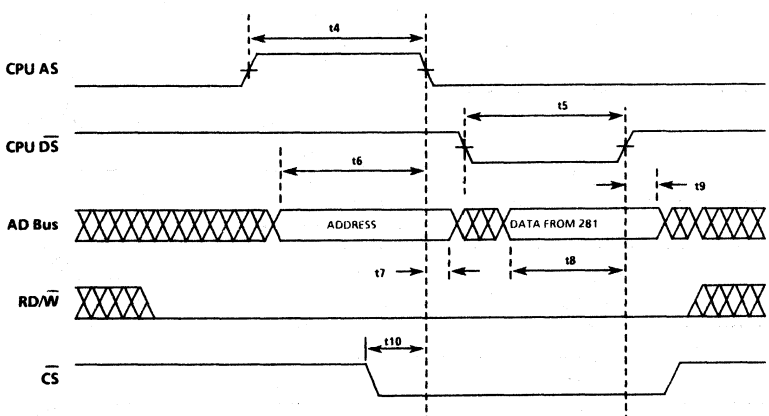


Figure 16: Programme mode CPU write timing

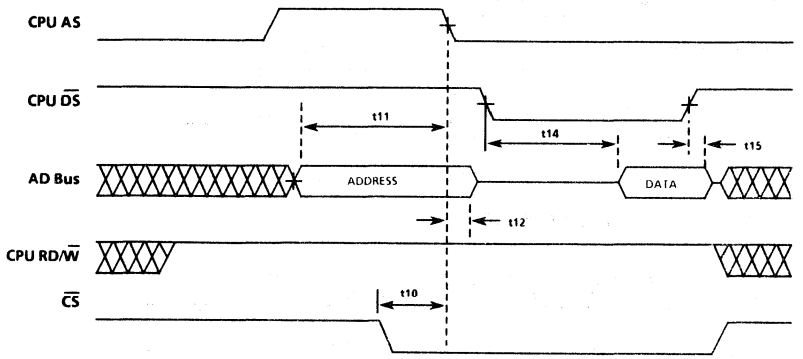


Figure 17: Programme mode CPU read timing

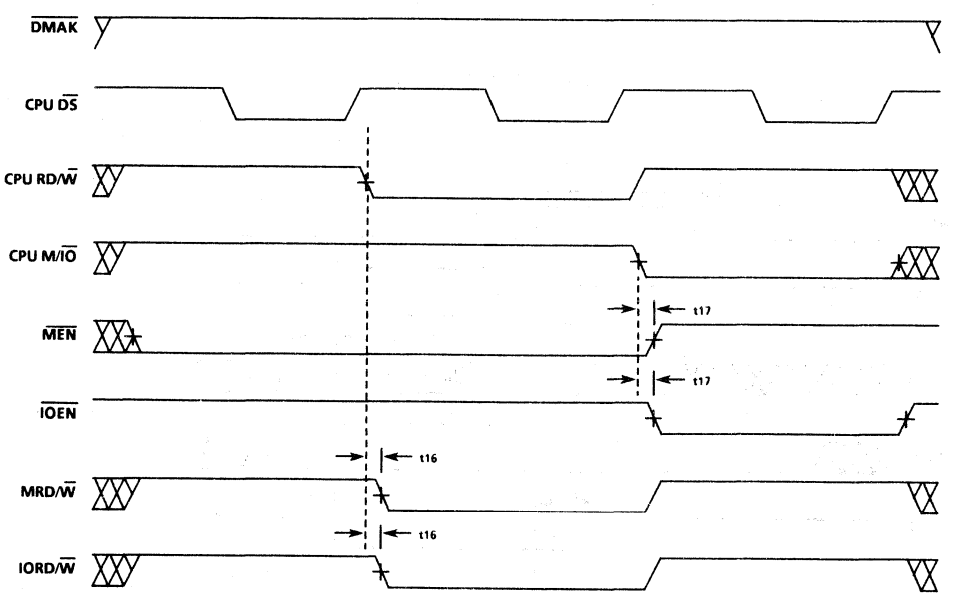
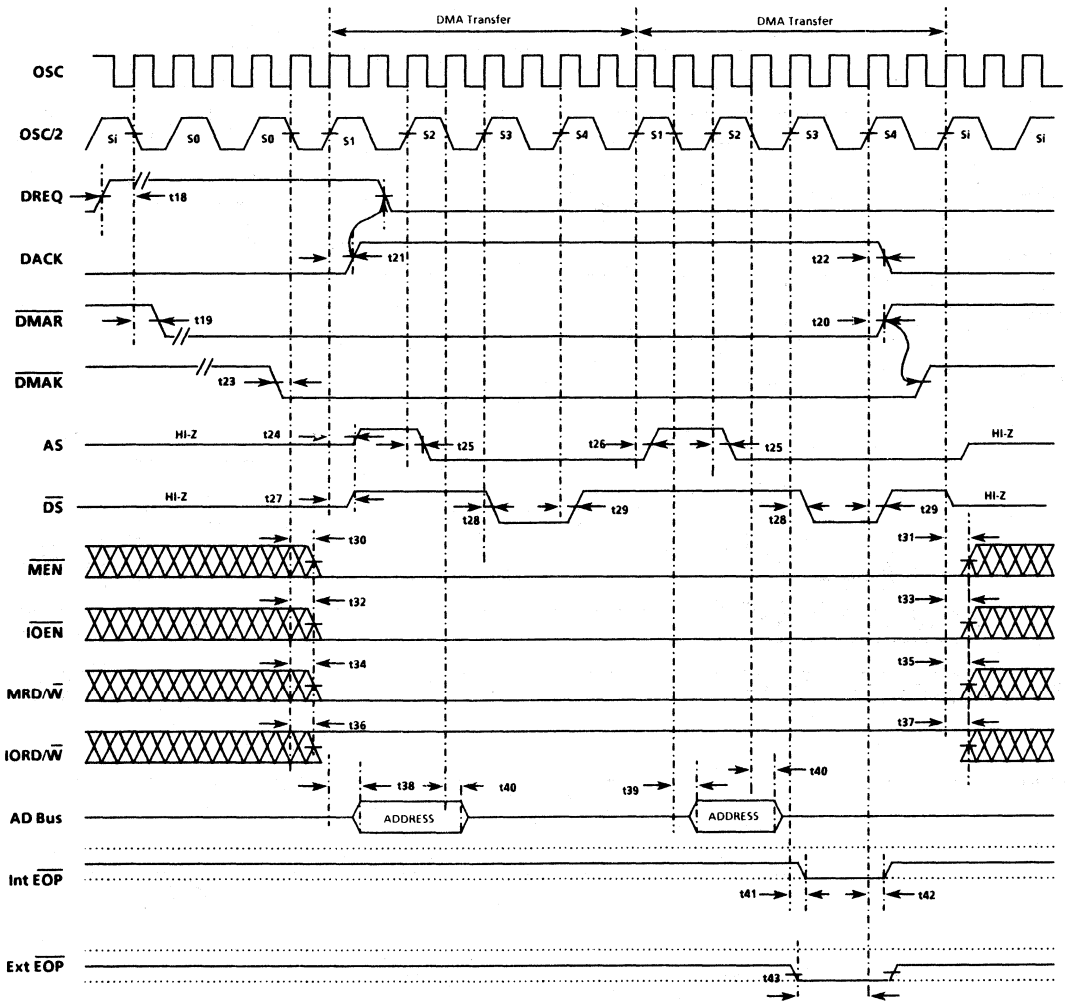


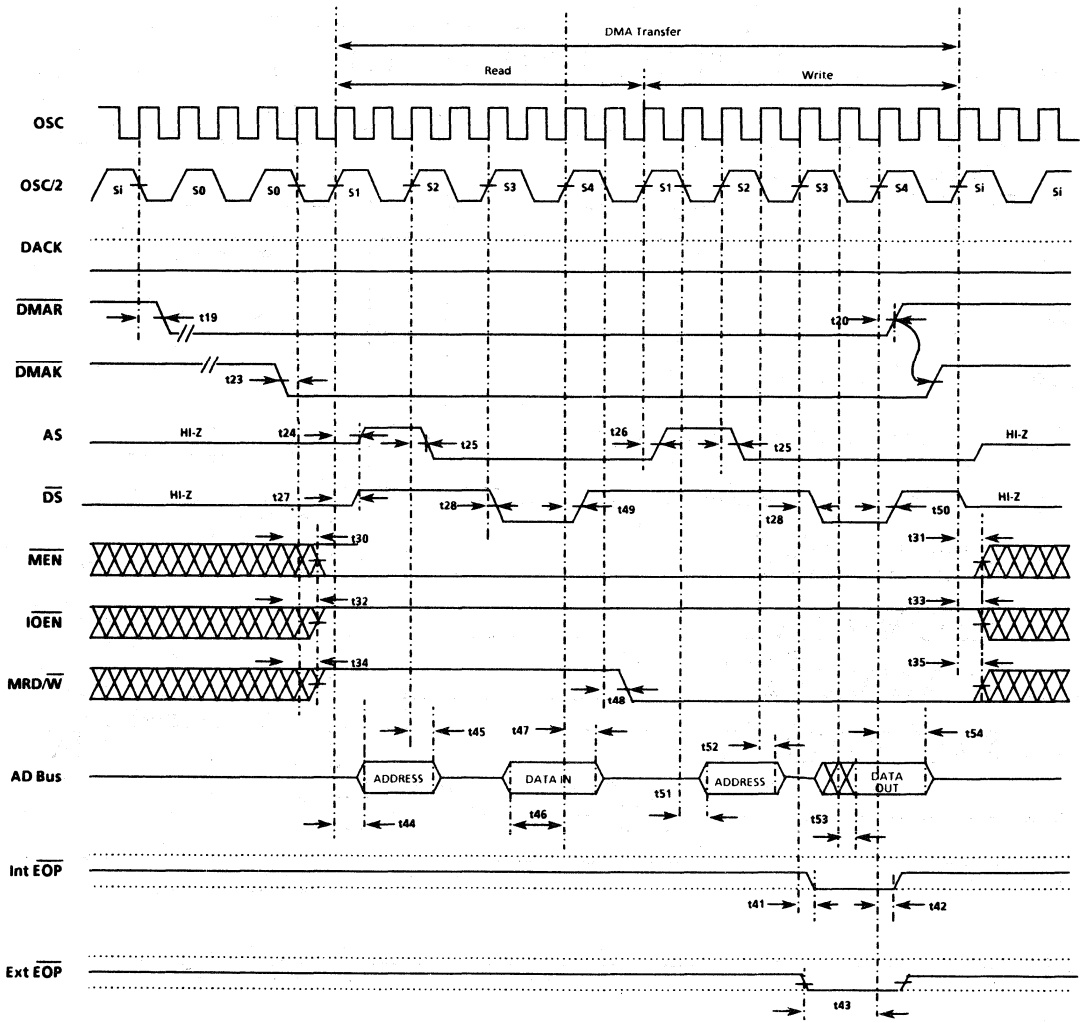
Figure 18: Memory and IO control signal timing (Non-DMA)



NOTES:

1. OSC/2 is internally generated from the input signal OSC.
2. This diagram shows a peripheral to memory transfer. The control signals MRD/W and IORD/W are in the opposite state for a memory to peripheral transfer.

Figure 19: DMA transfer timing, IO to memory.

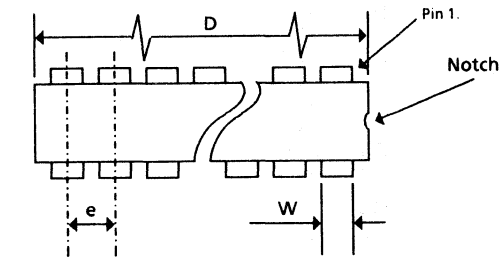


NOTES:

1. A memory to memory transfer is initiated by setting a software DREQ for channel 0.
2. OSC/2 is internally generated from the input signal OSC.

Figure 20: DMA transfer timing, memory to memory.

12 Packaging Information



Ref.	Min.	Nom.	Max.
A			5.60 (0.220)
A_1	0.38 (0.015)		1.53 (0.060)
b	0.35 (0.014)		0.59 (0.023)
c	0.20 (0.008)		0.36 (0.014)
D			82.10 (3.232)
e		2.54 (0.100) typ	
e_1		23.52 (0.900) typ	
H	4.71 (0.185)		5.38 (0.212)
M_E			23.52 (0.900)
Dimensions in mm (inches)			

MEDL XG413

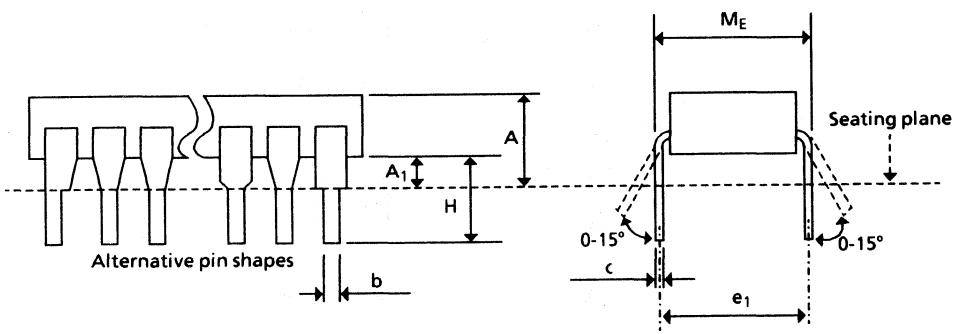


Figure 21a: 64-Lead Ceramic DIL (solder seal) - package style C

GEC PLESSEY
SEMICONDUCTORS

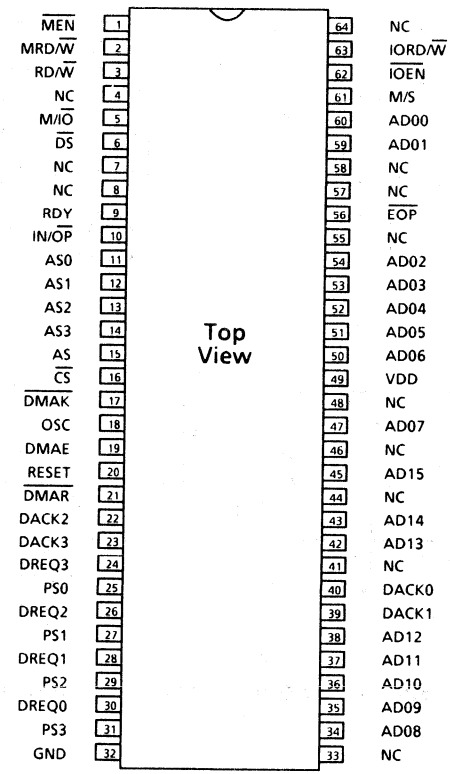
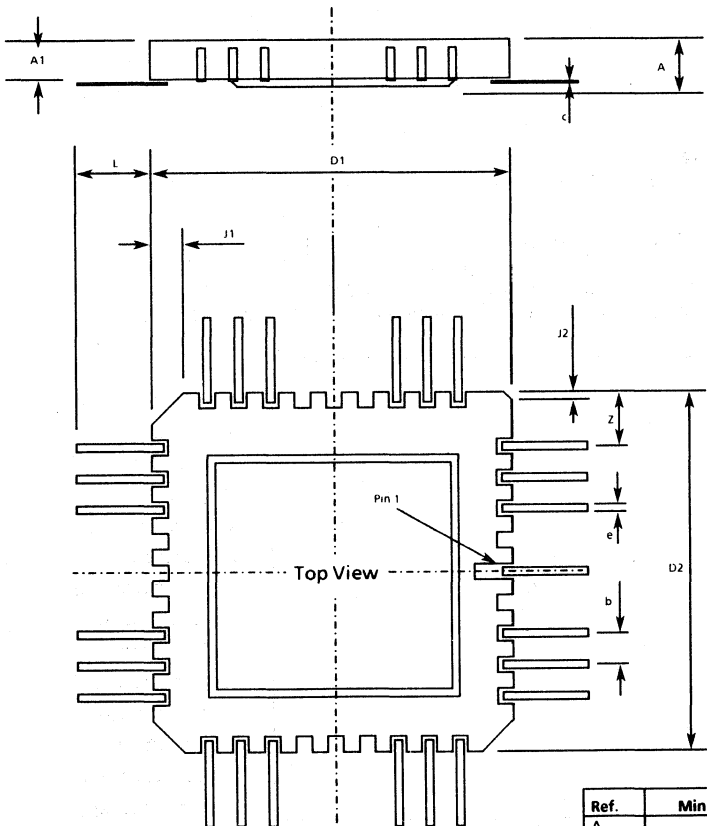


Figure 21b: 64-Lead Ceramic DIL (solder seal) - package style C

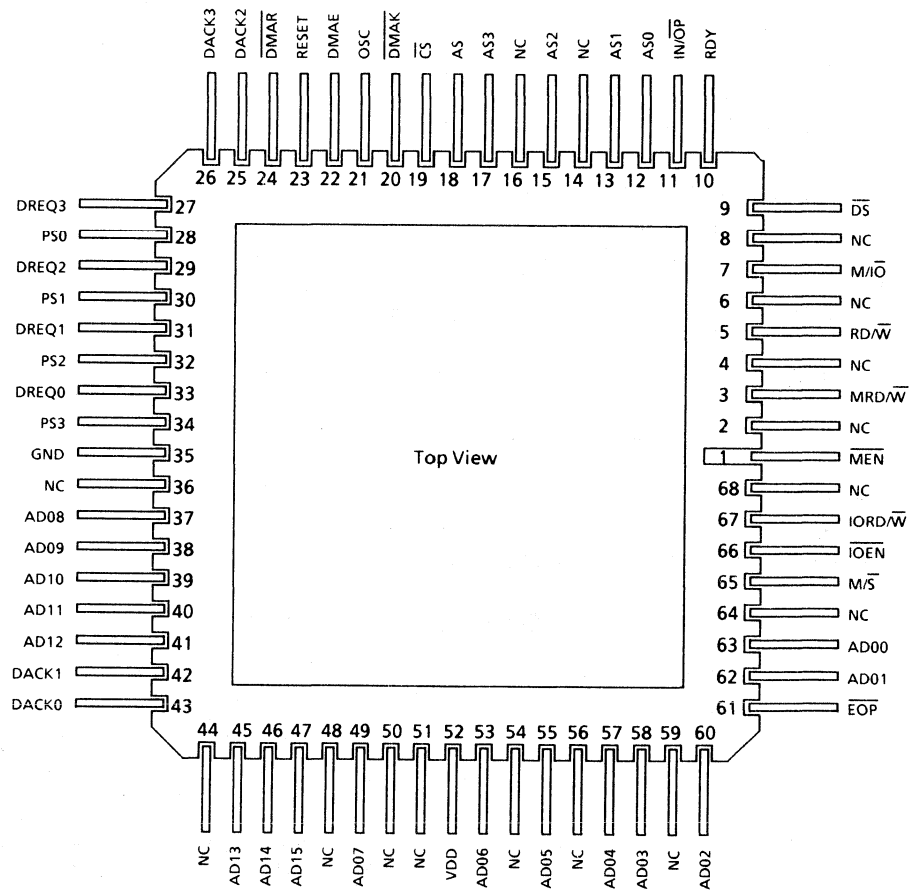


Ref.	Min.	Nom.	Max.
A			2.59 (0.102)
A_1	1.83 (0.072)		2.24 (0.088)
b	0.25 (0.010)		0.36 (0.014)
c	0.10 (0.004)		0.20 (0.008)
D1 D2	23.88 (0.940)		24.51 (0.965)
e		2.54 (0.050)	
j1		1.02 (0.040)	
j2		0.51 (0.020)	
L	8.89 (0.350)		25.85 (0.445)
Z	1.65 (0.065)		2.16 (0.085)
Dimensions in mm (inches)			

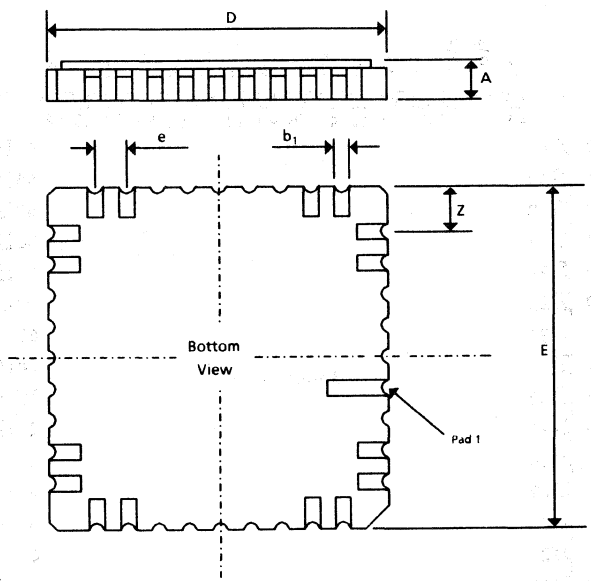
MEDL XG491

Figures 22a: 68-Lead Topbraze Flatpack (Package style F)

GEC PLESSEY
SEMICONDUCTORS



Figures 22b: 68-Lead Topbraze Flatpack (Package style F)



Ref.	Min.	Nom.	Max.
A	1.78 (0.070)	-	2.08 (0.082)
b_1	-	0.51 (0.020)	-
D	18.08 (0.712)	-	18.62 (0.733)
E	18.08 (0.712)	-	18.62 (0.733)
e	-	1.02 (0.040)	-
Z	1.40 (0.055)	-	1.78 (0.070)

Dimensions in mm (inches)

MEDL XG493

Figure 23a. 64-pad Leadless Chip Carrier (Package style L)

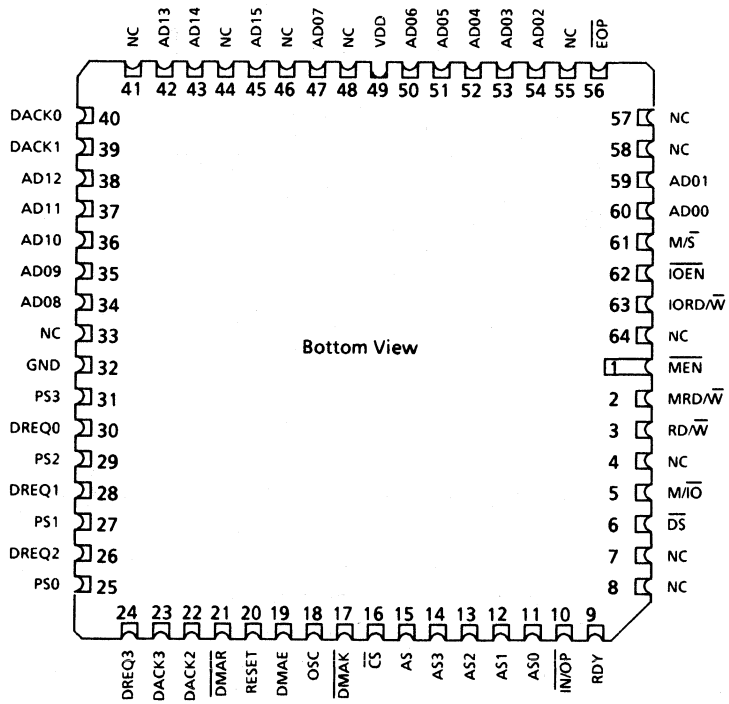


Figure 23b. 64-pad Leadless Chip Carrier (Package style L)

MA28137

Radiation Hard Programmable DMA Controller

13 Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

Total Dose (Function to specification, note 1)	$1x10^6$ Rad(Si)
Total Dose (Function to specification, note 2)	$1x10^5$ Rad(Si)
Transient Upset (Stored data loss)	3×10^{10} Rad(Si)/sec
Transient Upset (Survivability)	$>1 \times 10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	1×10^{15} neutrons/cm^2
Single Event Upset (GSO 10% worst case)	$<10^{-10}$ errors/bitday
Latch-up	Not possible

Notes: 1. Circuits with all inputs 'CMOS' types
2. Circuits with 'TTL' type inputs

3

14 Ordering Information

Unique circuit designator.

MAx28137xxxxx

Radiation Tolerance

S	Radiation hard processing
R	100 kRads (Si) guaranteed
Q	300 kRads (Si) guaranteed
H	1000 kRads (Si) guaranteed

Package Type

C	Ceramic DIL (solder seal)
F	Flatpack (solder seal)
L	Leadless Chip Carrier
N	Naked Die

QA/QCI Process (see section 9, part 4)

Test Process (see section 9, part 3)

Assembly Process (see section 9, part 2)

Reliability Level

L	Rel 0
C	Rel 1
D	Rel 2
E	Rel 3/4/5/STACK
B	Class B
S	Class S

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.

S10204FDS Issue 2 September 1990

MA28151

Radiation Hard Programmable Communication Interface

Features

- **Radiation hard to 1MRad(Si)**
- **Latch up free, high SEU immunity**
- **Silicon-on-Sapphire technology**
- **Synchronous 5-8 Bit characters; internal or external character synchronisation; automatic sync insertion**
- **Asynchronous 5-8 bit characters; clock rate-1, 16 or 64 times baud rate; break character generation; 1, 1½ or 2 stop bits.**
- **All inputs and outputs are TTL compatible**
- **Compatible with the MAS281 (MIL STD 1750A) microprocessor**

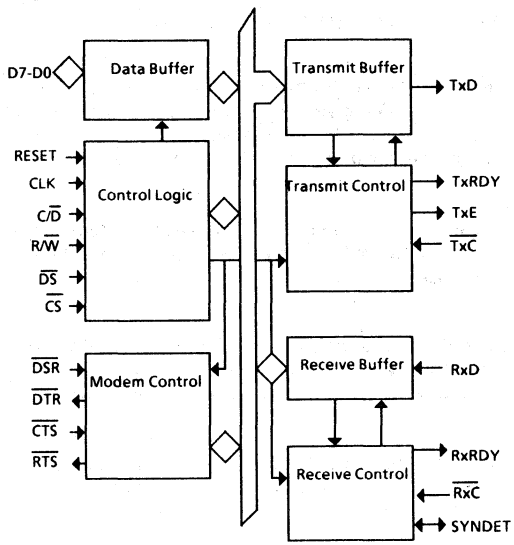


Figure 1: MA28151 Block diagarm

General Description

The MA28151 is based on the industry standard 8251A Universal Synchronous Asynchronous Receiver/Transmitter (USART), modified for data communications with the MAS281 microprocessor.

The MA28151 is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM "bi-sync"). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission.

Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART signals the CPU whenever it receives a character for transmission or whenever it receives a character for the CPU. The CPU can read the complete status of the USART at any time, including data transmission errors and control signals such as SYNDET and TxEMPTY.

MA28151

Radiation Hard Programmable Communication Interface

GEC PLESSEY

SEMICONDUCTORS

The MA28151 is based on the industry standard 8251A USART, modified for use with the MAS281 processor, incorporating the following features:

1. MA28151 has double-buffered data paths with separate I/O registers for control status, data in and data out, which considerably simplifies control programming and minimizes CPU overhead.

2. In synchronous operations, the Receiver detects and handles "break" automatically, relieving the CPU of this task.

3. A refined Rx initialisation prevents the Receiver from starting when in the "break" state, preventing unwanted interrupts from the disconnected USART.

4. At the conclusion of a transmission, the TxD line will always return to the marking state unless SBRK is programmed.

5. Tx Enable logic enhancement prevents a Tx Disable command from prematurely halting transmission of the previously written data before completion. The logic also prevents the transmitter from turning off in the middle of a word.

6. When external Sync Detect is programmed, Internal Sync Detect is disabled and an External Sync Detect status is provided via a flip-flop, which clears itself upon a status read.

7. The possibility of a false sync detect is minimized in two ways: by ensuring that if double character sync is programmed, the characters will be continuously detected and by clearing the Rx register to all 1's whenever Enter-Hunt command is issued in Sync mode.

8. When the MA28151 is not selected, the RD/$\overline{W}$ and $\overline{DS}$ lines do not affect the internal operation of the device.

9. The MA28151 Status can be read at any time but the status update will be inhibited during status read.

10. The MA28151 is free from extraneous glitches, providing higher speed and better operating margins.

11. Synchronous Baud rate is from DC to 64K.

12. Asynchronous Baud rate is from DC to 19.2K.

Functional Description

General

The MA28151 is a Universal Synchronous /Asynchronous Receiver/Transmitter designed for use with the MAS281 microprocessor. Like other I/O devices in a microcomputer system, its functional configuration is programmed by the system's software for maximum flexibility. The MA28151 can support most serial data techniques in use, including IBM bi-sync.

In a communication environment, an interface device must convert parallel format system data into serial format for transmission, and convert incoming serial data into parallel system data for reception. The interface device must also delete or insert bits or characters that are functionally unique to the communication technique. In essence, the interface should appear transparent to the CPU for the simple input or output of byte-oriented system data.

Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the MA28151 to the system data bus. Data is transmitted or received by the buffer upon execution of OUTput or INput instructions from the CPU.

Control word, Command words and Status information are also transferred through the Data Bus Buffer. The Command Status, Data-in and Data-out registers are separate 8-bit registers, communicating with the system bus through the Data Bus Buffer.

Radiation Hard Programmable Communication Interface

This functional block accepts inputs from the system control bus and generates control signals for overall device operation. It contains the Control Word Register and Command Word Register, which store the various control formats for the device's functional definition.

Reset

A high on this input forces the MA28151 into idle mode. The MA28151 will remain at idle until its functional definition is programmed with a new set of control words. Minimum RESET pulse width is 6 tcy (clock must be running).

The device can also be put into the idle state by a command reset operation.

Clock (CLK)

The CLK input is used to generate internal device timing and is normally connected to the clock generator (OSC) of the MAS281.

Please note: None of the external inputs or outputs are referenced to CLK but the frequency of CLK must be greater than 30 times the Receiver or Transmitter data bit rates.

Data Strobe ($\overline{DS}$)

This input indicates that a data transfer is taking place. During a CPU write operation the MA28151 reads data from the bus on the rising edge of $\overline{DS}$. During a read operation the MA28151 can output data while $\overline{DS}$ is low. Data is valid on the rising edge of $\overline{DS}$.

Read/Write Select (RD/$\overline{W}$)

A high on the RD/$\overline{W}$ input indicates a read of data or status information from the MA28151. A low on this input indicates a transfer of data or control words into the MA28151. The RD/$\overline{W}$ line is valid only when $\overline{DS}$ is low. Figure 2 summarises the MAS28151 read/write operations.

Control/Data (C/$\overline{D}$)

This input, in conjunction with the $\overline{DS}$ and RD/$\overline{W}$ inputs, informs the MA28151 that the word on the Data Bus is either a data character, control word or status information.

1 = CONTROL/STATUS ; 0 = DATA

C/$\overline{D}$	RD/$\overline{W}$	$\overline{DS}$	$\overline{CS}$	ACTION
0	1	0	0	28151 TO CPU
0	0	0	0	CPU TO 28151
1	1	0	0	STATUS TO CPU
1	0	0	0	CPU TO CONTROL
X	X	1	0	BUS TRISTATE
X	X	X	1	BUS TRISTATE

Figure 2: Read/Write Control

Chip Select ($\overline{CS}$)

A low on this input selects the MA28151. No reading or writing will occur unless the device is selected. When $\overline{CS}$ is high, the Data Bus is in the float state and the $\overline{DS}$ and RD/$\overline{W}$ lines have no effect on the chip.

Modem Control

The MA28151 has a set of control inputs and outputs which can be used to simplify the interface to almost any modem. The modem control signals are general purpose in nature and can be used for functions other than modem control, if necessary.

Data Set Ready ($\overline{DSR}$)

The $\overline{DSR}$ input signal is a general-purpose, 1-bit inverting input port. Its condition can be tested by the CPU using a Status Read operation. The $\overline{DSR}$ input is normally used to test modem conditions such as Data Set Ready.

Data Terminal Ready ($\overline{DTR}$)

The $\overline{DTR}$ output signal is a general purpose, 1-bit inverting output port. It can be set low by programming the appropriate bit in the Command instruction word. The $\overline{DTR}$ output signal is normally used for modem control such as Data Terminal Ready.

Request to Send ($\overline{RTS}$)

The $\overline{RTS}$ output signal is a general purpose, 1-bit inverting output port. It can be set low by programming the appropriate bit in the Command instruction word. The $\overline{RTS}$ output signal is normally used for modem control such as Request To Send.

Clear to Send ($\overline{CTS}$)

A low on this input enables the MA28151 to transmit serial data if the Tx Enable bit in the Command byte is set to a high. If either a Tx Enable off or $\overline{CTS}$ off condition occurs while the Tx is in operation, the Tx will transmit all the data in the USART, written prior to Tx disable command, before shutting down.

Transmitter Buffer

The Transmitter Buffer accepts parallel data from the Data Bus Buffer, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin on the falling edge of $\overline{TxC}$. The transmitter will begin transmission upon being enabled if $\overline{CTS} = 0$. The TxD line will be held in the marking state immediately upon a master Reset, or when Tx Enable or $\overline{CTS} = 1$, or the transmitter is empty.

Transmitter Control

The Transmitter Control manages all activities associated with the transmission of serial data. It accepts and issues signals both externally and internally to accomplish this function.

Transmitter Ready (TxRDY)

This output signals the CPU that the transmitter is ready to accept a data character. The TxRDY output pin can be used as an interrupt to the system since it is masked by TxEnable; or, for Polled operation, the CPU can check TxRDY using a Status Read operation. TxRDY is automatically reset by the falling edge of $\overline{DS}$ (with RD/$\overline{W}$ low) when a data character is loaded from the CPU.

Note that when using the polled operation, the TxRDY status bit is *not* masked by TxEnable, but will only indicate the Empty/Full Status of the Tx Data input Register.

Transmitter Empty (TxE)

When the MA28151 has no characters to send, the TxEMPTY output will go high. It resets upon receiving a character from CPU if the transmitter is enabled. TxEMPTY remains high when the transmitter is disabled. TxEMPTY can be used to indicate the end of transmission mode, so that the CPU can turn the line around in the half-duplex operational mode.

In the Synchronous mode, a high on the TxEMPTY output indicates that a character has not been loaded and the SYNC character or characters are about to be or are being automatically transmitted as fillers. TxEMPTY does not go low when the SYNC characters are being shifted out.

Transmitter Clock ($\overline{TxC}$)

The Transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous transmission mode, the Baud Rate (1x) is equal to the $\overline{TxC}$ frequency. In Asynchronous transmission mode, the baud rate is a fraction of the actual $\overline{TxC}$ frequency. A portion of the mode instruction selects this factor; it can be 1, 1/16 or 1/64 the $\overline{TxC}$.

For Example:
If Baud Rate equals 110 Baud
$\overline{TxC}$ equals 110Hz in the 1x mode
$\overline{TxC}$ equals 1.72 KHz in the 16x mode
$\overline{TxC}$ equals 7.04 KHz in the 64x mode
The falling edge of $\overline{TxC}$ shifts the serial data out of the MA28151.

Receiver Buffer

The Receiver accepts serial data, converts the data to parallel format, checks for bits or characters that are unique to the communications techniques and sends an assembled character to the CPU. Serial data is input to the RxD pin and is clocked in on the rising edge of $\overline{RxC}$.

Receiver Control

This functional block manages all receiver-related activities which consist of the following features:

The RxD initialisation circuit prevents the MA28151 from mistaking an unused input line for an active low data line in the break condition. Before starting to receive serial characters on the RxD line, a valid 1 must first be detected after a chip master Reset. Once this has been determined, a search for a valid low (start bit) is enabled. This feature is only active in the asynchronous mode and is only done once for each master Reset.

The False Start bit detection circuit prevents false starts as the result of a transient noise spike by first detecting the falling edge and then strobing the nominal center of the Start bit (RxD = low).

Parity error detection sets the corresponding status bit.

The Framing Error status bit is set if the Stop bit is absent at the end of the data byte (asynchronous mode).

RxRDY (Receiver Ready)

This output indicates that the MA28151 contains a character that is ready to be input to the CPU. RxRDY can be connected to the interrupt structure of the CPU or, for polled operation, the CPU can check the condition of RxRDY using a Status Read operation. RxEnable, when off holds RxRDY in the Reset Condition. For Asynchronous mode, to set RxRDY, the Receiver must be enabled to sense a Start Bit and a complete character must be assembled and transferred to the Data Output Register. For Synchronous mode, to set RxRDY, the Receiver must be enabled and a character must finish assembly and be transferred to the Data Output Register.

Failure to read the received character from the Rx Data Output Register prior to the assembly of the next Rx Data character will set overrun condition error and the previous character will be written over and lost. If the Rx Data is being read by the CPU when the internal transfer is occurring, the overrun error will be set and the old character will be lost.

3

$\overline{RxC}$ (Receiver Clock)

The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode the Baud Rate (1x) is equal to the actual frequency of $\overline{RxC}$. In Asynchronous Mode, the Baud Rate is a fraction of the actual $\overline{RxC}$ frequency. A portion of the mode instruction selects this factor: 1, 1/16 or 1/64 of the Receiver Clock.

For example:
Baud Rate equals 300 Baud, if
$\overline{RxC}$ equals 300 Hz in the 1x mode:
$\overline{RxC}$ equals 4800 Hz in the 16x mode
$\overline{RxC}$ equals 19.2 KHz in the 64x mode.
Baud Rate equals 2400 Baud if
$\overline{RxC}$ equals 2400Hz in the 1x mode
$\overline{RxC}$ equals 38.4 KHz in the 16x mode;
$\overline{RxC}$ equals 153.6 KHz in the 64x mode.
Data is sampled into the MA28151 on the rising edge of $\overline{RxC}$.

Note: In most communications systems, the MA28151 will be handling both the transmission and reception operations of a single link. Consequently the Receive and Transmit Baud Rates will be the same. Both $\overline{TxC}$ and $\overline{RxC}$ will require identical frequencies for this operation and can be tied together and connected to a single frequency source (Baud Rate Generator) to simplify the interface.

Sync/Break Detect (SYNDET/BRKDET)

This pin is used in Synchronous Mode for SYNDET and may be used as either input or output, programmable through the Control Word. It is reset to output mode, low upon RESET. When used as an output (internal Sync mode), the SYNDET pin will go high to indicate that the MA28151 has located the SYNC character in the Receive mode. If the MA28151 is programmed to use double Sync characters (bi-sync), the SYNDET will go high in the middle of the last bit of the second Sync character.

SYNDET is automatically reset upon a Status Read operation.

When used as an input (external SYNC detect mode), a positive going signal will cause the MA28151 to start assembling data characters on the rising edge of the next $\overline{RxC}$. Once in SYNC, the high input signal can be removed. When External SYNC Detect is programmed, Internal SYNC Detect is disabled.

BREAK (Async Mode Only)

This output will go high whenever the receiver remains low through two consecutive stop bit sequences including the start bits, data bits, and parity bits. Break Detect may also be read as a Status bit. It is reset only upon a master chip Reset or Rx Data returning to a "one" state.

C/$\overline{D}$	ACTION
1	MODE INSTRUCTION
1	SYNC CHARACTER 1 (SYNC ONLY) *
1	SYNC CHARACTER 2 (SYNC ONLY) *
1	COMMAND INSTRUCTION
0	DATA
1	COMMAND INSTRUCTION
0	DATA
1	COMMAND INSTRUCTION

Note: The second sync character is skipped if mode instruction has programmed the MA28151 to single character mode. Both sync characters are skipped if mode instruction has programmed the MA28151 to async mode.

Figure 3: Typical data block

Operation Description

General

The complete functional definition of the MA28151 is programmed by the system's software. A set of control words must be sent out by the CPU to initialize the MA28151 to support the desired communications format. These control words will program the: BAUD RATE, CHARACTER LENGTH, NUMBER OF STOP BITS, SYNCHRONOUS or ASYNCHRONOUS OPERATION, EVEN/ODD/OFF PARITY, etc.. In the Synchronous Mode, options are also provided to select either internal or external character synchronization.

Once programmed, the MA28151 is ready to perform its communication functions. The TxRDY output is raised high to signal the CPU that the MA28151 is ready to receive a data character from the CPU. This output (TxRDY) is reset automatically when the CPU writes a character into the MA28151. Alternatively, the MA28151 receives serial data from the MODEM or I/O device. Upon receiving an entire character, the RxRDY output is raised high to signal the CPU that the MA28151 has a complete character ready for the CPU to fetch. RxRDY is reset automatically upon the CPU data read operation.

The MA28151 cannot begin transmission until the TxEnable (Transmitter Enable) bit is set in the Command instruction and it has received a Clear To Send ($\overline{CTS}$) input. The TxD output will be held in the marking state upon Reset.

Programming the MA28151

Mode and Command Instructions

Prior to starting data transmission or reception, the MA28151 must be loaded with a set of control words generated by the CPU. These control signals define the complete functional definition of the MA28151 and must immediately follow a Reset operation (internal or external)

The control words are split into two formats:
1. Mode Instruction
2. Command Instruction

Mode Instruction

This instruction defines the general operational characteristics of the MA28151. It must follow a Reset operation (internal or external). Once the Mode instruction has been written into the MA28151 by the CPU, SYNC characters or Command Instructions may be written.

Command Instruction

This instruction defines a word that is used to control the actual operation of the MA28151.

Both the Mode and Command Instruction must conform to a specified sequence for proper device operation. The Mode instruction must be written immediately following a Reset operation, prior to using the MA28151 for data communications.

All control words written into the MA28151 after the Mode Instruction will load the Command Instruction. Command Instructions can be written into the MA28151 at any time in the data block during the operation of the MA28151. To return to the Mode Instruction format, the master Reset bit in the Command Instruction word can be set to initiate an internal Reset operation. This automatically places the MA28151 back into the Mode Instruction format. Command Instructions must follow the Mode Instructions or Sync characters.

Mode Instruction Definition

The MA28151 can be used for either Asynchronous or Synchronous data communications. To understand how the Mode Instruction defines the functional operation of the MA28151, the designer can best view the device as two separate components, one Asynchronous and the other Synchronous, sharing the same package. The format definition can be changed only after a master chip Reset. For explanation purposes the two formats will be isolated.

NOTE: When parity is enabled it is not considered as one of the data bits for the purpose of programming the word length. The actual parity bit received on the Rx Data line cannot be read on the Data Bus. In the case of a programmed character length of less than 8 bits, the least significant data bus bits will hold the data; unused bits are 'don't care' when writing data to the MA28151, and will be zeros when reading the data from the MA28151.

Test Mode

The Mode Instruction can be used to select a scan path test facility. In this mode a test vector is read in through RxD and read out in TxD. For further information of test mode please contact a Marconi Electronic Devices at the address on page 1.

Asynchronous Mode (Transmission)

Whenever a data character is sent by the CPU the MA28151 automatically adds a Start bit (low level), followed by the data bits (least significant bit first,) and the programmed number of Stop bits to each character. Also, an even or odd Parity bit is inserted prior to the Stop bit(s), as defined by the Mode Instruction. The Character is then transmitted as a serial data stream on the TxD output. The serial data is shifted out on the falling edge of $\overline{TxC}$ at a rate equal to 1, 1/16 or 1/64 times that of the $\overline{TxC}$, as defined by the Mode Instruction. BREAK characters can be continuously sent to the TxD if commanded to do so.

When no data characters have been loaded into the MA28151 the TxD output remains high (marking) unless a Break (continuously low) has been programmed.

Asynchronous Mode (Receive)

The RxD line is normally high. A falling edge on this line triggers the beginning of a START bit. The validity of this START bit is checked by again strobing this bit at its nominal center (16x or 64X mode only). If a low is detected again, it is a valid START bit, and the bit counter will start counting. The bit counter thus locates the center of the data bits, the parity bit (if it exists) and the stop bits. If a parity error occurs, the parity error flag is set. Data and parity bits are sampled on the RxD pin with the rising edge of $\overline{RxC}$. If a low level is detected as the STOP bit, the Framing Error flag will be set. The STOP bit signals the end of a character. Note that the receiver requires only one stop bit, regardless of the number of stop bits programmed. This character is then loaded into the parallel I/O buffer of the MA28151. The RxRDY pin is raised to signal the CPU that a character is ready to be fetched.

If a previous character has not been fetched by the CPU, the present character replaces it in the I/O buffer, and the OVERRUN Error flag is raised (thus the previous character is lost). All of the error flags can be reset by an Error Reset Instruction. The occurrence of any of these errors will not affect the operation of the MA28151.

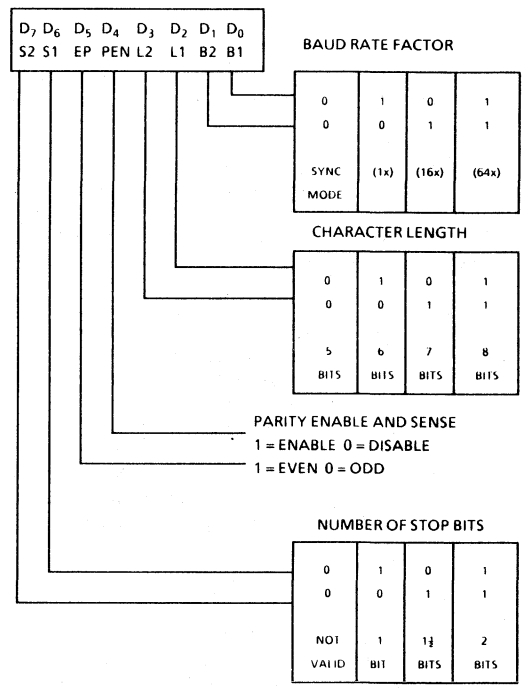


Figure 4: Mode instruction format, asynchronous mode

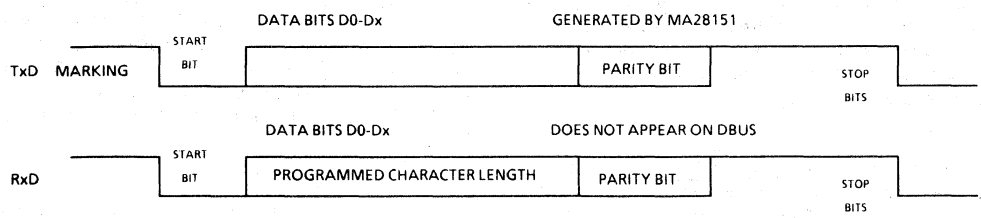


Figure 5: Asynchronous Mode

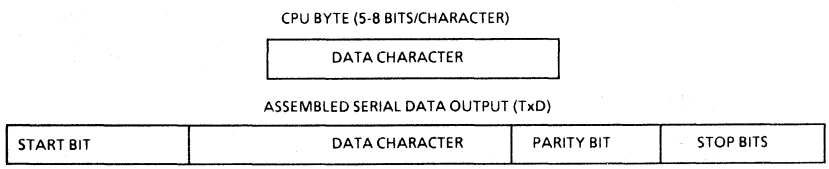
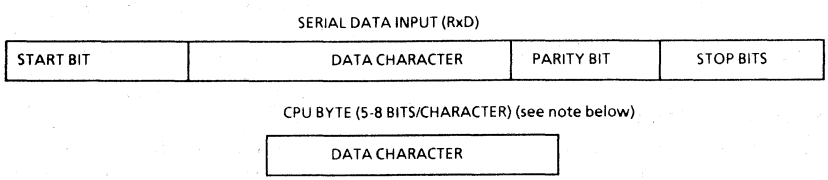


Figure 6: Transmission Format



NOTE: If character length is defined as 5,6,or 7 bits the unused bits are set to zero.

Figure 7: Receive Format

Synchronous Mode (Transmission)

The TxD output is continuously high until the CPU sends its first character to the MA28151 which usually is a SYNC character. When the $\overline{CTS}$ line goes low, the first character is serially transmitted out. All characters are shifted out on the falling edge of $\overline{TxC}$. Data is shifted out at the same rate as the $\overline{TxC}$.

Once transmission has started, the data stream at the TxD output must continue at the $\overline{TxC}$ rate. If the CPU does not provide the MA28151 with a data character before the MA28151 Transmitter Buffers become empty, the SYNC characters (or character if in single SYNC character mode) will be automatically inserted in the TxD data stream. In this case, the TxEMPTY does not go low when the SYNC is being shifted out (see figure below). The TxEMPTY pin is internally reset by a data character being written into the MA28151.

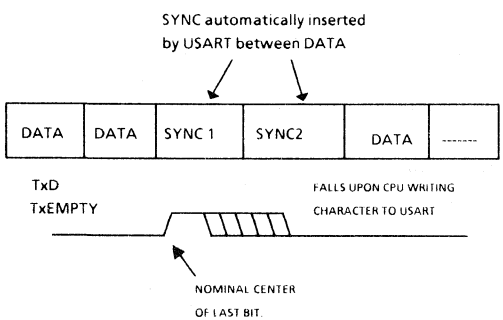


Figure 8: Sync Character Insertion

Synchronous Mode (Receiver)

In this mode character synchronisation can be internally or externally achieved. If the SYNC mode has been programmed, ENTER-HUNT command should be included in the first command instruction word written. Data on the RxD pin is then sampled on the rising edge of $\overline{RxC}$. The content of the Rx buffer is compared to every bit boundary with the first SYNC character until a match occurs.

If the MA28151 has been programmed for two SYNC characters, the subsequent received character is also compared; when both SYNC characters have been detected, the USART ends the HUNT mode and is in character synchronization. The SYNDET pin is then set high, and is reset automatically by a STATUS READ. If parity is programmed, SYNDET will not be set until the middle of the parity bit, instead of the middle of the last data bit.

In the external SYNC mode, synchronization is achieved by applying a high level on the SYNDET pin, thus forcing the MA28151 out of the HUNT mode. The high level can be removed after one $\overline{RxC}$ cycle. An ENTER HUNT command has no effect in the asynchronous mode of operation.

Parity error and overrun error are both checked in the same way as in the Asynchronous Receive mode. Parity is checked when not in HUNT, regardless of whether the Receiver is enabled or not.

The CPU can command the receiver to enter the HUNT mode if synchronisation is lost. This will also set all the used character bits in the buffer to a one thus preventing a possible false SYNDET caused by data that happens to be in the Rx buffer at ENTER HUNT time.

Note: the SYNDET flip-flop is reset at each Status Read, regardless of whether internal of external SYNC has been programmed. This does not cause the MA28151 to return to the HUNT mode. When in SYNC mode, but not in HUNT, Sync Detection is still functional, but only occurs at the known word boundaries. Thus, if one Status Read indicates SYNDET and a second Status Read also indicates SYNDET, then the programmed SYNDET characters have been received since the previous Status Read. (If double character sync has been contiguously received to gate a SYNDET indication) When external SYNDET mode is selected,internal Sync Detect is disabled, and the SYNDET flip-flop may be set at any bit boundary.

Data Format, Synchronous Mode

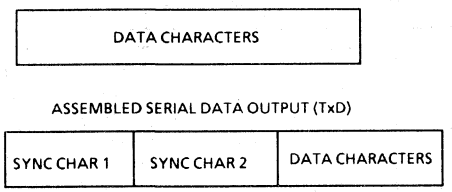


Figure 9: Receive Format, Synchronous Mode

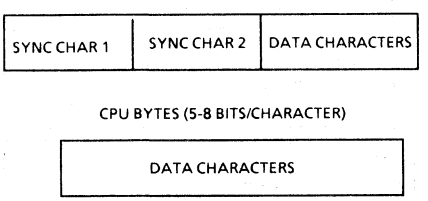


Figure 10: Data Format, Synchronous Mode

Mode Instruction Format, Synchronous Mode

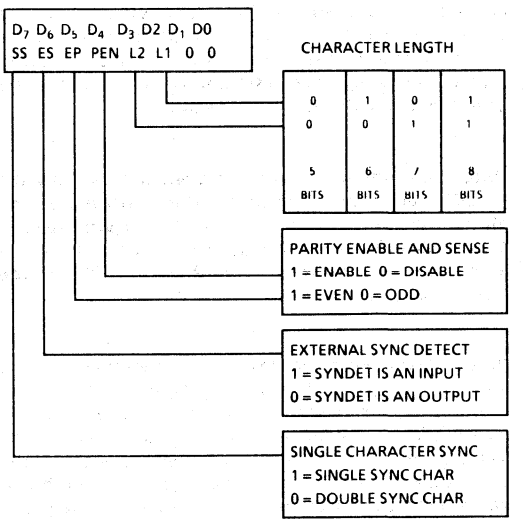


Figure 11: Mode Instruction Format, Synchronous Mode

Radiation Hard Programmable Communication Interface

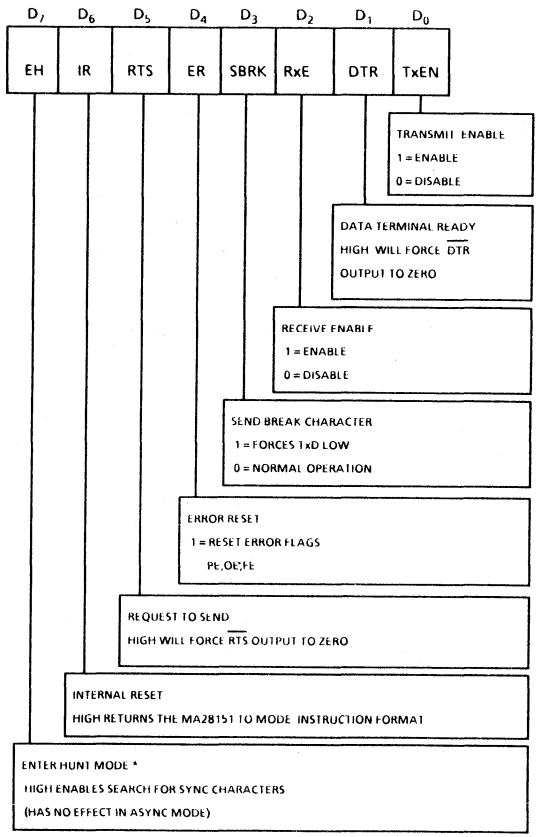
Command Instruction Definition

Once the functional definition of the MA28151 has been programmed by the Mode Instruction and the sync characters are loaded (if in Sync Mode) then the device is ready to be used for data communications. The Command Instruction controls the actual operation of the selected format. Functions such as: Enable Transmit/Receive, Error Reset and Modem Controls are provided by the Command Instruction.

Once the Mode Instruction has been written into the MA28151 and Sync characters inserted, if necessary, then all further "control writes" ($C/\overline{D} = 1$) will load a Command Instruction. A Reset Operation (internal or external) will return the MA28151 to the Mode instruction format.

Note: Internal Reset on Power-up. When power is first applied, the MA28151 may come up in the Mode, Sync character or Command format. To guarantee that the device is in the Command instruction format before the Reset command is issued, it is safest to execute the worst-case initialization sequence (sync mode with two sync characters). Loading three 00Hs consecutively into the device with $C/\overline{D} = 1$ configures sync operation and writes two dummy 00H sync characters. An internal reset command (40H) may then be issued to return the device to the idle state.

Command Instruction Format



*Note: ERROR RESET Must be performed whenever RxENABLE and ENTER-HUNT are programmed

Figure 12: Command Instruction Format

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Radiation Hard Programmable Communication Interface

Status Read Definition

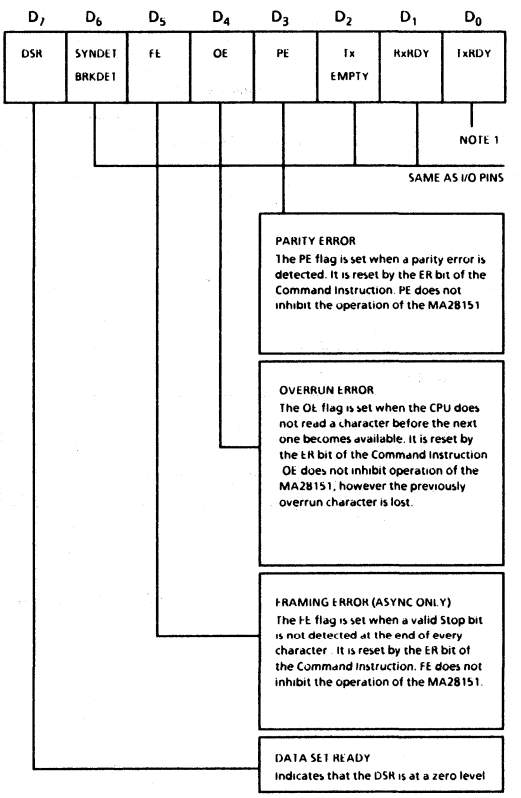
In data communication systems it is often necessary to examine the status of the active device to ascertain if errors have occurred or other conditions that require the processor's attention. The MA28151 has facilities that allow the programmer to read the status of the device at any time during the functional operation. (Status update is inhibited during status read).

A normal read command is issued by the CPU with $C/\overline{D}$ high to accomplish this function.

Some of the bits in the Status Read Format have identical meanings to external output pins so that the MA28151 can be used in a completely polled or interrupt-driven environment. TxRDY is an exception.

Note that status update can have a maximum delay of 28 clock periods from the actual event affecting the status.

Status Read Format



NOTE 1:
TxRDY status bit has different meanings from the TxRDY output pin. The former is not conditioned by $\overline{CTS}$ and TxEN, the latter is conditioned by both CTS and $\overline{TxEN}$.
i.e. TxRDY status bit 0 DB buffer empty
TxRDY pin out = DB buffer empty OR ($\overline{CTSN}$ = 0) OR (TxEN = 1)

Figure 13: Status Read Format

Timing Waveforms

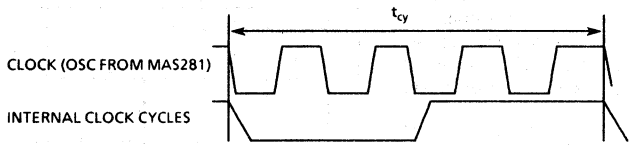


Figure 14: System Clock Input

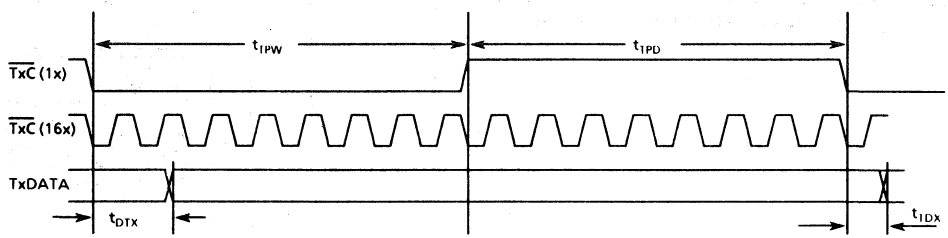


Figure 15: Transmitter Clock and Data

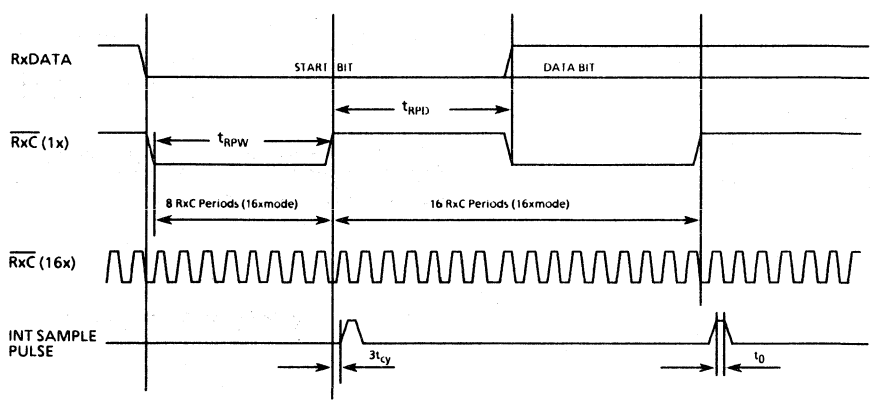


Figure 16: Receive Clock and Data

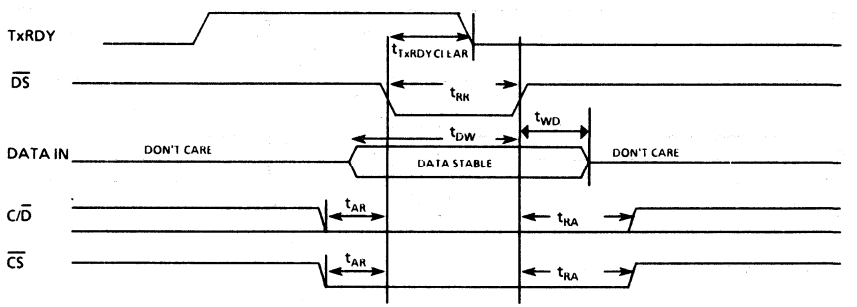


Figure 17: Write Data Cycle (CPU to USART)

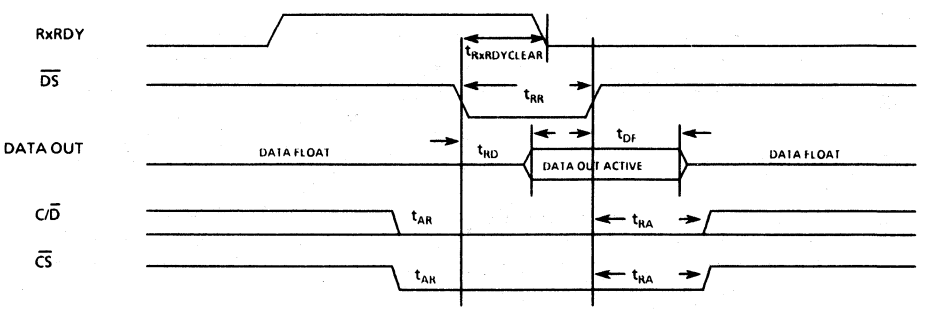
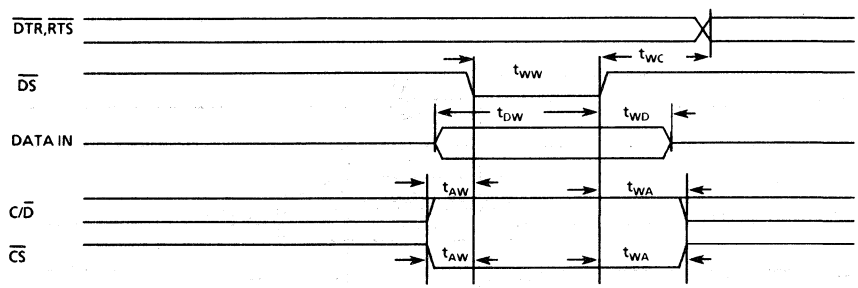
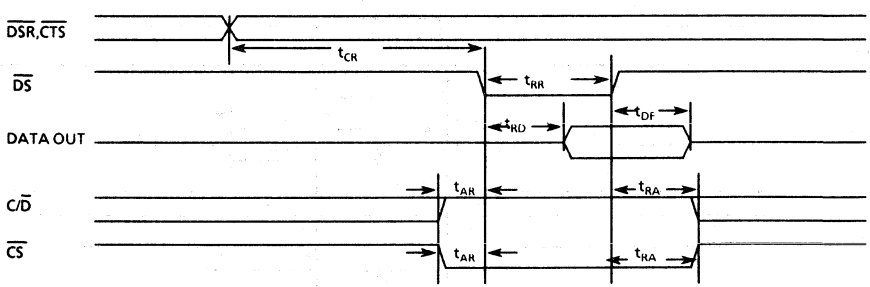


Figure 18: Read Data Cycle (USART to CPU)



NOTE : t_{WC} INCLUDES THE RESPONSE TIMING OF A CONTROL BYTE

Figure 19: Write Control or Output Port Cycle (CPU to USART)



NOTE : t_{CR} INCLUDES THE EFFECT OF CTS ON THE TxENABLE CIRCUITRY

Figure 20: Read Control or Output Port Cycle (USART to CPU)

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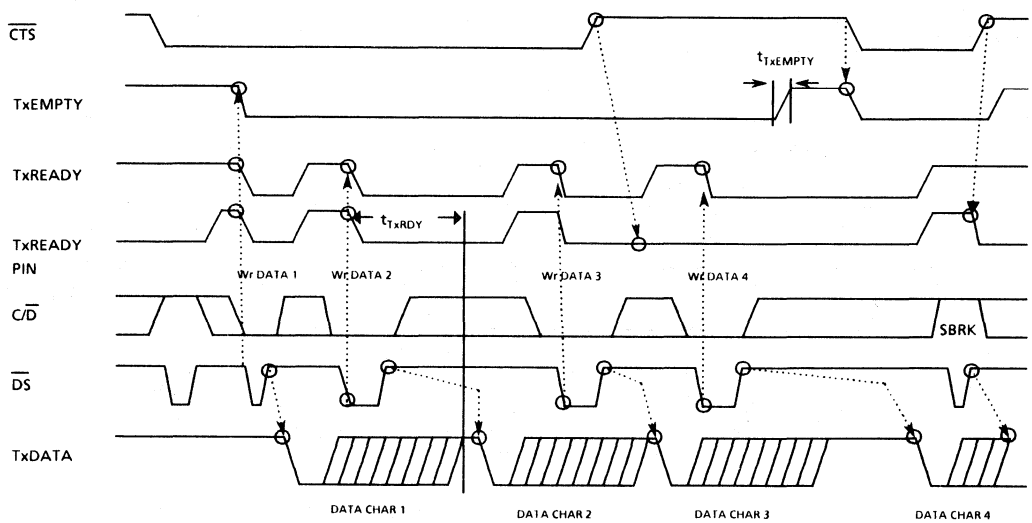

EXAMPLE FORMAT = 7 BIT CHARACTER WITH PARITY AND 2 STOP BITS.

Figure 21: Transmitter Control and Flag Timing (ASYNC Mode)

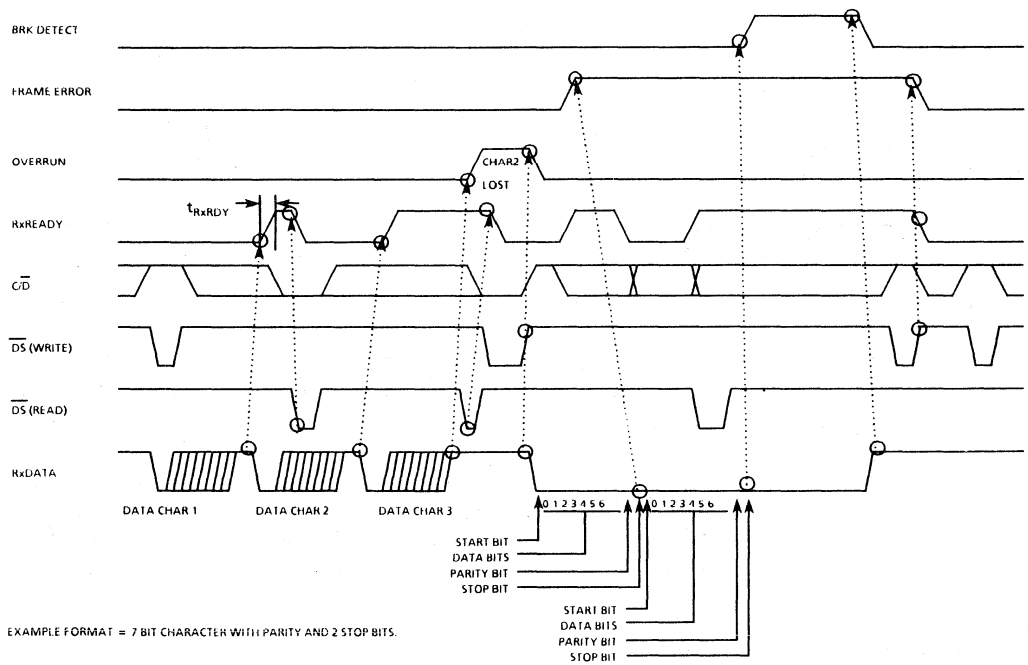

Figure 22: Receiver Control and Flag Timing (ASYNC Mode)

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DC Characteristics and Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0 5	10	V
V_I	Input voltage	-0.3	V_{DD} + 0.3	V
-	Current through any pin	-20	+ 20	mA
T_A	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Figure 23: Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

Symbol	Parameter	Conditions	Total dose radiation not exceeding $3x10^5$ Rad (Si)			Total dose ≤1 MRad (Si)		Units
			Min.	Typ.	Max.	Min.	Max.	
V_{DD}	Supply voltage	-	4.5	5.0	5.5	4 5	5.5	V
V_{IH}	Input high voltage	-	2.0	-	-	2 0	-	V
V_{IL}	Input low voltage	-	-	-	0.8	-	0.3	V
V_{OH}	Output high voltage	I_{OH} = -2mA	2.4	-	-	2.4	-	V
V_{OL}	Output low voltage	I_{OL} = 5mA	-	-	0.4	-	0.4	V
I_{IN}	Input leakage current	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-	-	± 10	-	± 100	uA
I_{OZ}	Tristate leakage current	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-	-	± 50	-	± 100	uA
I_{DD}	Power supply current	Static, V_{DD} = 5.5V	-	0.1	10	-	10	mA

V_{DD} = 5V ± 10%, over full operating temperature range.

Figure 24: Operating Electrical Characteristics

AC Electrical Characteristics

Symbol	Parameter	Min.	Max.	Units	Condition
t_{CY}	Clock reset	200	1000	nS	Notes 1,5,6.
t_0	Clock high pulse width	120	-	nS	-
$\overline{t_0}$	Clock low pulse width	120	-	nS	-
t_R, t_F	Clock rise and fall time	-	20	nS	-
t_{DTX}	TxD delay from falling edge of TxD	-	1	uS	-
f_{Tx}	Transmitter input clock frequency	DC DC DC	64 310 615	kHz kHz kHz	1x baud rate 16x baud rate 64x baud rate
t_{TPW}	Transmitter input clock pulse width	$12xt_{CY}$ $1xt_{CY}$	- -	- -	1x baud rate 16x and 64x baud rate
t_{TPD}	Transmitter input clock pulse delay	$15xt_{CY}$ $3xt_{CY}$	- -	- -	1x baud rate 16x and 64x baud rate
f_{Rx}	Receiver input clock frequency	DC DC DC	64 310 615	kHz kHz kHz	1x baud rate 16x baud rate 64x baud rate
t_{RPW}	Receiver input clock pulse width	$12xt_{CY}$ $1xt_{CY}$	- -	- -	1x baud rate 16x and 64x baud rate
t_{RPD}	Receiver input clock pulse delay	$15xt_{CY}$ $3xt_{CY}$	- -	- -	1x baud rate 16x and 64x baud rate
t_{TxRDY}	TxRDY pin delay from CENTER of last bit	-	$8xt_{CY}$	-	Note 7
$t_{TxRDY\ CLEAR}$	TxRDY fall from leading edge of WRITE	-	400	-	Note 7
t_{RxRDY}	RxRDY pin delay from center of last bit	-	$26xt_{CY}$	-	Note 7
$t_{RxRDY\ CLEAR}$	RxRDY fall from leading edge of READ	-	400	-	Note 7
$t_{TxEMPTY}$	TxEMPTY from centre of last bit	$20xt_{CY}$	-	-	Note 7
t_{WC}	Control delay from rising edge of WRITE	$8xt_{CY}$	-	-	Note 7
t_{CR}	Control to READ set-up time ($\overline{DSR}$,$\overline{CTS}$)	$20xt_{CY}$	-	-	Note 7
t_{AR}	Address stable before $\overline{DS}$ ($\overline{CS}$, C/$\overline{D}$)	0	-	ns	Note 2
t_{RA}	Address hold time before $\overline{DS}$ ($\overline{CS}$, C/$\overline{D}$)	0	-	ns	Note 2
t_{RR}	$\overline{DS}$ pulse width	50	-	ns	-
t_{RD}	Data delay from $\overline{DS}$ (READ)	-	200	ns	Note 3
t_{DF}	$\overline{DS}$ to data floating (READ)	10	100	ns	Note 8
t_{DW}	Data set-up time to $\overline{DS}$ (WRITE)	150	-	ns	-
t_{WD}	Data hold time to $\overline{DS}$ (WRITE)	20	-	ns	-
t_{RV}	Recovery time between writes (not shown)	$6x\ t_{CY}$	-	-	Note 4

NOTES: 1. AC Timings measured $V_{OH} = 1.5$ $V_{OL} = 1.5$
2. $\overline{CS}$ and Command/Data are considered as addresses
3. Assumes that address is valid before $\overline{DS}$ goes low
4. This recovery time is for Mode Initialisation only. Write data is allowed when TxRDY = 1. Recovery time between writes for Asynchronous Mode is $8xt_{CY}$ and for Synchronous Mode is $16xt_{CY}$.
5. The $\overline{TxC}$ and $\overline{RxC}$ frequencies have the following limitation with respect to clock: For 1xBaud rate, f_{1x} or $f_{RX} \leq 1/(30t_{CY})$: For 16x and 64x Baud rate, f_{Tx} or $f_{RX} \leq 1/(4.5t_{CY})$.
6. Reset Pulse Width = $6t_{CY}$ minimum; System clock must be running during Reset.
7. Status update can have a maximum delay of 28 clock periods from the event affecting the status.
8. Data Bus connected to V_{DD} via loads of 680Ω (minimum).

Figure 25: AC Electrical Characteristics

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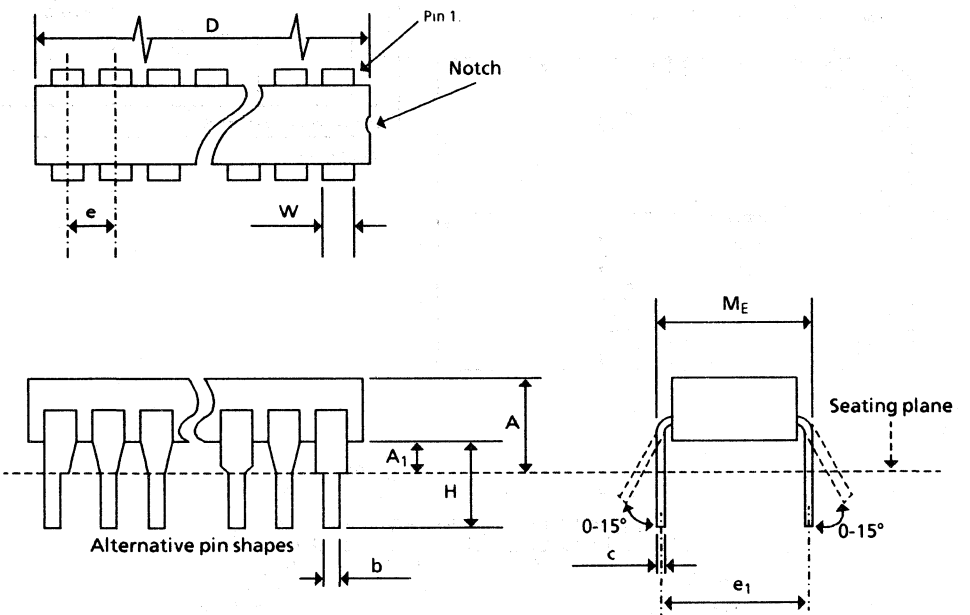
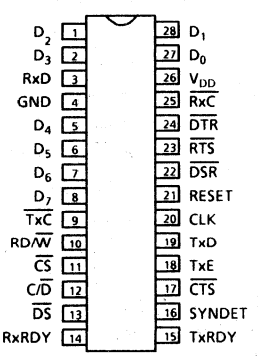
Radiation Hard Programmable Communication Interface

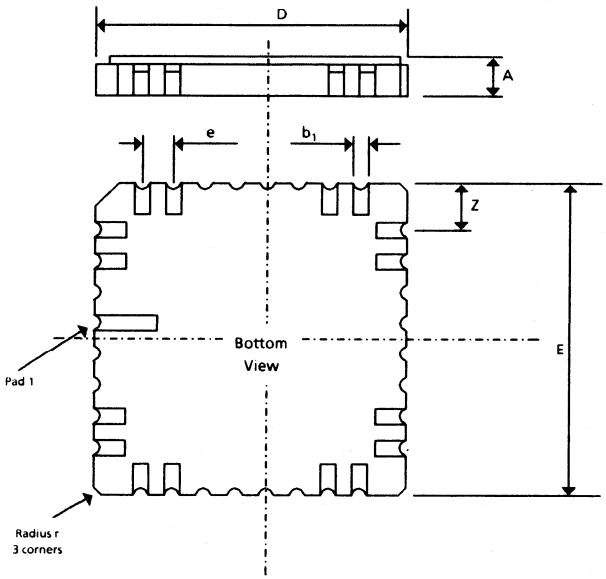
Outlines and Pin Assignments





Ref.	Min.	Nom.	Max.
A	-	-	5.60 (0.220)
A_1	0.38 (0.015)	-	1.53 (0.060)
b	0.35 (0.014)	-	0.59 (0.023)
c	0.20 (0.008)	-	0.36 (0.014)
D	-	-	36.02 (1.418)
e	-	2.54(0.100) typ.	-
e_1	-	15.24(0.600) typ.	-
H	4.71 (0.185)	-	5.38 (0.212)
M_E	-	-	15.90 (0.626)
Z	-	-	1.27 (0.050)
W	-	-	1.53 (0.060)
Dimensions in mm (inches)			

Figure 26. 28-Lead Ceramic DIL (solder seal) - package style C



Ref.	Min.	Nom.	Max.
A			2.16 (0.085)
b_1		0.51 (0.020)	
D			14.60 (0.575)
E			14.60 (0.575)
e		1.02 (0.040)	
Z		1.52 (0.065) typ.	

Dimensions in mm (inches)

MEDL XG431

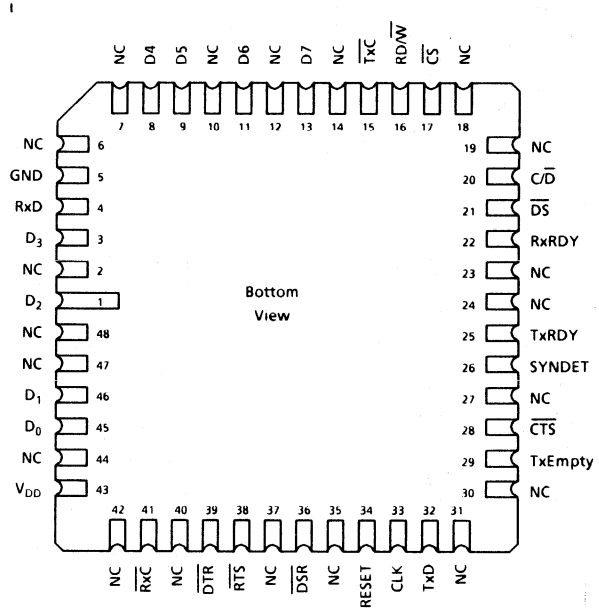


Figure 27: 48-pad Leadless Chip Carrier (Package style L)

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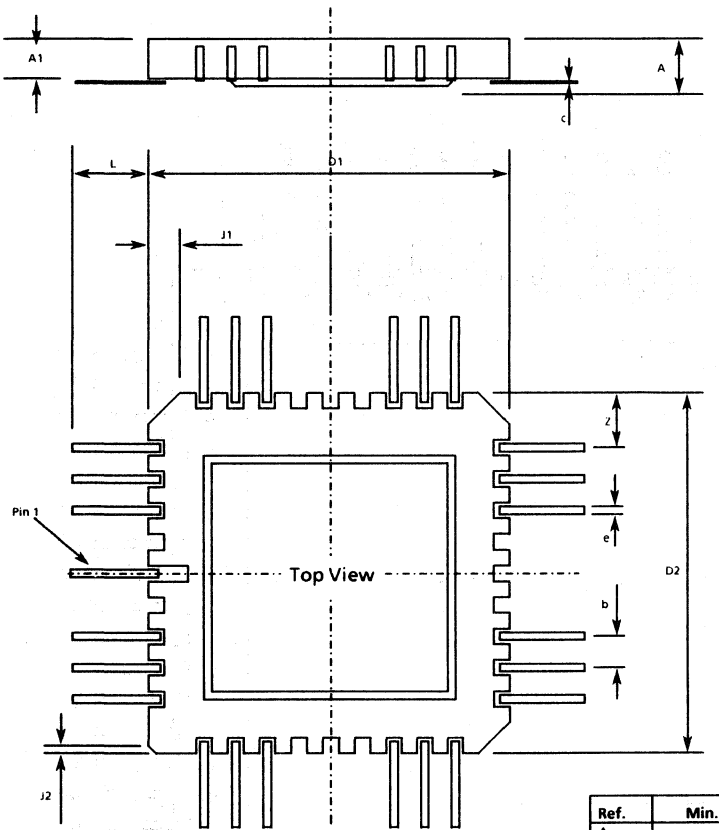
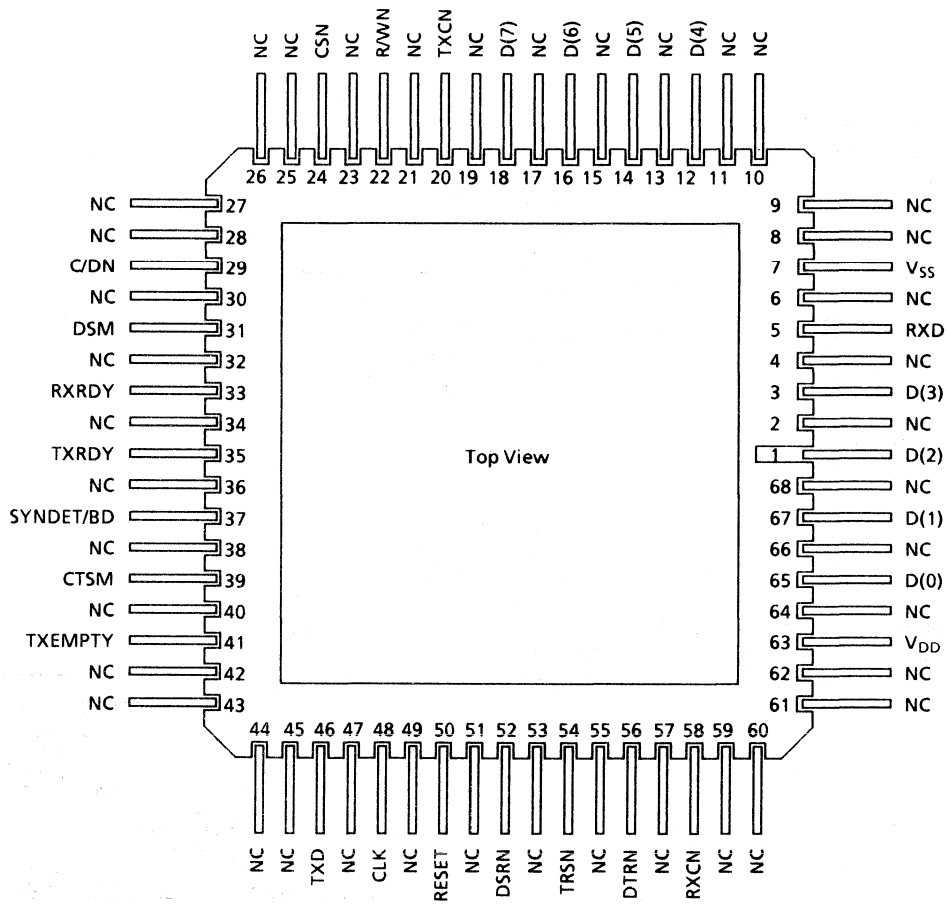


Ref.	Min.	Nom.	Max.
A			2.59 (0.102)
A_1	1.83 (0.072)		2.24 (0.088)
b	0.25 (0.010)		0.36 (0.014)
c	0.10 (0.004)		0.20 (0.008)
D1 D2	23.88 (0.940)		24.51 (0.965)
e		2.54 (0.050)	
j1		1.02 (0.040)	
j2		0.51 (0.020)	
L	8.89 (0.350)		25.85 (0.445)
Z	1.65 (0.065)		2.16 (0.085)
Dimensions in mm (inches)			

MEDL XG491

Figures 28a. 68-Lead Topbraze Flatpack (Package style F)



Figures 28b. 68-Lead Topbraze Flatpack (Package style F)

RadiationTolerance

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

Total Dose (Function to specification)	$3x10^5$ Rad(Si)
Transient Upset (survivability)	$>10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$1x10^{15}$ neutrons/cm^2
Single Event Upset (GSO 10% worst case)	$<10^{-10}$ errors/bitday
Latch-up	Not possible

Figure 29: Radiation Hardness Parameters

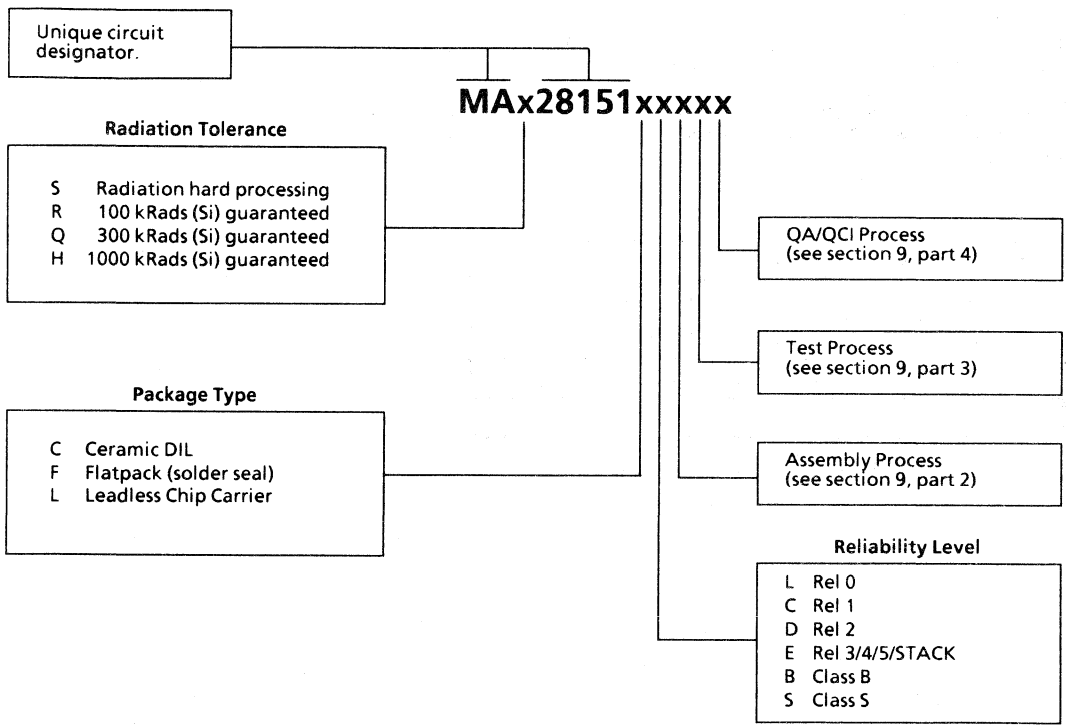
MA28151

Radiation Hard Programmable Communication Interface

GEC PLESSEY
SEMICONDUCTORS

Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



GEC PLESSEY

SEMICONDUCTORS

S10205FDS Issue 2 September 1990

MA28155

Radiation Hard Programmable Peripheral Interface

Features

- **Radiation Hard to 1 MRad (Si)**
- **High SEU immunity, latch up free**
- **Silicon-on-Sapphire technology**
- **24 Programmable I/O Pins**
- **All inputs & outputs are TTL Compatible**
- **Direct Bit Set/Reset Capability Easing Control application Interface**
- **Reduces System Package Count**
- **Compatible with MAS281 (Mil Std 1750A) microprocessor**

General Description

The MA28155 is a general purpose programmable Input/Output device designed for use with the MAS281 microprocessor. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation.

In the first mode (MODE 0), each group of 12 I /O pins may be programmed in sets of 4 to be inputs or outputs. In the second mode (MODE 1), each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for hand-shaking and interrupt control signals. The third mode of operation (MODE 2) is the bidirectional bus mode, which uses 8 lines for a bidirectional bus and 5 lines, borrowing one from the other group, for hand-shaking.

3

Block Diagram

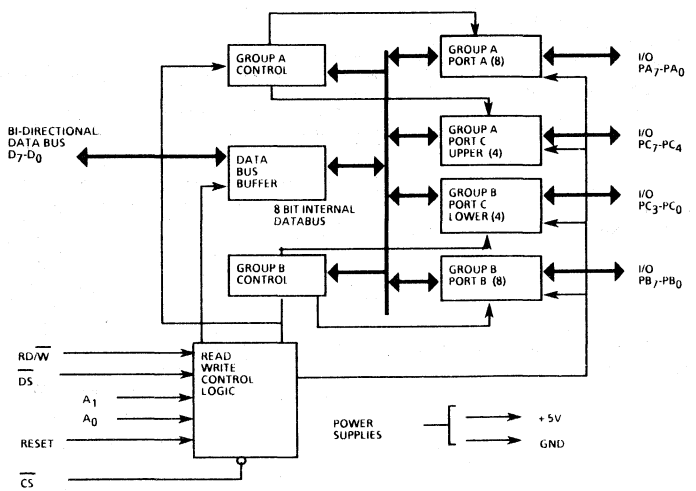


Figure 1. Block Diagram

MA28155

Radiation Hard Programmable Peripheral Interface

GEC PLESSEY

SEMICONDUCTORS

Functional Description

The MA28155 is a programmable peripheral interface (PPI) device designed for use with MAS281. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the MA28155 is programmed by the system software so that, normally, no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the MA28155 to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

Reset (RESET)

A high on this input clears the control register and all ports (A,B,C) are set to the input mode.

Chip Select ($\overline{CS}$)

A low on this input pin enables the communication between the MA28155 and the CPU.

Read/Write Select (RD/$\overline{W}$)

A high on RD/$\overline{W}$ indicates a CPU read from the MA28155 and a low indicates a CPU data or control word write to the MA28155. The RD/$\overline{W}$ line is active only when $\overline{DS}$ is low.

Data Strobe ($\overline{DS}$)

This input indicates that a data transfer is taking place. During a CPU write operation the MA28155 reads data from the bus on the rising edge of $\overline{DS}$. During a read operation the MA28155 outputs data to the bus while $\overline{DS}$ is low. Data is valid on the rising edge of $\overline{DS}$.

Port Select 0 and Port Select 1 (A0 and A1)

These input signals, in conjunction with the $\overline{DS}$ and RD/$\overline{W}$ inputs, control the selection of one of the three ports of the control word registers. They are normally connected to the least significant bits of the address bus.

Basic Operation

A1	A0	$\overline{DS}$	RD/$\overline{W}$	$\overline{CS}$	READ
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS
					WRITE
0	0	0	0	0	DATA BUS → PORT A
0	1	0	0	0	DATA BUS → PORT B
1	0	0	0	0	DATA BUS → PORT C
1	1	0	0	0	DATA BUS → CONTROL
					DISABLE
x	x	x	x	1	DATA BUS → TRI-STATE
1	1	0	1	0	ILLEGAL CONDITION
x	x	1	x	0	DATA BUS → TRI-STATE

Table 1. Basic Operation

MA28155

Radiation Hard Programmable Peripheral Interface

Operational Description

Mode Selection

There are three basic modes of operation, which can be selected by the system software:

Mode 0. Basic Input/Output
Mode 1. Strobed Input/Output
Mode 2. Bi-directional Bus

When the reset input goes high all ports will be set to the input mode (i.e. all 24 lines will be in the high impedance state). After the reset is removed the MA28155 can remain in the input mode with no additional initialisation required.

During the execution of the system program any of the other modes may be selected using a single output instruction. This allows a single MA28155 to service a variety of peripheral devices with a single software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed.

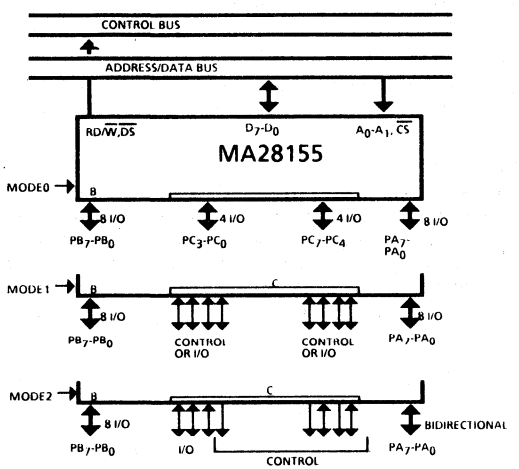


Figure 2. Basic Mode Definitions and Bus Interface

Modes may be combined so that their functional definition can be tailored to almost any I/O structure. For instance; Group B can be programmed in Mode O to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

The design of the MA28155 has taken into account things such as efficient PC board layout, control signal definition verses PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the optimum use of available pins.

Mode Definition Format ($D_7 = 1$)

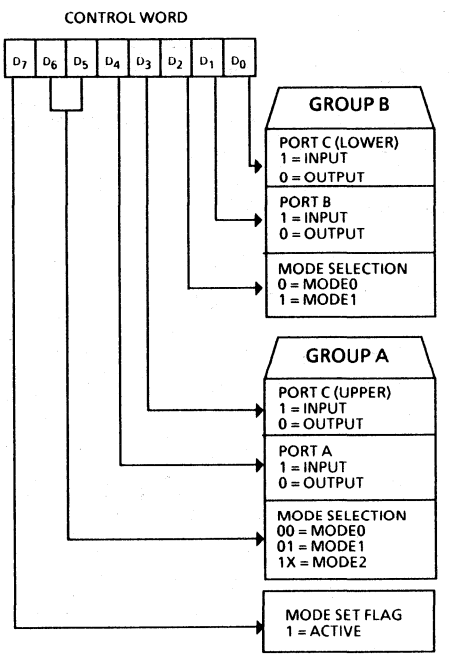


Figure 3. Mode Definition Format ($D_7 = 1$)

Radiation Hard Programmable Peripheral Interface

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single output instruction. This feature reduces software requirements in control-based applications.

When Port C is being used as Status/Control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the MA28155 is programmed to operate in Mode 1 or 2, control signals are provided that can be used as interrupt request inputs to the CPU (figure 4). The interrupt request signals, generated from Port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the Bit Set/Reset function of Port C.

This function allows the programmer to disallow or allow a specific I/O device to interrupt the CPU, without affecting any other device in the interrupt structure.

INTE flip-flop definitions:
(BIT-SET): INTE is SET -Interrupt enable
(BIT-RESET): INTE is RESET -Interrupt disable

Note: All mask flip-flops are automatically reset during mode selection and device reset.

Bit Set/Reset Format ($D_7 = 0$)

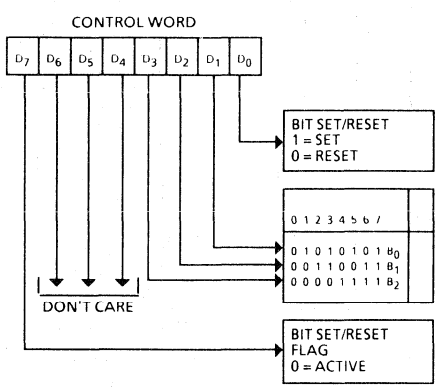


Figure 4. Bit Set/Reset Format ($D_7 = 0$)

Group A and Group B Controls

The functional configuration of each port is programmed by the system software. In essence, the CPU outputs a control word to the MA28155. The control word contains information such as mode, bit set, bit reset, etc., this initializes the functional configuration of the MA28155.

Each of the Control blocks (Group A and Group B) accept commands from the Read/Write Control Logic, receive control words from the internal data bus and issue the proper commands to its associated ports:

Control Group A - Port A and Port C upper (C_7-C_4)
Control Group B - Port B and Port C lower (C_3-C_O)

The Control Word Register can only be written into. Therefore reading of the Control Word Register is not allowed.

Ports A, B and C

The MA28155 contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or personality to further enhance the power and flexibility of the MA28155.

Port A.
One 8-bit data output latch/buffer and one 8-bit data input latch.

Port B.
One 8-bit data input/output latch/buffer and one 8-bit input buffer.

Port C.
One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

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Radiation Hard Programmable Peripheral Interface

Operating Mode 0 (Basic Input/Output)

This functional configuration provides simple input and output operation for each of the three ports. No handshaking is required; data is simply written to or read from a specified port.

- Two 8-bit ports and 4-bit ports.
- Any port can be input or output .
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.

Basic Input (read)

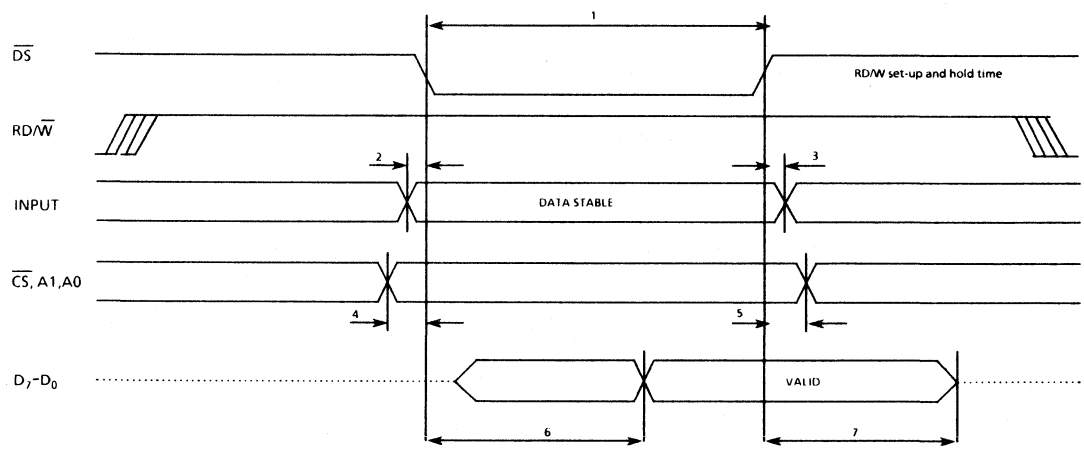


Figure 5. Basic Input (read) timing Diagram

Basic Input (write)

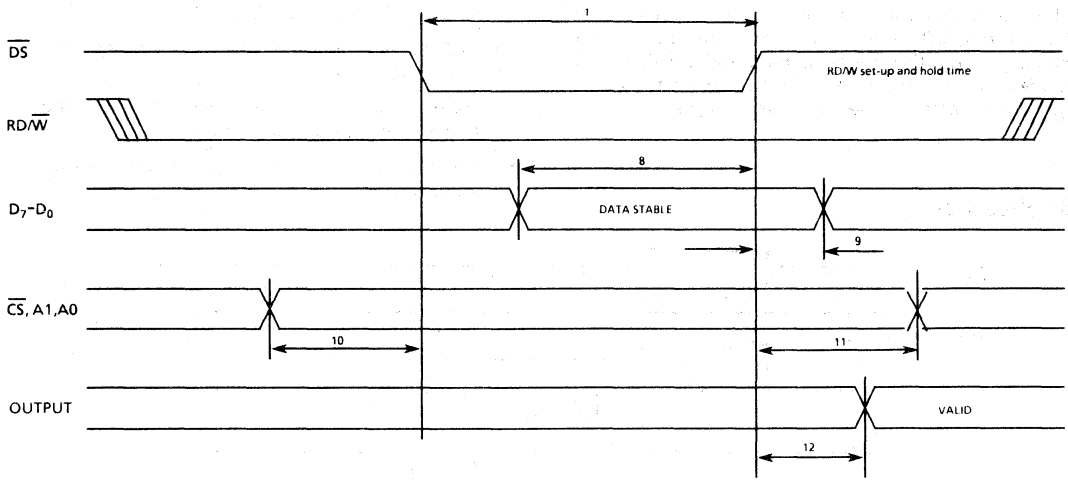


Figure 6. Basic Input (write) Timing Diagram

Port Definition Mode 0

D_4	D_3	D_1	D_0	PORT A	PORT C (UPPER)		PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

Table 2. Port Definition Mode 0 (see also figure 3)

Radiation Hard Programmable Peripheral Interface

Operating Mode 1 (Strobed Input/Output)

This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or handshaking signals. In mode 1, port A and port B use the lines on port C to generate or accept these handshaking signals.

- Two Groups (Group A and Group B) .
- Each Group contains one 8-bit data port and one 4-Bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Strobed Input

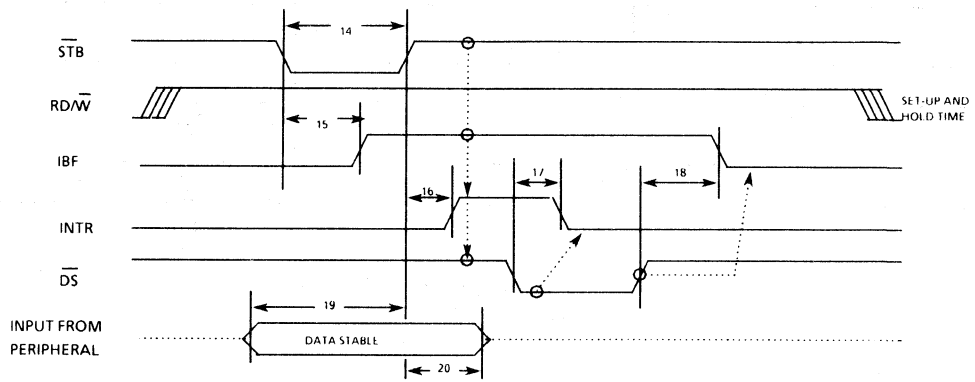


Figure 7. Strobed Input Timing Diagram

Strobed Output

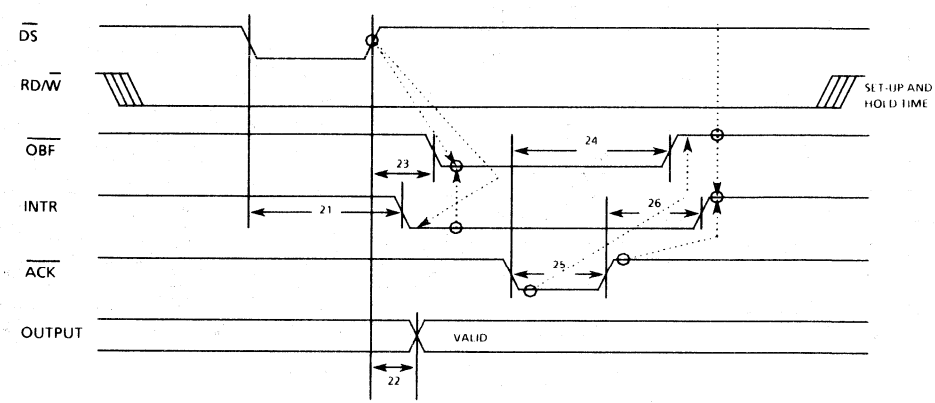


Figure 8. Strobed Output Timing Diagarm

MA28155

Radiation Hard Programmable Peripheral Interface

Input Control Signal Definition (Mode 1)

STB (Strobe Input).
A low on this input loads data into the input latch.

IBF (Input Buffer Full F/F).
A high on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement.

IBF is set by the STB input being low and is reset by the rising edge of DS input.

INTR (Interrupt Request).
A high on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the STB being high and IBF being high and INTE being enabled. It is reset by the falling edge of $\overline{DS}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A: Controlled by bit set/reset of PC_4

INTE B: Controlled by bit set/reset of PC_2

Strobed Input

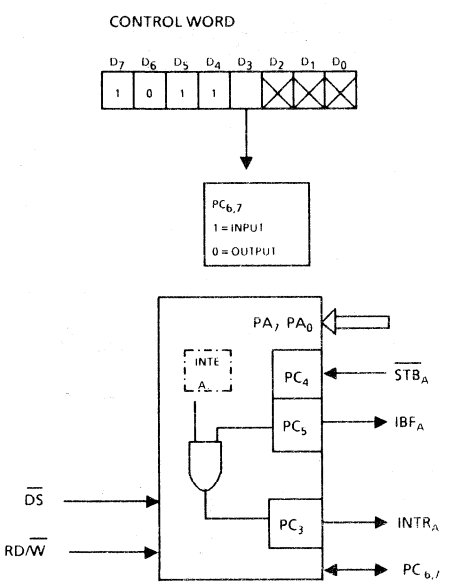


Figure 9. Strobed Input (PORT A)

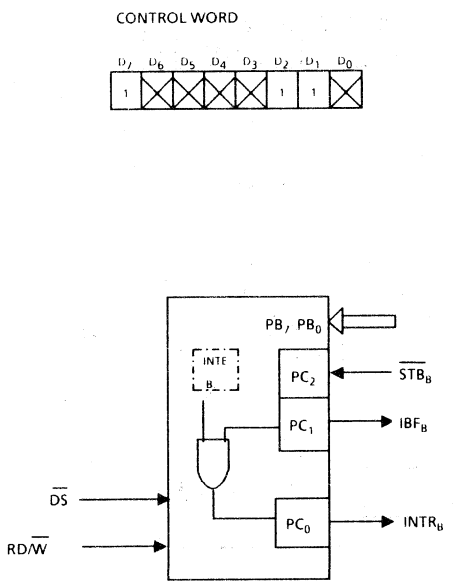


Figure 10. Strobed Input (PORT B)

Output Control Signal Definition (Mode 1)

$\overline{OBF}$ (Output Buffer Full Flip-Flop).
The $\overline{OBF}$ output will go low to indicate that the CPU has written data out to the specified port. The OBF flip-flop will be set by the rising edge of the $\overline{DS}$ input and reset by $\overline{ACK}$ input being low.

$\overline{ACK}$ (Acknowledge Input).
A low on this input informs the 28155 that the data from port A or port B has been accepted; in essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request).
A high on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is high, $\overline{OBF}$ is high and INTE is high. It is reset by the falling edge of $\overline{DS}$.

INTE A: Controlled by bit set/reset of PC_6
INTE B: Controlled by bit set/reset of PC_2

Strobed Output

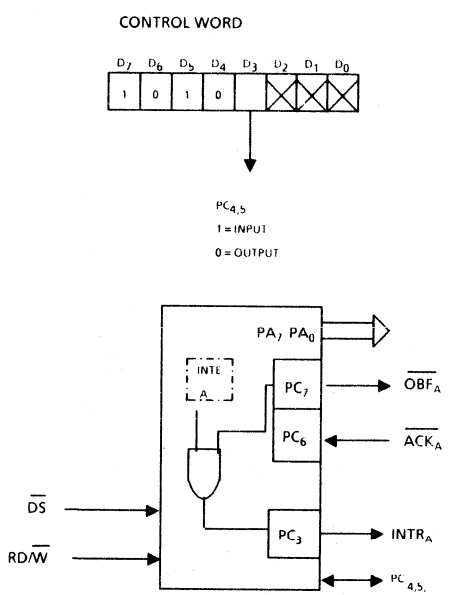


Figure 11. Strobed Output (PORT A)

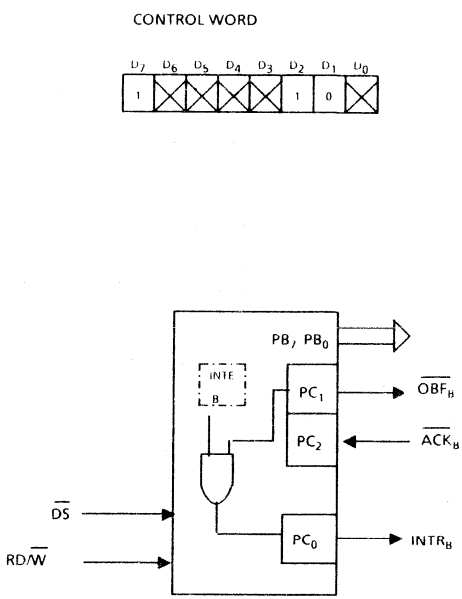


Figure 12. Strobed Output (PORT B)

Combinations of Mode 1

Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

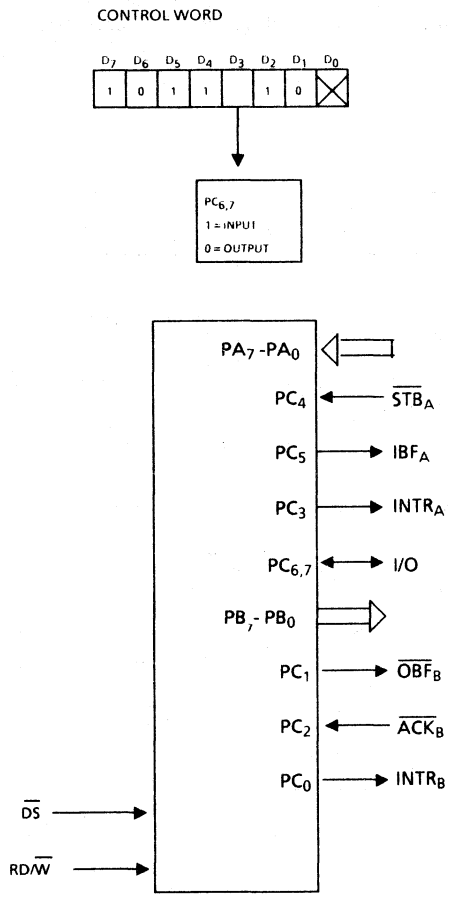


Figure 13. PORT A-(STROBED INPUT) PORT B-(STROBED OUTPUT)

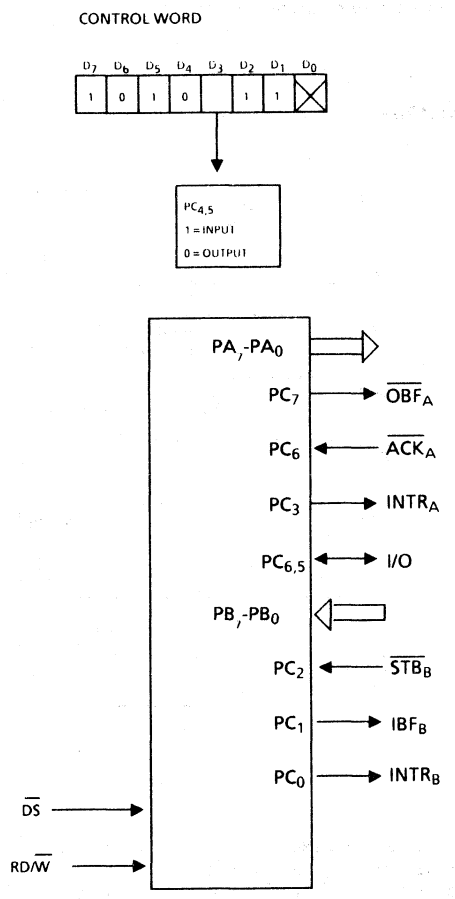


Figure 14. PORT A-(STROBED OUTPUT) PORT B-(STROBED INPUT)

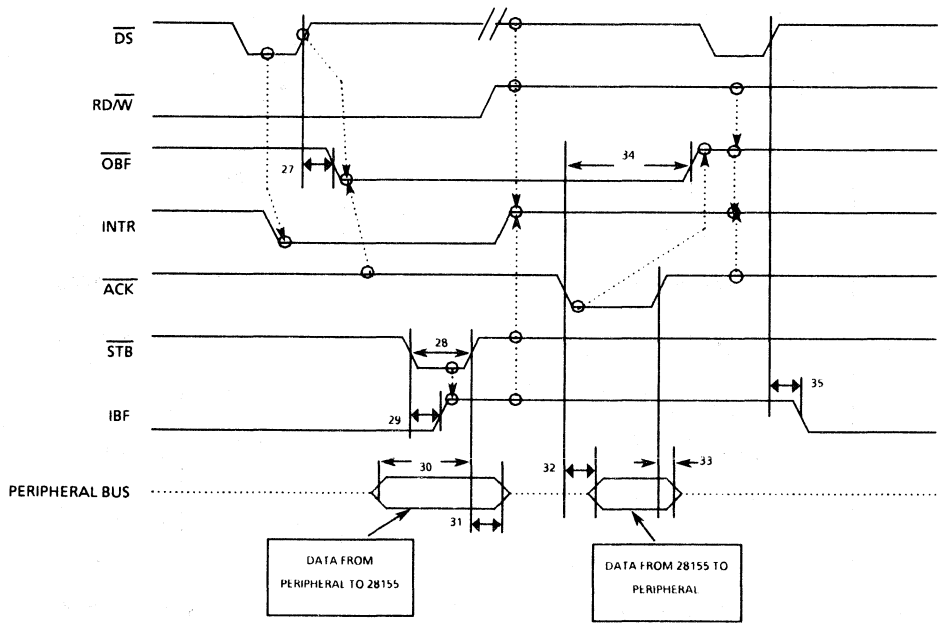
Radiation Hard Programmable Peripheral Interface

Operating Mode 2 (Strobed Bidirectional Bus I/O)

This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O) . Handshaking signals are provided to maintain proper bus flow discipline in a similar manner to Mode 1. Interrupt generation and enable/disable functions are also available.

- Used in group A only.
- One 8-bit bidirectional bus port (port A) and 5-bit control port (port C).
- Both inputs and outputs are latched.
- The 5-bit control port (port C) is used for control and status of the 8-bit bidirectional bus port (port A).

Bidirectional



NOTE: Any sequence where RD/W = 0 coincident with DS low occurs before ACK and STB occurs before RD/W = 1 coincident with DS is permissable
(INTR = IBF.MASK.STB.(RD/W = 1.DS = 0) + OBF.MASK.ACK.(RD/W = 0.DS = 0))

Figure 15. Bidirectional Timing Diagram

Bidirectional Bus I/O Control Signal Definition (Mode 2)

INTR (Interrupt Request):
A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Full):
The $\overline{OBF}$ output will go low to indicate that the CPU has written data out to port A.

$\overline{ACK}$ (Acknowledge):
A low on this input enables the tri-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (INTE flip-flop associated with $\overline{OBF}$):
Controlled by Bit Set/Reset of PC_6.

Input Operations

$\overline{STB}$ (Strobe input):
A low on this input loads data in to the input latch.

IBF (Input Buffer Full Flip-Flop):
A high on this output indicates data has been loaded in to the input latch.

INTE 2 (The INTE flip-flop associated with IBF). Controlled by Bit Set/Reset of PC_4.

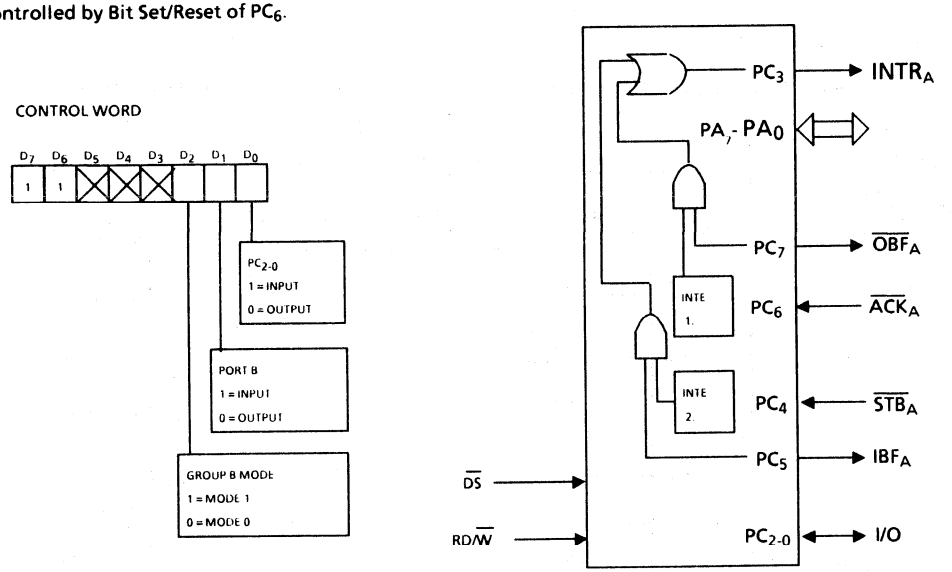


Figure 16. Mode 2 Bidirectional

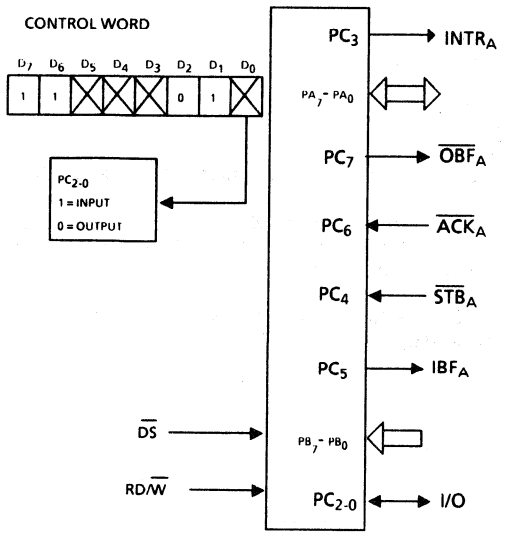


Figure 17a. Mode 2 and Mode 0 (input)

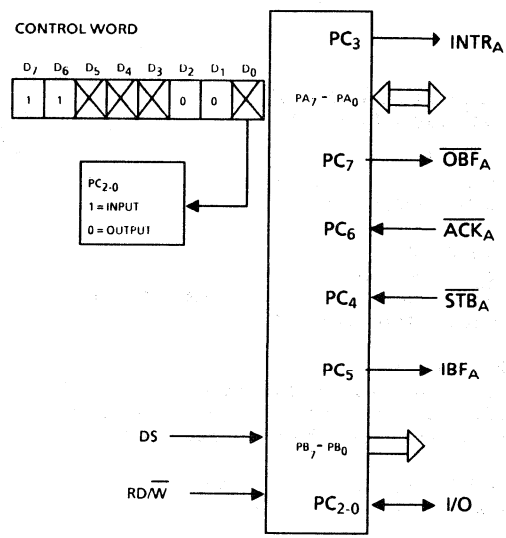


Figure 17b. Mode 2 and Mode 0 (output)

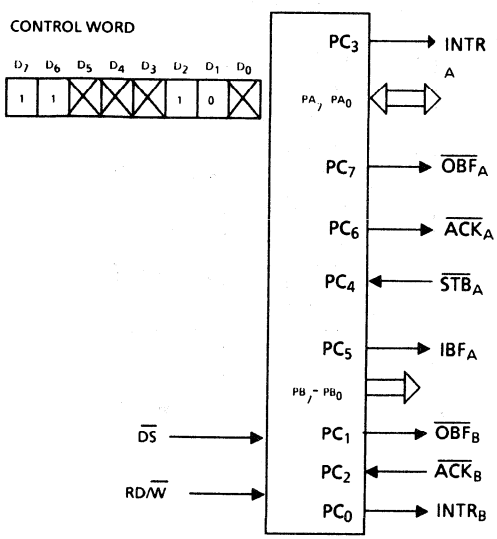


Figure 17c. Mode 2 and Mode 1 (output)

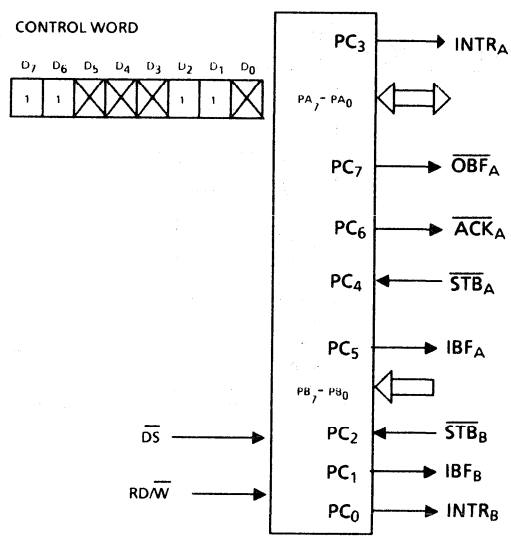


Figure 17d. Mode 2 and Mode 1 (input)

MA28155

Radiation Hard Programmable Peripheral Interface

Mode Definition Summary

	MODE 0		MODE 1		MODE 2
	IN	OUT	IN	OUT	
PA_0	IN	OUT	IN	OUT	⇐⇒
PA_1	IN	OUT	IN	OUT	⇐⇒
PA_2	IN	OUT	IN	OUT	⇐⇒
PA_3	IN	OUT	IN	OUT	⇐⇒
PA_4	IN	OUT	IN	OUT	⇐⇒
PA_5	IN	OUT	IN	OUT	⇐⇒
PA_6	IN	OUT	IN	OUT	⇐⇒
PA_7	IN	OUT	IN	OUT	⇐⇒
PB_0	IN	OUT	IN	OUT	–
PB_1	IN	OUT	IN	OUT	–
PB_2	IN	OUT	IN	OUT	–
PB_3	IN	OUT	IN	OUT	–
PB_4	IN	OUT	IN	OUT	–
PB_5	IN	OUT	IN	OUT	–
PB_6	IN	OUT	IN	OUT	–
PB_7	IN	OUT	IN	OUT	–
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$
PC_5	IN	OUT	IBF_A	I/O	IBF_A
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$

Table 3. Mode Definition Summary

Special Mode Combination Considerations.

There are several combinations of modes when not all of the bits in port C are used for control or status. The remaining bits can be used as follows:

If programmmed as inputs -

All input lines can be accessed during normal port C read

If programmed as outputs-

Bits in C upper (PC_7-PC_4) must be individually accessed using a bit set/reset function.

Bits in C lower (PC_3-PC_0) can be accessed using the bit set/reset function or bits PC_2-PC_0 may also be accessed as a trio by writing into port C.

Reading Port C Status.

In Mode 0 Port C transfers data from or to the peripheral device. When the MA28155 is programmed to function in Modes 1 or 2 Port C generates or accepts handshaking signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the status of each peripheral device and change the program flow accordingly.

There is no special instruction to read the Status Information from Port C. A normal read operation of Port C is executed to perform this function.

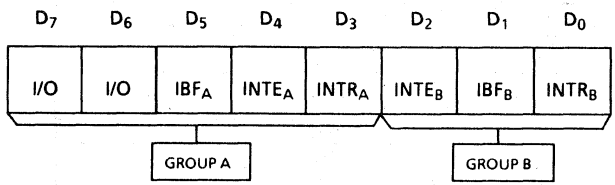


Figure 18a. Mode 1 Input Configuration

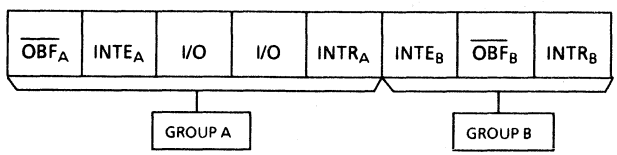


Figure 18b. Mode 1 Ouput Configuration

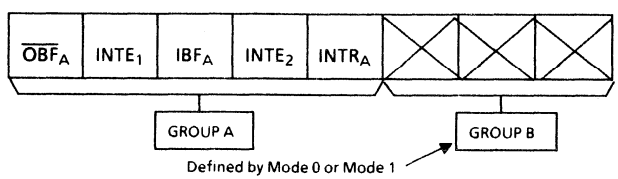


Figure 18c. Mode 2

MA28155

Radiation Hard Programmable Peripheral Interface

DC Characteristics and Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0.5	10	V
V_I	Input voltage	-0.3	V_{DD} + 0.3	V
-	Current through any pin	-20	+ 20	mA
T_A	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Table 4: Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

Symbol	Parameter	Conditions	Total dose radiation not exceeding $3x10^5$ Rad (Si)			Total dose ≤1 MRad (Si)		Units
			Min.	Typ.	Max.	Min.	Max.	
V_{DD}	Supply voltage	-	4.5	5.0	5.5	4.5	5.5	V
V_{IH}	Input high voltage	-	2.0	-	-	2.0	-	V
V_{IL}	Input low voltage	-	-	-	0.8	-	0.3	V
V_{OH}	Output high voltage	I_{OH} = -6mA	2.4	-	-	2.4	-	V
V_{OL}	Output low voltage	I_{OL} = 12.0mA	-	-	0.5	-	0.5	V
I_{IN}	Input leakage current	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-	-	± 10	-	± 100	uA
I_{OZ}	Tristate leakage current	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-	-	± 50	-	± 100	uA
I_{DD}	Power supply current	Static, V_{DD} = 5.5V	-	0.1	5	-	10	mA

V_{DD} = 5V ± 10%, over full operating temperature range.

Table 5: Operating Electrical Characteristics

Radiation Hard Programmable Peripheral Interface

AC Electrical Characteristics

	Parameter	Min.	Max.	Units		Parameter	Min.	Max.	Units
					18	$\overline{DS}$ ↑ to IBF ↓	-	65	ns
					19	Peripheral Data set up to $\overline{STB}$ ↑	0	-	ns
1	$\overline{DS}$ width	65	-	ns	20	Peripheral Data hold after $\overline{STB}$ ↑	100	-	ns
2	Peripheral Data set up to $\overline{DS}$	0	-	ns	21	$\overline{DS}$ ↓ to INTR ↓ (note 4)	-	DS + 100	ns
3	Peripheral Data hold after $\overline{DS}$	10	-	ns	22	Output valid from $\overline{DS}$ ↑	-	100	ns
4	$\overline{CS}$, A1,A0 setup to $\overline{DS}$ ↓	0	-	ns	23	$\overline{DS}$ ↑ to $\overline{OBF}$ ↓	-	105	ns
5	$\overline{CS}$, A1,A0 hold after $\overline{DS}$ ↑	0	-	ns	24	$\overline{ACK}$ ↓ to $\overline{OBF}$ ↑	-	50	ns
6	Data valid from $\overline{DS}$ ↓	-	60	ns	25	$\overline{ACK}$ pulse width	100	-	ns
7	Data float from $\overline{DS}$ ↑ (note 5)	10	100	ns	26	$\overline{ACK}$ ↑ INTR ↑	-	80	ns
8	Data set up to $\overline{DS}$ ↓	20	-	ns	27	$\overline{DS}$ ↑ to $\overline{OBF}$ ↓	-	105	ns
9	Data hold after $\overline{DS}$ ↑	30	-	ns	28	$\overline{STB}$ pulse width	100	-	ns
10	$\overline{CS}$, A1,A0 setup to $\overline{DS}$ ↓	0	-	ns	29	$\overline{STB}$ ↓ to IBF ↑	-	65	ns
11	$\overline{CS}$, A1,A0 hold after $\overline{DS}$ ↑	20	-	ns	30	Peripheral Data set up to $\overline{STB}$ ↑	0	-	ns
12	Output valid from $\overline{DS}$ ↑	-	100	ns	31	Peripheral Data hold after $\overline{STB}$ ↑	100	-	ns
14	$\overline{STB}$ pulse width	100	-	ns	32	Output valid from $\overline{ACK}$ ↓	-	45	ns
15	$\overline{STB}$ ↓ to IBF ↑	-	65	ns	33	Output float from $\overline{ACK}$ ↑ (note 5)	10	100	ns
16	$\overline{STB}$ ↑ to INTR ↑	-	65	ns	34	$\overline{ACK}$ ↓ to $\overline{OBF}$ ↑	-	50	ns
17	$\overline{DS}$ ↓ to INTR ↓	-	65	ns	35	$\overline{DS}$ ↑ to IBF ↓	-	65	ns

1. V_{DD} = 5V ± 10% and C_{Ci} = 50pF, over full operating temperature range.
2. Input Pulse V_{SS} to 3.0 Volts.
3. Times Measurement Reference Level 1.5 Volts.
4. $\overline{DS}$ = Data Strobe Pulse Width.
5. Measured by a 1.0 Volt change in output voltage. Outputs tied to V_{SS} via 680Ω.

Table 6: AC Electrical Characteristics

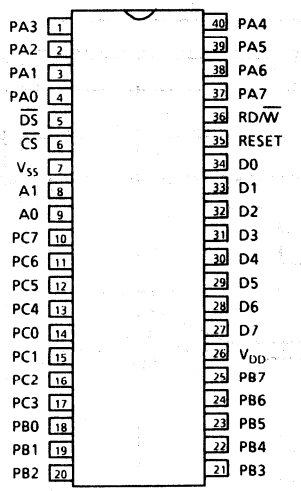
MA28155

Radiation Hard Programmable Peripheral Interface

Package Outlines and Pin Assignments

Ref.	Min.	Nom.	Max.
A			5.60 (0.220)
A_1	0.38 (0.015)		1.53 (0.060)
b	0.35 (0.014)		0.59 (0.023)
c	0.20 (0.008)		0.36 (0.014)
D			51.31 (2.020)
e		2.54 (0.100) typ	
e_1		15.24 (0.600) typ	
H	4.71 (0.185)		5.38 (0.212)
M_E			15.90 (0.626)
Dimensions in mm (inches)			

MEDL XG405



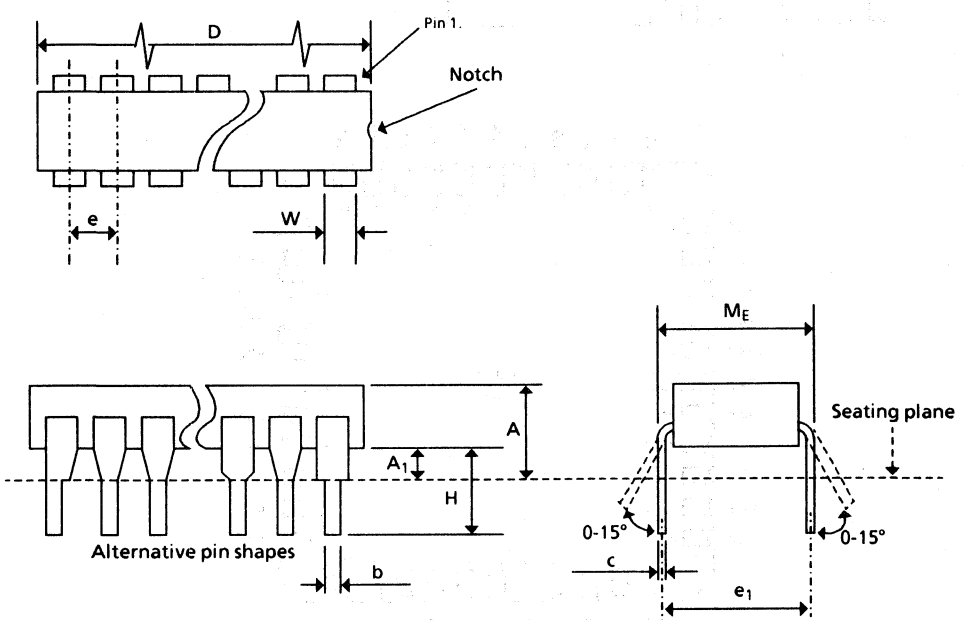
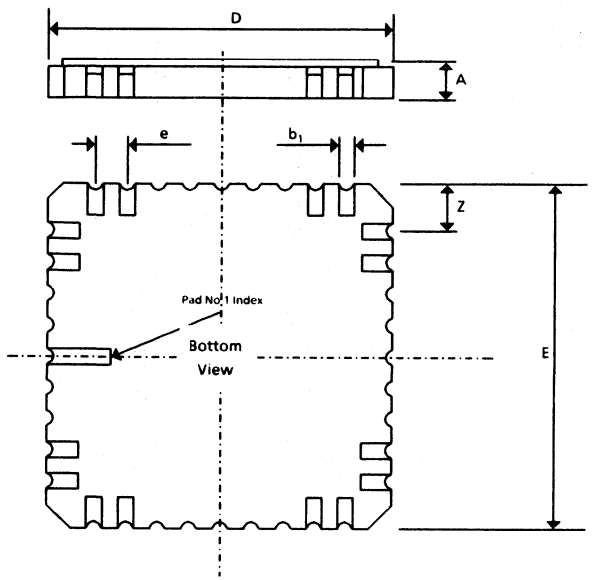


Figure 19. 40-Lead Ceramic DIL (solder seal) - package style C



Ref.	Min.	Nom.	Max.
A			2.29 (0.090)
b_1		0.64 (0.025)	
D	16.33 (0.643)		16.81 (0.662)
E	16.33 (0.643)		16.81 (0.662)
e		1.27 (0.050)	
Z		1.91 (0.075) typ.	

Dimensions in mm (inches)

MEDL XG446

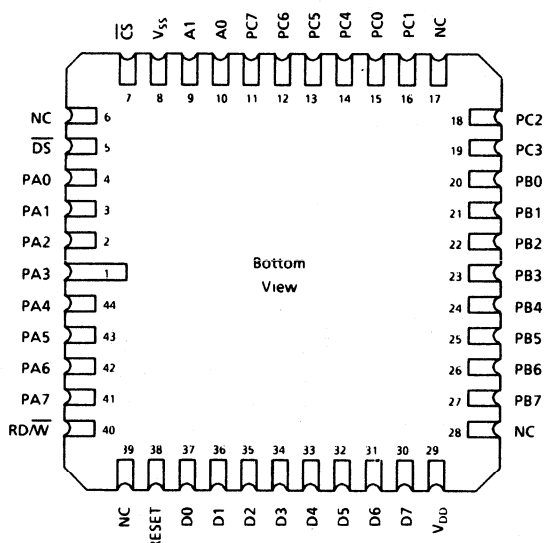


Figure 20. 44-pad Leadless Chip Carrier (Package style L)

RadiationTolerance

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

Total Dose (Function to specification)	$3x10^5$ Rad(Si)
Transient Upset (survivability)	$>10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$1x10^{15}$ neutrons/cm^2
Single Event Upset (GSO 10% worst case)	$<10^{-10}$ errors/bitday
Latch-up	Not possible

Figure 21: Radiation Hardness Parameters

Radiation Hard Programmable Peripheral Interface

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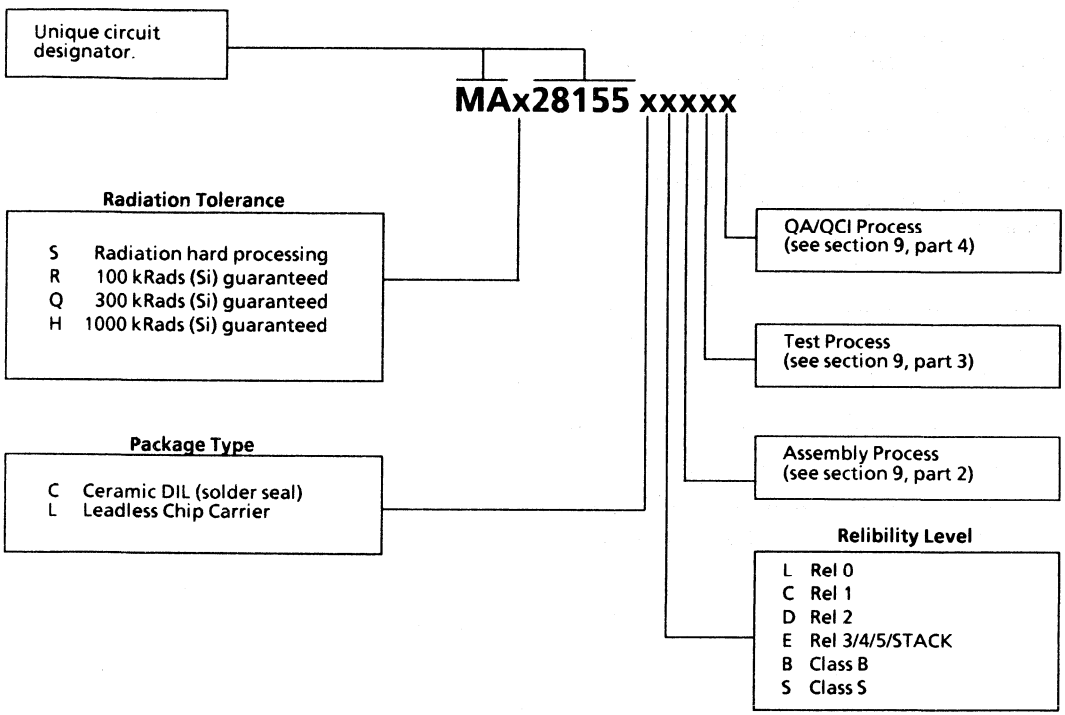
SEMICONDUCTORS

Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



section 4

BIT SLICE & ARITHMETIC CIRCUITS

GEC PLESSEY
SEMICONDUCTORS

S10604FDS Issue 1.2 October 1990

MA2901

Radiation Hard 4-Bit Microprocessor Slice

Features

- **Fully compatible with industry standard 2901**
- **CMOS SOS technology**
- **High SEU immunity and latch-up free**
- **High speed**
- **Low power**

General Description

The MA2901 is an industry standard 4-bit microprocessor slice. It provides a set of ALU functions selected by microcode data applied to the inputs. The device is cascadable to handle any word length. It can be used as a building block in the construction of microcomputers and controllers tailored to meet specialised applications.

Dual Address Architecture
Machine cycles are saved by simultaneous, independent access to two working registers.

ALU has Eight Functions
Operations performed are addition, two subtractions and five logic functions on two source operands.

Four State Flags
Zero, negative, carry and overflow.

Left / Right Shift is Independent of ALU
Only one cycle taken for add and shift operations.

Expandable
Any number of MA2901 units can be connected together to achieve longer word lengths.

Micro Programmable
Three groups, each of three bits, for ALU function, source operand and destination control.

Operation

A detailed block diagram of the bipolar micro-programmable microprocessor structure is shown in figure 1. The circuit is a four-bit slice, cascadable to any number of bits. Therefore, all data paths within the circuit are four bits wide. The two key elements in the figure 1 are the 16-word by 4-bit 2-port RAM and the high speed ALU.

Data from any of the 16 words of the Random Access Memory (RAM) can be read from the A-port of the RAM as controlled by the 4-bit A-address field input. Likewise, data from any of the 16 words of the RAM as defined by the B-address field input can be simultaneously read from the B-port of the RAM. The same code can be applied to the A-select field and B-select field in which case the identical file data will appear at both the RAM A-port and B-port outputs simultaneously.

When enabled by the RAM write enable (RAM EN), new data is always written into the file (word) defined by the B-address field of the RAM. The RAM data input field is driven by a 3-input multiplexer. This configuration is used to shift the ALU output data (F) if desired. This three-input multiplexer scheme allows the data to be shifted up one bit position, shifted down one bit position, or not shifted in either direction.

The RAM A-port data outputs and RAM B-port data outputs drive separate 4-bit latches. These latches hold the RAM data while the clock input is LOW. This eliminates any possible race conditions that could occur while new data is being written into the RAM.

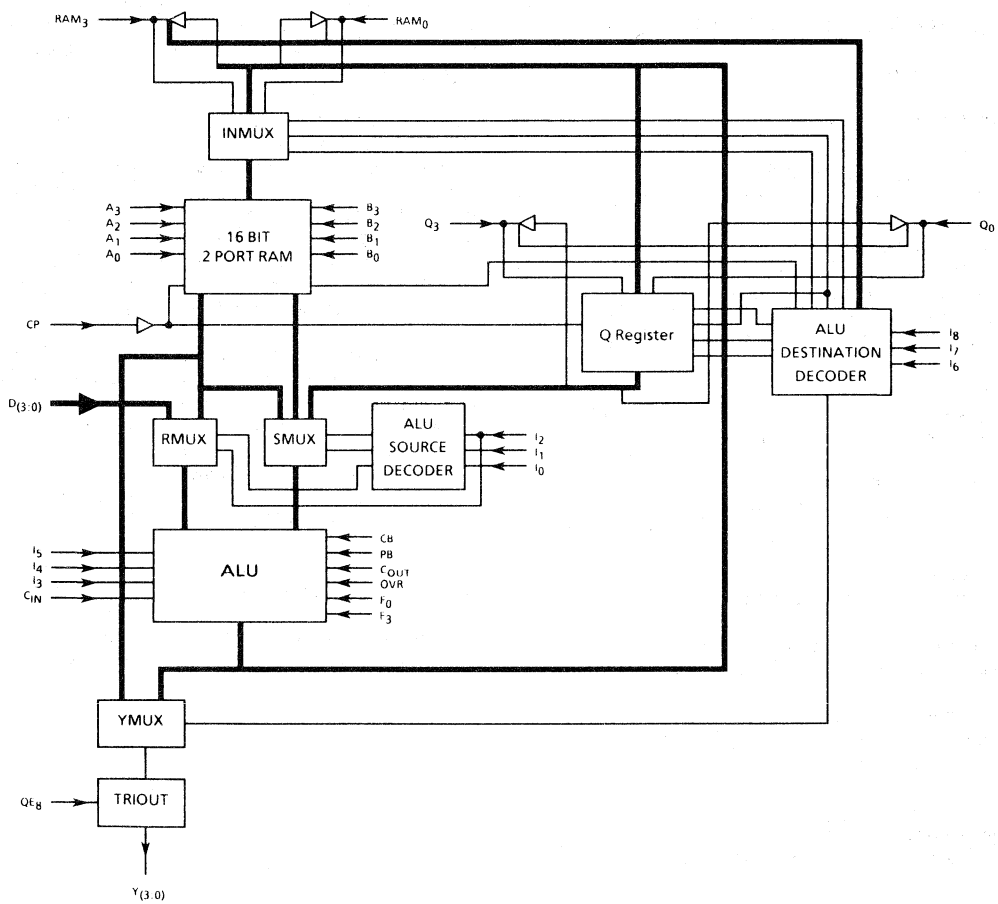


Figure 1: Block Diagram

MA2901

Radiation Hard 4-Bit Microprocessor Slice

The high-speed Arithmetic Logic Unit (ALU) can perform three binary arithmetic and five logic operations on the two 4-bit input words R and S. The R input field is driven from a 2-input multiplexer, while S input field is driven from a 3-input multiplexer. Both multiplexers also have an inhibit capability; that is, no data is passed. This is equivalent to a "zero" source operand.

The ALU R-input multiplexer has the RAM A-port and the direct data inputs (D) connected as inputs. Likewise, the ALU S-input multiplexer has the RAM A-port, the RAM B-port and the Q register connected as inputs.

This multiplexer scheme gives the capability of selecting various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. These five inputs, when taken two at a time, result in ten possible combinations of source operand pairs. These combinations include AB, AD, AQ, A0, BD, BQ, B0, DQ, D0 and Q0. It is apparent the AD, AQ and A0 are somewhat redundant with BD, BQ and B0 in that if the A address and B address are the same, the identical function results. Thus, there are only seven completely non-redundant sourced operand pairs for the ALU. The MA2901 microprocessor implements eight of these pairs. The microinstruction inputs used to select the ALU source operands are the I_0, I_1, and I_2 inputs. The definition of I_0, I_1, and I_2 for the eight source operand combinations are as shown in figure 2. Also shown is the octal code for each selection.

The two source operands not fully described as yet are the D input and Q input. The D input is the four-bit wide direct data field input. This port is used to insert all data into the working registers inside the device. Likewise this input can be used in the ALU to modify any of the internal data files. The Q register is a separate 4-bit file intended primarily for multiplication and division routines but it can also be used as an accumulator or holding register for some applications.

The ALU itself is a high speed arithmatic/logic operator capable of performing three binary arithmatic and five logic functions. The I_3, I_4, and I_5 microinstruction inputs are used to select the ALU function. The definition of these inputs is shown in Figure 3. The octal code is also shown for reference. The normal technique for cascading ALU of several devices is in a look-ahead carry mode. Carry generate, GN, and carry propagate, PN, are outputs of the device for use with a carry-look-ahead-generator. A carry-out $C_n + 4$, is also generated and is available as an output for use as the carry flag in a status register. Both carry-in (C_n) and carry-out ($C_n + 4$) are active HIGH.

The ALU has three other status-oriented outputs. These are F_3, F = 0, and overflow (OVR). The F_3 output is the most significant (sign) bit of the ALU and can be used to determine positive or negative results without enabling the three-state data outputs. F_3 is non-inverted with respect to the sign bit output Y_3. The F = 0 output is used for zero detect. It is an open-collector output and can be wire OR'ed between microprocessor slices. F = 0 is HIGH when all F outputs are LOW. The overflow output (OVR) is used to flag arithmetic operations that exceed the available two's complement number range. The overflow output (OVR) is HIGH when overflow exists. That is when $C_n + 3$ and $C_n + 4$ are not the same polarity.

The ALU data output is routed to several destinations. It can be a data output of the device and it can also be stored in the RAM or the Q register. Eight possible combinations of ALU destination functions are available as defined by the I_6, I_7, and I_8 microinstruction inputs. These combinations are shown in figure 4.

The four-bit data output field (Y) features three-state outputs and can be directly bus organised. An output control (OEN) is used to enable the three-state outputs. When OEN is HIGH, the Y outputs are in the high-impedance state.

A two-input multiplexer is also used at the data output such that either the A-port of the RAM or the ALU outputs (F) are selected at the device Y outputs. This selection is controlled by the I_6, I_7, and I_8 micro-instruction inputs.

As was discussed previously, the RAM inputs are driven from a three-input multiplexer. This allows the ALU outputs to be entered non-shifted, shifted up one position ($\times 2$) or shifted down one position ($\div 2$). The shifter has two ports; labeled RAM_0 and RAM_3. Both of these ports consist of a buffer-driver with a three-state output and an input to the multiplexer.

In the shift up mode, the RAM_3 buffer is enabled and the RAM_0 multiplexer input is enabled. Likewise, in the shift down mode, the RAM_0 buffer and RAM_3 input are enabled. In the no-shift mode, both buffers are in the high-impedance state and the multiplexer inputs are not selected. The shifter is controlled from the I_6, I_7 and I_8 microinstruction inputs as defined in Figure 4.

Similarly, the Q register is driven from a 3-input multiplexer. In the non-shift mode, the multiplexer enters the ALU data into the Q register. In either the shift-up or shift-down mode, the multiplexer selects the Q register data appropriately shifted up or down. The Q shifter also has two ports; one is labeled Q_0 and the other is Q_3. The operation of these two ports is similar to the RAM shifter and is also controlled from I_6, I_7, and I_8 as shown in Figure 4.

The clock input shown in Figure 1 controls the RAM, the Q registerm and the A and B data latches. When enabled, data is clocked into the Q register on the LOW-to-HIGH transition of the clock. When the clock input is HIGH, the A and B latches are open and will pass whatever data is present at the RAM outputs. When the clock input is LOW, the latches are closed and will retain the last data entered. If the RAM-EN is enabled new data will be written into the RAM file (word) defined by the B address field when the clock input is LOW.

Microcode				ALU Source Operands	
I_2	I_1	I_0	Octal Code	R	S
L	L	L	0	A	C
L	L	H	1	A	B
L	H	L	2	0	Q
L	H	H	3	0	B
H	L	L	4	0	A
H	L	H	5	D	A
H	H	L	6	D	Q
H	H	H	7	D	0

Figure 2: ALU Source Operand Control

Microcode				ALU Function	Symbol
I_5	I_4	I_3	Octal Code		
L	L	L	0	R plus S	R + S
L	L	H	1	S minus R	S - R
L	H	L	2	R minus S	R - S
L	H	H	3	R OR S	R $\vee$ S
H	L	L	4	RN AND S	RN $\wedge$ S
H	L	H	5	R AND S	R $\wedge$ S
H	H	L	6	R EX-OR S	R $\forall$ S
H	H	H	7	R EX-NOR S	RN $\forall$ SN

Figure 3: ALU Function Control

Source Operands and ALU Function

Any one of eight source operand pairs can be selected by instruction inputs I_0, I_1 and I_2 for use by the ALU; instruction inputs I_3, I_4, and I_5 then control function selection for the ALU - five logic and three arithmetic functions. In the arithmetic mode, the carry input (C_n) also affects the ALU functions; the carry input has no effect on the 'F' result in the logic mode. These control parameters (I_6 - I_0 and C_n) are summarised in Figure 5 to completely define the ALU/source operand functions.

The ALU functions can also be examined on a task basis: that is, add, subtract, AND, OR, and so on. Again, in the arithmetic mode, the carry input still affect the result, whereas in the logic mode it will not. Figures 6 and 7, respectively, define the various logic and arithmetic functions of the ALU; both carry states ($C_n = 0$ / $C_n = 1$) are defined in the function matrices.

Microcode				RAM Function		Q-Reg. Function		Y Output	RAM Shifter		Q Shifter	
I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_3	Q_0	Q_3
L	L	L	0	X	None	None	F→Q	F	X	X	X	X
L	L	H	1	X	None	X	None	F	X	X	X	X
L	H	L	2	None	F→B	X	None	A	X	X	X	X
L	H	H	3	None	F→B	X	None	F	X	X	X	X
H	L	L	4	Down	F/2→B	Q/2→Q	F	-	F_0	IN_3	Q_0	IN_3
H	L	H	5	Down	F/2→B	X	None	F	F_0	IN_3	Q_0	X
H	H	L	6	Up	2F→B	Up	2Q→Q	F	IN_0	F_3	IN_0	Q_3
H	H	H	7	Up	2F→B	X	None	F	IN_0	F_3	X	Q_3

X = Don't Care. Electrically, the shift pin is a TTL input internally connected to a TRI-STATE output which is in the high-impedance state.
B = Register addressed by B inputs.
Up is towards MSB, Down is toward LSB.

Figure 4: ALU Destination Control

	$I_{2,1,0}$ Octal	0	1	2	3	4	5	6	7
Octal $I_{5,4,3}$	ALU Source / ALU Function	A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0	C_n = L R plus S	A + Q	A + B	Q	B	A	D + A	D + Q	D
	C_n = H	A + Q + 1	A + B + 1	Q + 1	B + 1	A + 1	D + A + 1	D + Q + 1	D + 1
1	C_n = L S minus R	Q - A - 1	B - A - 1	Q - 1	B - 1	A - 1	A - D1	Q - D - 1	- D - 1
	C_n = H	Q - A	B - A	Q	B	A	A - D	Q - D	- D
2	C_n = L R minus S	A - Q - 1	A - B - 1	- Q - 1	- B - 1	- A - 1	D - A - 1	D - Q - 1	D - 1
	C_n = H	A - Q	A - B	- Q	- B	- A	D - A	D - Q	D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	RN AND S	AN ∧ Q	AN ∧ B	Q	B	A	DN ∧ A	DN ∧ Q	0
6	R EX-OR S	A ∀ Q	A ∀ B	Q	B	A	D ∀ A	D ∀ Q	D
7	R EX-NOR S	AN ∀ QN	AN ∀ BN	Q	B	A	DN ∀ AN	DN ∀ QN	DN

+ = plus; - = minus; ∨ = OR; ∧ = AND; ∀ = EX-OR

Figure 5: Source Operand and ALU Function Matrix

Octal $I_{5,4,3}$ / $I_{2,1,0}$	Group	Function
40	AND	A Q
41		A B
45		D A
46		D Q
30	OR	A ∨ Q
31		A ∨ B
35		D ∨ A
36		D ∨ Q
60	EX-OR	A ∀ Q
61		A ∀ B
65		D ∀ A
66		D ∀ Q
70	EX-NOR	AN ∀ QN
71		AN ∀ BN
75		DN ∀ AN
76		DN ∀ QN
72	INVERT	Q
73		B
74		A
77		D
62	PASS	Q
63		B
64		A
67		D
32	PASS	Q
33		B
34		A
37		D
40	'ZERO'	0
43		0
44		0
47		0
50	AND	AN Q
51		AN B
55		DN A
56		DN Q

Figure 6: ALU Logic Mode Functions (C_n Irrelevant)

Octal $I_{5,4,3}$ / $I_{2,1,0}$	C_n = 0 (Low)		C_n = 1 (High)	
	Group	Function	Group	Function
00	ADD	A + Q	ADD plus one	A + Q + 1
01		A + B		A + B + 1
05		D + A		D + A + 1
06		D + Q		D + Q + 1
02	PASS	Q	Increment	Q + 1
03		B		B + 1
04		A		A + 1
07		D		D + 1
12	Decrement	Q - 1	PASS	Q
13		B - 1		B
14		A - 1		A
27		D - 1		D
22	1s comp	- Q - 1	2s comp (Negate)	- Q
23		- B - 1		- B
24		- A - 1		- A
17		- D - 1		- D
10	SUBTRACT (1s comp)	Q - A - 1	SUBTRACT (2s comp)	Q - A
11		B - A - 1		B - A
15		A - D - 1		A - D
16		Q - D - 1		Q - D
20		A - Q - 1		A - Q
21		A - B - 1		A - B
25		D - A - 1		D - A
26		D - Q - 1		D - Q

Figure 7: ALU Arithmetic Mode Functions

MA2901

Radiation Hard 4-Bit Microprocessor Slice

Pin Description

Name	I/O	Description
A_{0-3}	I	The four address inputs to the register stack used to select one register whose contents are displayed through the A port.
B_{0-3}	I	The four address inputs to the register stack used to select one register whose contents are displayed through the B port and into which new data can be written when the clock goes LOW
I_{0-8}	I	The nine instruction control lines. Used to determine what data sources will be applied to the ALU ($I_{0,1,2}$), what function the ALU will perform ($I_{3,4,5}$), and what data is to be deposited in the Q-register or the register stack ($I_{6,7,8}$).
Q_3 RAM_3	I/O	A shift line at the MSB of the Q-register (Q_3) and the register stack (RAM_3). Electrically these lines are three-state outputs connected to TTL inputs internal to the device. When the destination code on $I_{6,7,8}$ indictes an up shift (octal 6 or 7) the three-state outputs are enabled and the MSB of the Q-register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. Otherwise, the three-state outputs are electrically OFF (high-impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q-register (octal 4) and RAM (octal 4 or 5)
Q_0 RAM_0	I/O	Shift lines like Q_3 and RAM3, but at the LSB of the Q-register and RAM. These pins are tied to the Q_3 and RAM_3 pins of the adjacent device to transfer data between devices for up and down shifts of the Q-register and ALU data.
D_{0-3}	I	Direct data inputs. A four-bit data field which may be selected as one of the ALU data sources for entering data into the devices D_0 is the LSB.
Y_{0-3}	O	The four data outputs. These are three-state output lines. When enabled, they display either the four outputs of the ALU or the data on the A-port of the register stack, as determined by the destination code $I_{6,7,8}$.
OEN	I	Output Enable. When OEN is HIGH, the Y outputs are OFF; when OEN is LOW, the Y outputs are active (HIGH or LOW).
GN; PN	O	The carry generate and propagate outputs of the internal ALU. These signals are used with the MA2901 for carry lookahead.
OVR	O	Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.
F = 0	O	This is an open collector output which goes HIGH (OFF) if the data on the four ALU outputs F_{0-3} are all LOW. In positive logic, it indicates the result of the ALU operation is zero.
F_3	O	The most significant ALU output bit.
C_n	I	The carry-in to the internal ALU.
$C_n + 4$	O	The carry-out of the ALU internal ALU.
CP	I	The clock input. The Q-register and register stack outputs change on the clock LOW-to-HIGH transition. The clock LOW time is internally the write enable to the 16 x 4 RAM which compromises the "master" latches of the register stack. While the clock is LOW, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.

Figure 8: Pin Description

DC Characteristics and Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0.5	7	V
V_I	Input voltage	-0.3	V_{DD} + 0.3	V
-	Current through any pin	-20	+ 20	mA
T_A	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Figure 9: Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Conditions	Total dose radiation not exceeding $3x10^5$ Rad (Si)			Total dose ≤1 MRad (Si)		Units
			Min.	Typ.	Max.	Min.	Max.	
V_{DD}	Supply voltage	-	4.5	5.0	5.5	4.5	5.5	V
V_{IH}	Input high voltage	-	2.4	-	-	2.4	-	V
V_{IL}	Input low voltage	-	-	-	0.8	-	0.3	V
V_{OH}	Output high voltage	I_{OH} = -6mA	2.4	-	-	2.4	-	V
V_{OL}	Output low voltage	I_{OL} = 12.0mA	-	-	0.4	-	0.4	V
I_{IN}	Input leakage current	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-	-	± 10	-	± 100	uA
I_{OZ}	Tristate leakage current	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-	-	± 50	-	± 100	uA
I_{DD}	Power supply current	Static, V_{DD} = 5.5V	-	0.1	10	-	10	mA

V_{DD} = 5V ± 10%, over full operating temperature range.

Figure 10: Operating Electrical Characteristics

AC Electrical Characteristics

at 5 volts and 25°C

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	40ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	25MHz
Maximum Clock LOW time	20ns
Minimum Clock HIGH time	20ns
Minimum Clock Period	40ns

Figure 11: Cycle Time and Clock Characteristics

From Input	To Output							
	Y	F_3	C_{n+4}	G, P	F = 0	OVR	RAM_0 RAM_3	Q_0 Q_3
A, B, Address	47	-	41	37	50	44	43	-
D	37	28	29	27	26	33	33	-
C_n	44	34	35	-	33	44	48	-
$I_{0,1,2}$	40	30	25	33	29	34	43	-
$I_{3,4,5}$	28	25	17	25	19	24	19	-
$I_{6,7,8}$	35	-	-	-	-	-	32	19
A Bypass ALU (I = 2xx)	25	-	-	-	-	-	-	-
Clock	58	48	48	42	58	48	54	27

Note: All timings in ns.

Figure 12: Combinational Propagation Delays. C_L = 50pF

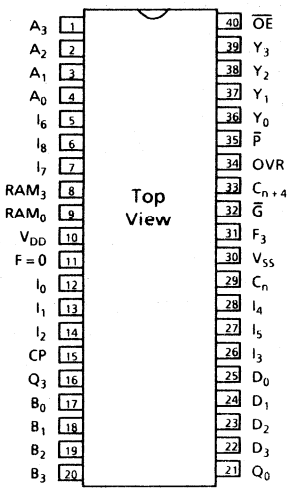
Input	CP: Set-up Time Before H→L	Hold Time After H→L	Set-up Time Before L→H	Hold Time After L→H
A, B Source Address	25	0	45	-
B Destination Address	25	Do Not Change		2
D	-	-	35	0
C_n	-	-	25	0
$I_{0,1,2}$	-	-	40	0
$I_{3,4,5}$	-	-	35	0
$I_{6,7,8}$	10	Do Not Change		10
$RAM_{0,3}$, $Q_{0,3}$	-	-	10	10

Figure 13: Set-up and Hold Times Relative to Clock (CP) Input

Out lines and Pin Assignments

Ref.	Min.	Nom.	Max.
A			5.60 (0.220)
A_1	0.38 (0.015)		1.53 (0.060)
b	0.35 (0.014)		0.59 (0.023)
c	0.20 (0.008)		0.36 (0.014)
D			51.31 (2.020)
e		2.54 (0.100) typ	
e_1		15.24 (0.600) typ	
H	4.71 (0.185)		5.38 (0.212)
M_E			15.90 (0.626)
Dimensions in mm (inches)			

MEDL XG405



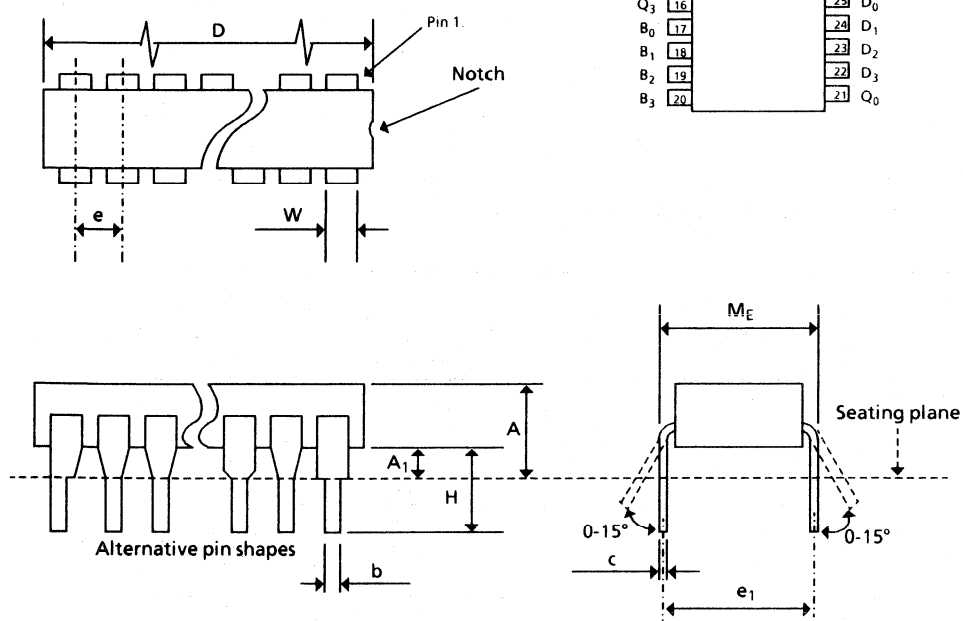


Figure 14: 40-Lead Ceramic DIL (solder seal) - package style C

RadiationTolerance

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

Total Dose (Function to specification)	10^6 Rad(Si)
Transient Upset (survivability)	$>10^{11}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	10^{15} neutrons/cm^2
Single Event Upset (GSO 10% worst case)	4.3×10^{-11} errors/bitday
Latch-up	Not possible

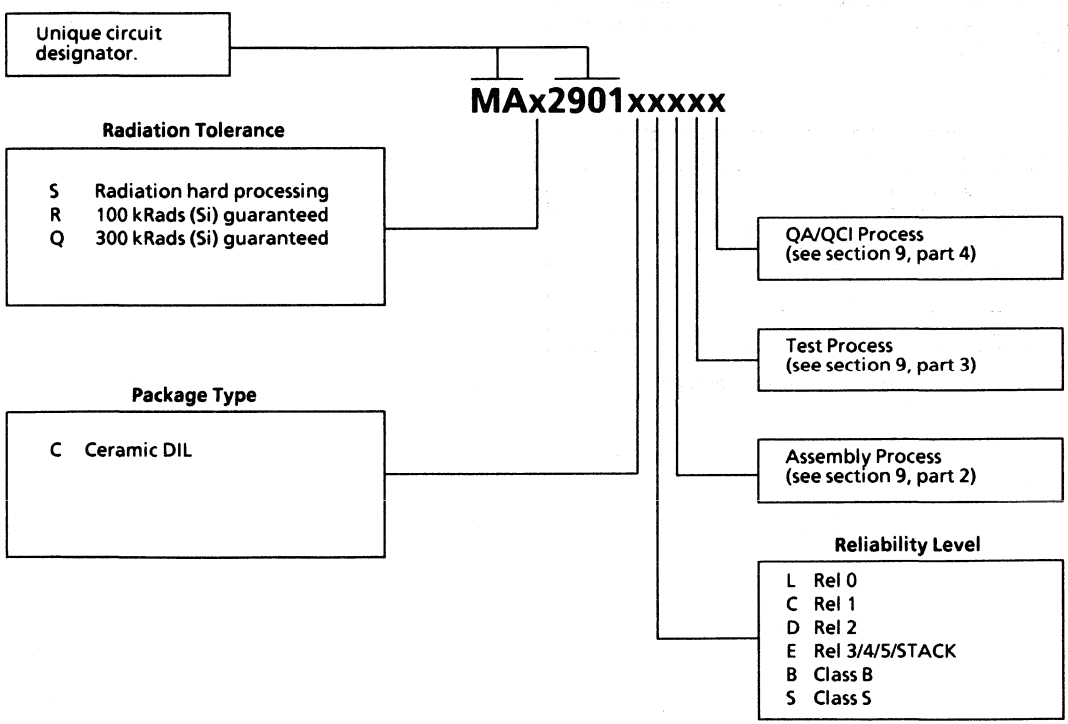
Figure 15: Radiation Hardness Parameters

Radiation Hard 4-Bit Microprocessor Slice

GEC PLESSEY
SEMICONDUCTORS

Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



GEC PLESSEY

SEMICONDUCTORS

S10600FDS/1 Issue 1.1 October 1990

MA2909/11

Radiation Hard Microprogram Sequencer

(Preliminary Data)

Features

- **Fully compatible with industry standard 2909A and 2911A components**
- **Radiation hard CMOS SOS technology**
- **High SEU immunity**
- **High speed / low power**
- **Fully TTL compatible**

General Description

The MA2909/11 Microprogram Sequencer is fully compatible with the industry standard 2909A and 2911A components, and forms part of the MEDL 2900 Series of devices. The series offers a building block approach to microcomputer and controller design, with each device in the range being expandable to permit efficient emulation of any microcode machine.

The devices have tristate outputs and have an internal address, with register changing state on LOW to HIGH clock transition.

The 4-bit slice can cascade to any number of microwords. Branch input for N-way branches is supported. Additional features include:

- 4-bit cascadable microprogram counter.
- 4 x 4 file with stack counter supporting nesting microsubroutines.
- Zero input for returning to the zero microcode word.
- Individual OR input for each bit for branching to higher microinstructions (2909 only).

The MA2909 is available in a 28 pin package and the MA2911 variant in a 20 pin package.

The 2909 is a 4-bit wide address controller intended for sequencing through a series of microinstructions contained in a ROM or PROM. Two 2909s may be interconnected to generate an 8-bit address (256 words), and three may be used to generate a 12-bit address (4K words).

The 2909 can select an address from any of four sources:

1) a set of external direct inputs (D);

2) external data from the R inputs, stored in an internal register;

3) a four-word push/pop stack; or

4) a program counter register (which usually contains the last address plus one).

The push/pop stack includes certain control lines so that it can efficiently execute nested subroutine linkages. Each of the four outputs can be OR'ed with an external input for conditional skip or branch instructions, and a separate line forces the outputs to all zeroes. The outputs are three-state.

The 2911 is an identical circuit to the 2909 except the four OR inputs are removed and the D and R inputs are tied together. The 2911 is in a 20-pin, 0.3in. centres package.

Radiation Hard Microprogram Sequencer
(Preliminary Data)

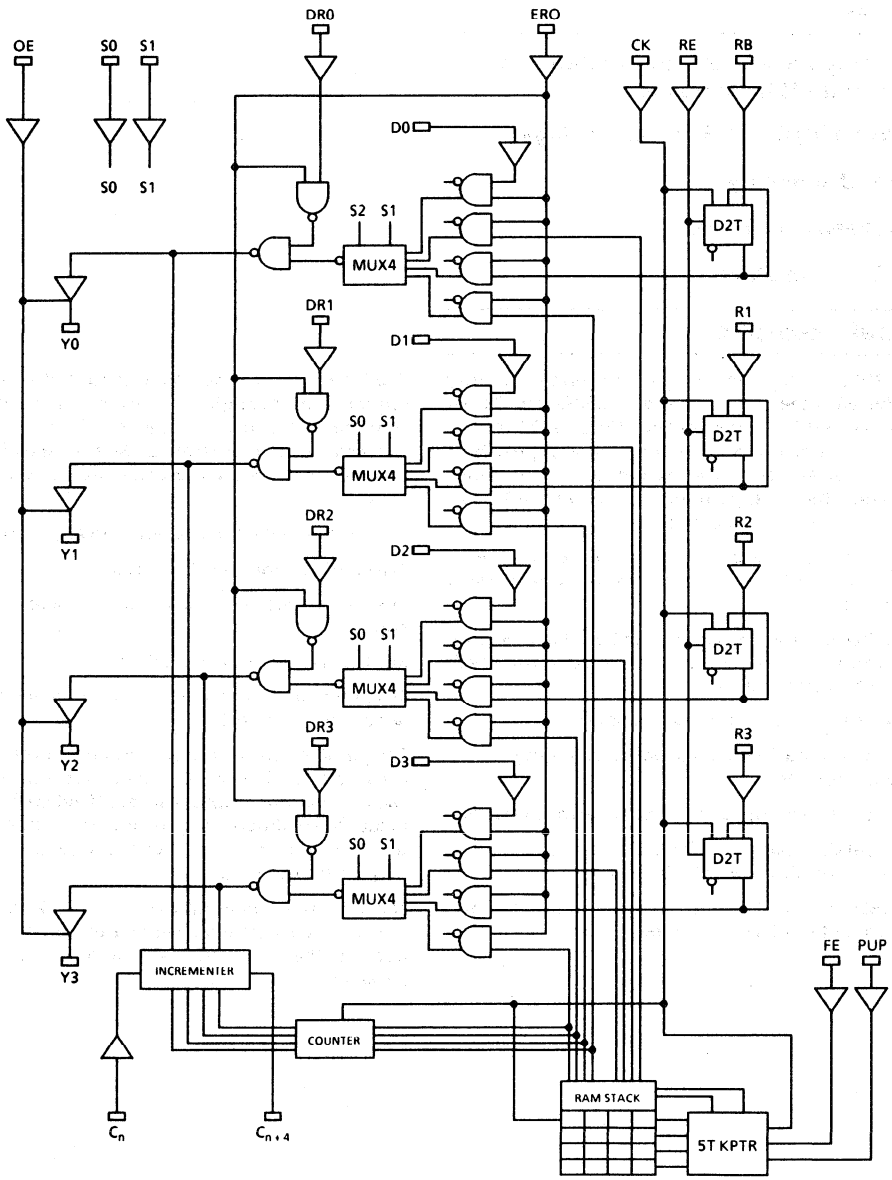


Figure 1: Microprogram Sequencer Block Diagram

MA2909/11

Radiation Hard Microprogram Sequencer

(Preliminary Data)

Architecture

The 2909/2911 are CMOS SOS microprogram sequencers intended for use in high-speed microprocessor applications. The device is a cascadable 4-bit slice such that two devices allow addressing of up to 256 words of microprogram and three devices allow addressing of up to 4K words of microprogram. A detailed logic diagram is shown in figure 1.

The device contains a four input multiplexer that is used to select either the address register, direct inputs, microprogram counter, or file as the source of the next microinstruction address. This multiplexer is controlled by the S0 and S1 inputs.

The address register consists of four D-type, edge triggered flip-flops with a common clock enable. When the address register enable is LOW, new data is entered into the register on the clock LOW-to-HIGH transition. The address register is available at the multiplexer as a source for the next microinstruction address. The direct input is a 4-bit field of inputs to the multiplexer and can be selected as the next microinstruction address. On the 2911 the direct inputs are also used as inputs to the register. This allows an N-way branch where N is any word in the microcode.

The 2909/2911 contains a microprogram counter (μPC) that is composed of a 4-bit incrementer followed by a4-bit register. The incrementer has carry-in (C_n) and carry-out ($C_n + 4$) such that cascading to larger word lengths is straight forward. The μPC can be used in either of two ways. When the least significant carry-in to the incrementer is HIGH, the microprogram register is loaded on the next clock cycle with the current Y output word plus one ($Y + 1 \rightarrow \mu PC$). Thus sequential microinstructions can be executed. If this least significant C_n is LOW, the incrementer passes the Y output word unmodified and the microprgram register is loaded with the same Y word on the next clock cycle ($Y \rightarrow \mu PC$). Thus, the same microinstruction can be executed any number of times by using the 4×4 file (stack). The file is used to provide return address linkage when executing microsubroutines. The file contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations (looping) to be performed without a push or pop.

The stack pointer operates as an up/down counter with separate push/pop and file enable inputs. When the file enable input is LOW and the push/pop input is HIGH, the PUSH operation is enabled. This causes the stack pointer to increment and the file to be written with the required return linkage - the next microinstruction address following the subroutine jump which initiated the PUSH.

If the file enable input is LOW and the push/pop control is LOW, a POP operation occurs. This implies the usage of the return linkage during this cycle and thus a return from subroutine. The next LOW-to-HIGH clock transition causes the stack pointer to decrement. If the file enable is HIGH, no action is taken by the stack pointer regardless of any other input.

The stack pointer linkage is such that any combination of pushed, pop or stack references can be achieved. One microinstruction subroutine can be performed. Since the stack is 4 words deep, up to four microsubroutines can be nested.

The ZERO input is used to force the four outputs to the binary zero state. When the ZERO input is LOW all Y outputs are LOW regardless of any other inputs (except OE). Each Y output bit also has a separate OR input such that a conditional logic one can be forced at each Y output. This allows jumping to different micro-instructions on programmed conditions.

The 2909/2911 feature three-state Y outputs. These can be particularly useful in designs requiring external equipment to provide automatic checkout of the micro-processor. The internal control can be placed in the high impedance state and preprogrammed...

Radiation Hard Microprogram Sequencer
(Preliminary Data)

Operation

Multiplexer Select Codes

Table 1 lists the select codes for the multiplexer. The two bits applied form the microword register (and additional combinational logic for branching) determine which data source contains the address for the next microinstruction. The contents of the selected source will appear on the Y outputs. Table 1 also shows the truth table for the output control and for the control of the push/pop stack. Table 2 shows indetail the effect of S_0, S_1, FE and PUP on the 2909. These four signals define the address that apears on the Y outputs and what the state of all the internal registers will be following the clock LOW-to-HIGH edge. In this illustration, the microprogram counter is assumed to contain initially some word J, the address register some word K, and the four words in the push/pop stack contain R_a through R_d.

OR1	ZERO	OE	Y1
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0 S_1

H = High, L = Low, Z = High Impedance

Table 1a: Output Control

FE	PUP	PUSH-POP stack change
H	X	No change
L	H	Increment stack pointer, then push current PC on to STK0
L	L	Pop stack (decrement stack pointer)

H = High, L = Low, X = Irrelevant

Table 1b: Synchronous Stack Control

S_1	S_2	Source for Y outputs	Symbol
L	L	Microprogram counter	µPC
L	H	Address/Holding register	AR
H	L	Push-Pop stack	STK0
H	H	Direct inputs	D_1

Table 1c: Address Selection

Cycle	S_1	S_0	FE	PUP	µPC	REG	STK0	STK1	STK2	STK3	Y_{OUT}	Comment	Principal Use
N	L	L	L	L	J	K	R_a	R_b	R_c	R_d	J	Pop Stack	End Loop
N+1			-		J+1	K	R_b	R_c	R_d	R_a	-		
N	L	L	L	H	J	K	R_a	R_b	R_c	R_d	J	Push µPC	Set-up Loop
N+1			-		J+1	K	J	R_a	R_b	R_c	-		
N	L	L	H	X	J	K	R_a	R_b	R_c	R_d	J	Continue	Continue
N+1			-		J+1	K	R_a	R_b	R_c	R_d	-		
N	L	H	L	L	J	K	R_a	R_b	R_c	R_d	K	Pop Stack; Use AR for Address	End Loop
N+1			-		K+1	K	R_b	R_c	R_d	R_a	-		
N	L	H	L	H	J	K	R_a	R_b	R_c	R_d	K	Push µPC; Jump to Address in AR	JSR AR
N+1			-		K+1	K	J	R_a	R_b	R_c	-		
N	L	H	H	X	J	K	R_a	R_b	R_c	R_d	K	Jump to Address in AR	JMP AR
N+1			-		K+1	K	R_a	R_b	R_c	R_d	-		
N	H	L	L	L	J	K	R_a	R_b	R_c	R_d	R_a	Jump to Address in STK0; Pop Stack	RTS
N+1			-		R_a+1	K	R_b	R_c	R_d	R_a	-		
N	H	L	L	H	J	K	R_a	R_b	R_c	R_d	R_a	Jump to Address in STK0; Push µPC	
N+1			-		R_a+1	K	J	R_a	R_b	R_c	-		
N	H	L	H	X	J	K	R_a	R_b	R_c	R_d	R_a	Jump to Address in STK0	Stack Ref (Loop)
N+1			-		R_a+1	K	R_a	R_b	R_c	R_d	-		
N	H	H	L	L	J	K	R_a	R_b	R_c	R_d	D	Pop Stack; Jump to Address on D	End Loop
N+1			-		D+1	K	R_b	R_c	R_d	R_a	-		
N	H	H	L	H	J	K	R_a	R_b	R_c	R_d	D	Jump to Address on D; Push µPC	JSR D
N+1			-		D+1	K	J	R_a	R_b	R_c	-		
N	H	H	H	X	J	K	R_a	R_b	R_c	R_d	D	Jump to Address on D	JMP D
N+1			-		D+1	K	R_a	R_b	R_c	R_d	-		

1 = High, 0 = Low, X = Irrelevant, Assume C_n = High
Note: STK0 is the location addressed by the stack pointer

Table 2: Output and Internal Next-Cycle Register States for 2909/2911

MA2909/11

Radiation Hard Microprogram Sequencer

(Preliminary Data)

Table 3 illustrates the execution of a subroutine using the 2909. The configuration of Figure 2 is assumed. The instruction being executed at any given time is the one contained in the microword register (μWR). The contents of the μWR also control (indirectly, perhaps) the four signals S_0, S_1, FE, and PUP. The starting address of the subroutine is applied to the D inputs of the 2909 at the appropriate time.

In the column on the left is the sequence of micro-instructions to be executed. At address J + 2, the sequence control portion of the microinstruction contains the command "Jump to subroutine at A".

At the time T_2, this instruction is in the μWR, and the 2909 inputs are set-up to execute the jump and save the return address. The subroutine address A is applied to the D inputs from the μWR and appears on the Y outputs. The first instruction of the subroutine, I(A), is accessed and is at the inputs of the μWR. On the next clock transition, I(A) is loaded into the μWR for execution, and the return address J + 3 is pushed on to the stack. The return instruction is executed at T_5. Table 4 is a similar timing chart showing one subroutine linking to a second, the latter consisting of only one microinstruction

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
2909 Inputs (from μWR)	S_1, S_0	0	0	3	0	0	2	0	0		
	FE	H	H	L	H	H	L	H	H		
	PUP	X	X	H	X	X	L	X	X		
	D	X	X	A	X	X	X	X	X		
Internal Registers	μPC	J + 1	J + 2	J + 3	A + 1	A + 2	A + 3	J + 4	J + 5		
	STK0	-	-	-	J + 3	J + 3	J + 3	-	-		
	STK1	-	-	-	-	-	-	-	-		
	STK2	-	-	-	-	-	-	-	-		
	STK3	-	-	-	-	-	-	-	-		
2909 Output	Y	J + 1	J + 2	A	A + 1	A + 2	J + 3	J + 4	J + 5		
ROM Output	(Y)	I(J + 1)	JSR A	I(A)	I(A + 1)	RTS	I(J + 3)	I(J + 4)	I(J + 5)		
Contents of μWR (instruction being executed)	μWR	I(J)	I(J + 1)	JSR A	I(A)	I(A + 1)	RTS	I(J + 3)	I(J + 4)		

Table 3: Subroutine Execution

CONTROL MEMORY

Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J-1	-
T_0	J	
T_1	J + 1	
T_2	J + 2	JSR A
T_6	J + 3	-
T_7	J + 4	
	-	
	-	-
	-	
	-	-
	-	
T_3	A	I(A)
T_4	A + 1	
T_5	A + 2	RTS
	-	
	-	-
	-	
	-	-
	-	
	-	-

(Routine B is only one instruction)

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
2909 Inputs (from μWR)	S_1, S_0	0	0	3	0	0	3	2	0	2	0
	FE	H	H	L	H	H	L	L	H	L	H
	PUP	X	X	H	X	X	H	L	X	L	X
	D	X	X	A	X	X	B	X	X	X	X
Internal Registers	μPC	J + 1	J + 2	J + 3	A + 1	A + 2	A + 3	B + 1	A + 4	A + 5	J + 4
	STK0	-	-	-	J + 3	J + 3	J + 3	A + 3	J + 3	J + 3	-
	STK1	-	-	-	-	-	-	J + 3	-	-	-
	STK2	-	-	-	-	-	-	-	-	-	-
	STK3	-	-	-	-	-	-	-	-	-	-
2909 Output	Y	J + 1	J + 2	A	A + 1	A + 2	B	A + 3	A + 4	J + 3	J + 4
ROM Output	(Y)	I(J + 1)	JSR A	I(A)	I(A + 1)	JSR B	RTS	I(A + 3)	RTS	I(J + 3)	I(J + 4)
Contents of μWR (instruction being executed)	μWR	I(J)	I(J + 1)	JSR A	I(A)	I(A + 1)	JSR B	RTS	I(A + 3)	RTS	I(J + 3)

Table 4: Two Nested Subroutines

CONTROL MEMORY

Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J-1	-
T_0	J	
T_1	J + 1	-
T_2	J + 2	JSR A
T_9	J + 3	-
	-	-
	-	-
	-	-
	-	-
T_3	A	-
T_4	A + 1	-
T_5	A + 2	JSR B
T_7	A + 3	-
T_8	A + 4	RTS
	-	-
	-	-
	-	-
	-	-
T_6	B	RTS
	-	-

Radiation Hard Microprogram Sequencer
(Preliminary Data)

DC Characteristics and Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0 5	7	V
V_I	Input voltage	-0 3	V_{DD} + 0 3	V
I_{DD}	Current through any pin	-	20	mA
T_A	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Figure 2: Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{OH}	Output high voltage	V_{DD} = Min., I_{OH} = 5 6mA, V_{IN} = V_{IH} or V_{IL}	2 4	-	V
V_{OL}	Output low voltage	V_{DD} = Min., I_{OL} = 16mA, V_{IN} = V_{IH} or V_{IL}	-	0 5	V
V_{IH}	Input high level (Note 1)	Guaranteed input logical high voltage for all inputs	V_{DD}/2	-	V
V_{IL}	Input low level (Note 1)	Guaranteed input logical low voltage for all inputs	-	0 8	V
I_{IH}	Input high current	V_{DD} = Max., V_{IN} = V_{DD}	-	10	µA
I_{IL}	Input low current	V_{DD} = Max., V_{IN} = V_{SS}	-	10	µA
I_{OZH}	Tristate high current	V_{DD} = Max., V_O = V_{DD}	-	50	µA
I_{OZL}	Tristate low current	V_{DD} = Max., V_O = V_{SS}	-	-50	µA
I_{DD}	Power supply current	V_{DD} = Max.	-	5	mA

1. These input levels provide no guaranteed noise immunity and should only be static tested in a noise-free environment.
2. V_{DD} = 5V ± 10%.

Figure 3: DC Operating Characteristics

MA2909/11

Radiation Hard Microprogram Sequencer

(Preliminary Data)

Time	
Minimum clock low time	15
Minimum clock high time	15

Table 8: Cycle Time and Clock Characteristics

From Input	Y	$C_n + 4$
D_i	28	32
S_0, S_1	26	27
OR_i	17	24
C_n	-	20
ZERO	31	34
OE LOW (enable)	19	-
OE HIGH (disable)*	20	-
Clock : S_1S_0 = LH	47	43
Clock : S_1S_0 = LL	47	43
Clock : S_1S_0 = HL	47	50

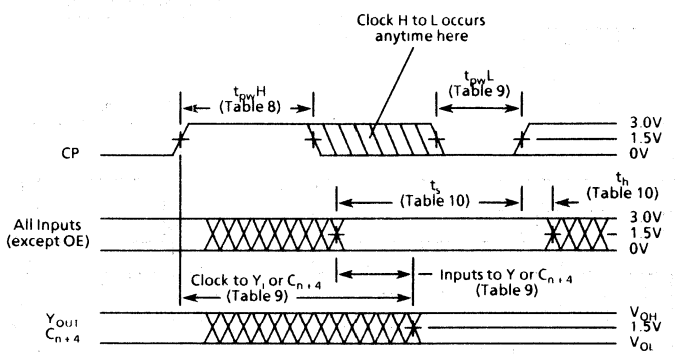
*C_L = 5pF

Table 9: Maximum Combinational Propagation Delays

From Input	Set-up Time	Hold Time
AE	3	5
R_i	3	5
PUP	13	5
FE	13	5
C_n	9	5
D_i	15	0
OR_i	13	0
S_0, S_1	16	0
ZERO	22	0

Table 10: Guaranteed Set-up and Hol Times (all in ns)

All times in ns across full voltage and temperature range.



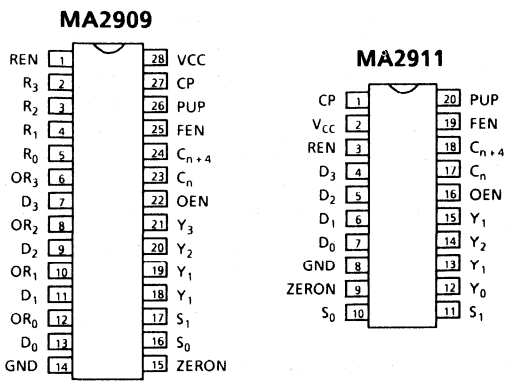
Radiation Hard Microprogram Sequencer

(Preliminary Data)

GEC PLESSEY

SEMICONDUCTORS

Connection Diagram Top View



28 Pin

Ref.	Min.	Nom.	Max.
A	-	-	5.60 (0.220)
A_1	0.38 (0.015)	-	1.53 (0.060)
b	0.35 (0.014)	-	0.59 (0.023)
c	0.20 (0.008)	-	0.36 (0.014)
D	-	-	36.02 (1.418)
e	-	2.54(0.100) typ.	-
e_1	-	15.24(0.600) typ.	-
H	4.71 (0.185)	-	5.38 (0.212)
M_E	-	-	15.90 (0.626)
Z	-	-	1.27 (0.050)
W	-	-	1.53 (0.060)
Dimensions in mm (inches)			

20 Pin

Ref.	Min.	Nom.	Max.
A	-	-	5.60 (0.220)
A_1	0.38 (0.015)	-	1.53 (0.060)
b	0.35 (0.014)	-	0.59 (0.023)
c	0.20 (0.008)	-	0.36 (0.014)
D	23.11 (0.910)	-	25.65 (1.010)
e	-	2.54(0.100) typ.	-
e_1	-	8.13 (0.300) typ.	-
H	4.71 (0.185)	-	5.38 (0.212)
M_E	-	-	7.95 (0.313)
Z	-	-	1.27 (0.050)
W	-	-	1.53 (0.060)
Dimensions in mm (inches)			

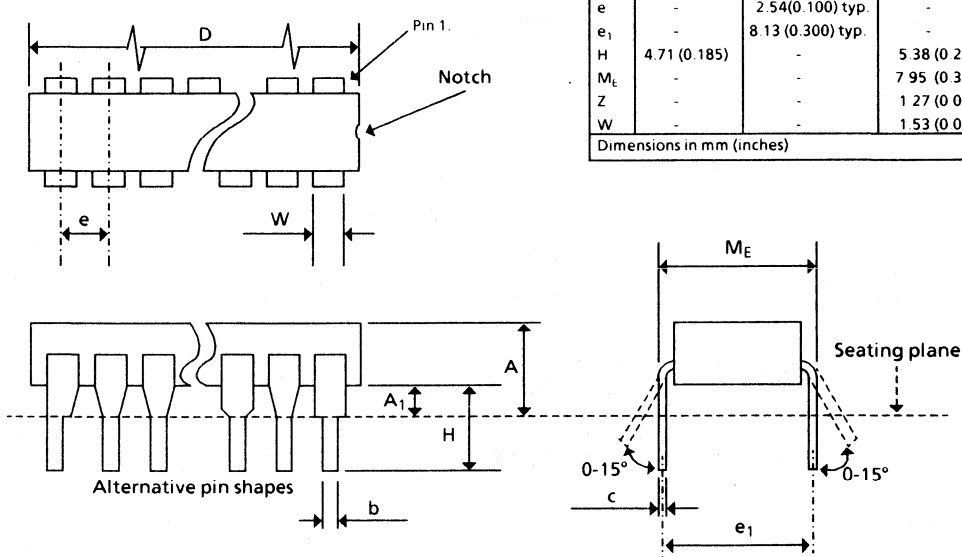


Figure 4: 28/20-Lead Ceramic DIL (solder seal) - package style C

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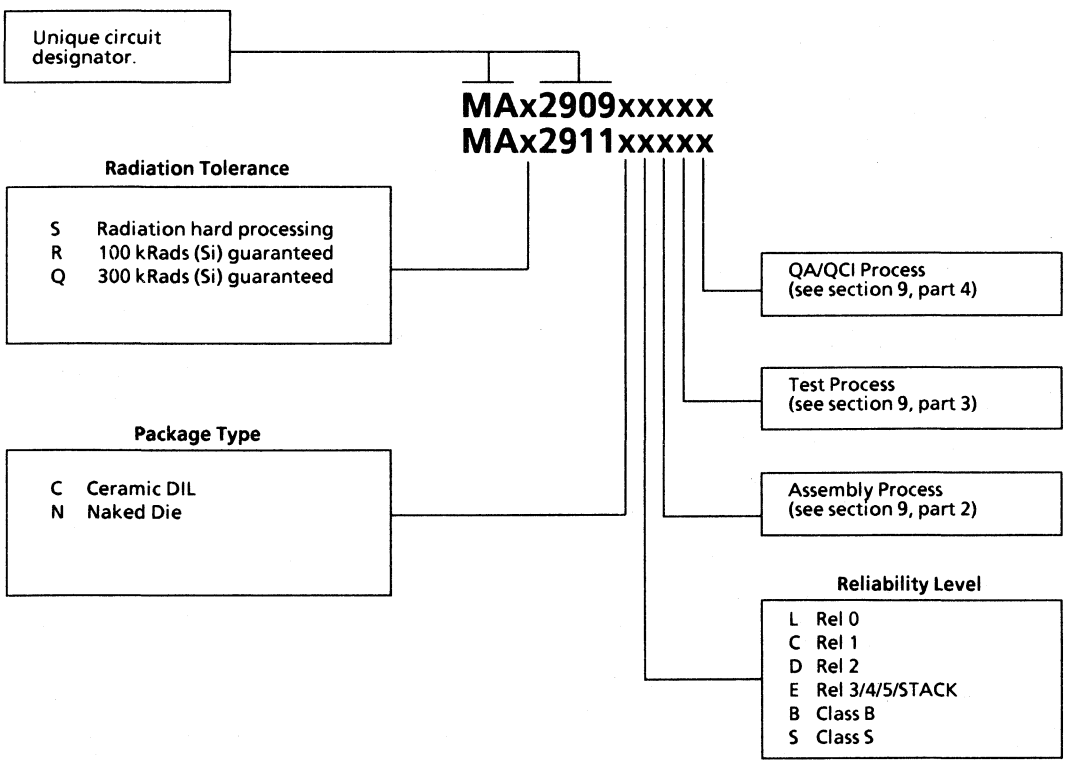
Radiation Hard Microprogram Sequencer

(Preliminary Data)

Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



GEC PLESSEY

SEMICONDUCTORS

MA2910

Radiation Hard Microprogram Controller

S10603FDS Issue 1.3 October 1990

Features

- **Fully compatible with industry standard 2910A**
- **CMOS SOS technology**
- **Radiation hard and high SEU immunity**
- **High speed/Low power**
- **Fully TTL compatible**

General Description

The industry standard MA2910 Microprogram Controller forms part of the MA2900 family of devices.

Offering a building block approach to microcomputer and controller design, each device in the range is expandable permitting efficient emulation of any microcode-controlled machine. The family has been designed for operation in severe environments such as space, and is qualified to the highest levels of reliability.

The MA2910 Micro-program Controller is an address sequencer intended for sequence control of micro-instructions stored in microprogram memory in high speed micro-processor applications.

All internal elements are full 12 bits wide and address up to 4096 words with one chip. The device has an integral settable 12 bit internal loop counter for repeating instructions and counting loop iterations.

The MA2910 has four address sources which allow Microprogram Address to be selected from the microgram counter, branch address bus, 9 level push/pop stack, or internal holding register.

The MA2910 supports 100ns cycle times and has an integral decoder function to enable external devices onto branch address bus which eliminates the requirement for an external decoder.

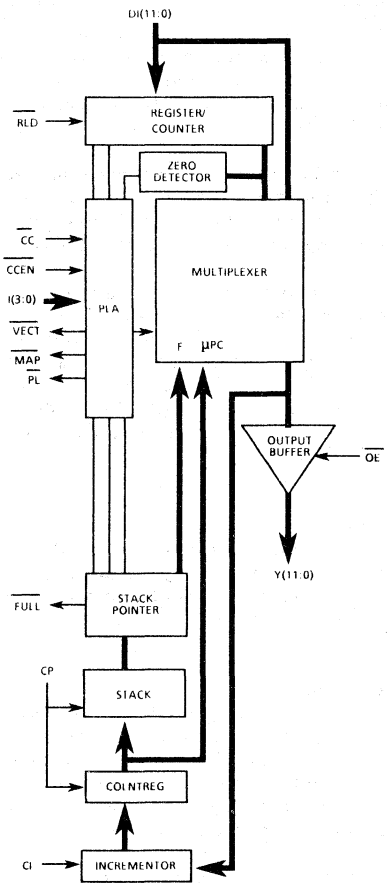


Figure 1. Block Diagram

4

Operation

The MA2910 is a SOS microprogram controller intended for use in high speed microprocessor applications. Besides the capability of sequential access, it provides conditional branching to any microinstruction within its 4096-microword range.

A last-in, first-out stack provides microsubroutine return linkage and looping capability; there are nine nesting levels of microsubroutines. Microinstruction loop count control is provided with a count capacity of 4096.

The device is controlled by 16, 4-bit microinstructions. The PLA decodes the microinstructions on I(3:P) and produces select control codes for the multiplexer, register/counter, microprogram counter register, and stack. The 4-bit microinstructions also generate three active low enable signals ($\overline{PL}$, $\overline{VECT}$, and $\overline{MAP}$) for external use. The operation of each device block is detailed below:

Multiplexer
The MA2910 contains a four-input multiplexer that is used to select either the register/counter, direct input, microprogram counter, or stack as the source of the next microinstruction address.

Register/Counter
The register/counter consists of 12 D-type, edge-triggered flip-flops, with a common clock enable. It is operated during microinstructions (8,9,15) as a 12-bit down counter, with result = zero available as a microinstruction branch test criterion. This provides efficient iteration of microinstructions.

The register/ counter is arranged such that if it is preloaded with a number N and is then used as a loop termination counter, the sequence will be executed exactly N + 1 times. During instruction 15, a three way branch under combined control of the loop counter and the condition code is available. When its load control, RLD, is LOW, new data is loaded on the next positive control transition.

The output of the register/counter is available to the multiplexer as a source for the next microinstruction address. The direct input furnishes a source of data for loading the register /counter.

Microprogram Counter-Register
The Microprogram Counter Register (μPC) is composed of a 12-bit incrementer followed by a 12-bit register. The (μPC) can be used in one of two ways: When the carry-in to the incrementer is HIGH, the microprogram register is loaded onto the next clock cycle with the current Y output word plus one (Y + 1 → μPC). Sequential microinstructions are thus executed. When the carry-in is LOW, the incrementer passes the Y output unmodified so that the μPC is reloaded with the same Y word on the next clock cycle (Y → μPC). The same microinstruction is thus executed any number of times.

Stack and Stack Pointer
The third source available at the multiplexer input is a 9-word by 12-bit stack. The stack is used to provide return address linkage when executing microsubroutines or loops. The stack contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations (looping) to be performed without a POP.

Explicit control of the stack pointer occurs during instruction 0 (RESET), which makes the stack empty by resetting the SP to zero. After a RESET, and whenever the stack is empty, the contents of the top of the stack are undefined until a push occurs. Any POPs performed while the stack is empty put undefined data on the outputs and leave the stack at zero.

The stack pointer operates as an up/down counter. During microinstructions 1,4, and 5, the PUSH operation may occur. This causes the stack pointer to increment and the file to be written with the required return linkage. On the cycle following the PUSH, the return data is at the new location pointed to by the stack pointer.

During five microinstructions, a POP operation may occur. The stack pointer decrements at the next rising clock edge following a POP, effectively removing old information from the top of the stack.

The stack pointer linkage is such that any sequence of pushes, pops, or stack references can be achieved. At RESET (instruction 0), the depth of nesting becomes zero. For each PUSH, the nesting depth increases by one; for each POP, the depth decreases by one.

MA2910
Radiation Hard Microprogram Controller

Pin Description

VDD and GND (Power and Ground)

The MA2910 operator from a single supply voltage of 5V + 10%

D (0 to 11) (Direct input)

These connections provide direct input to the register/counter, and the multiplexer. D0 is the least significant bit and D1 the most significant.

I (0 to 3) (instruction bus)

The data on these inputs is read on the rising edge of CP. It determines the instrcution to be exceeded in accordance with table 1.

$\overline{CC}$ (Condition Code)

This active low input is used to determine the result of conditional instruction. LOW indicates a TRUE condition.

$\overline{CCEN}$ (Condition code enable)

This active low input enables the CC input. When CCEN is HIGH, CC is ignored and a conditional operation execute as though CC were LOW (TRUE).

$\overline{CI}$ (Carry input)

When HIGH this input causes the microprogramme counter register to increment on the rising edge of CP. When LOW the counter remains unchanged.

$\overline{RLD}$ (Register load)

This active low input loads the register/counter from the D bus on the rising edge of CP. It will override any HOLD or DEC instruction specified by data on the I bus.

Y (0 to 11) (Microcode address)

This is a 12 bit wide trislate output bus. It carries the micro ode address generated according to the instruction read in from the I bus. OE can be used to put the bus in a high impedance state. This allows another to take control of the microcode address bus.

$\overline{OE}$ (Output enable)

This active low input is used to enable the 12 lines of the Y bus.

CP (Clock Pulse)

A LOW-to-HIGH transister on this input is used to trigger all state changes within the device.

$\overline{FULL}$ (stack full)

The active low output FULL indicater that 9 items have been loaded onto the stack.

$\overline{PL}$, $\overline{MAP}$ & $\overline{VECT}$ (pipeline, amp and vector)

These active low outputs are set according to the instruction being executed. At any time only one is enabled. They can be used.

$\overline{PL}$ The primary source of microprogramme jumps, usually part of a pipeline register.

$\overline{MAP}$ A PRDM which maps and instruction to a micrcode starting location.

$\overline{VECT}$ An optional thrid source, after a ventor from a DMA or interrupt source.

I_3-I_0	MNEMONIC	NAME	REGISTER/CONTROL CONTENTS	FAIL $\overline{CCEN}$ = LOW & $\overline{CC}$ = HIGH		PASS $\overline{CCEN}$ = HIGH & $\overline{CC}$ = LOW		REGISTER/ CONTROL	ENABLE
				Y	STACK	Y	STACK		
0	JZ	JUMP ZERO	X	0	CLEAR	O	CLEAR	HOLD	PL
1	CJS	COND JSP PL	X	PC	HOLD	D	PUSH	HOLD	PL
2	JMAP	JUMP MAP	X	D	HOLD	D	HOLD	HOLD	MAP
3	CJP	COND JUMP PL	X	PC	HOLD	D	HOLD	HOLD	PL
4	PUSH	PUSH/COND LD CNTR	X	PC	PUSH	PC	PUSH	Note1	PL
5	JSRP	COND JSB R/PL	X	R	PUSH	D	PUSH	HOLD	PL
6	CJV	COND JUMP VECTOR	X	PC	HOLD	D	HOLD	HOLD	VECT
7	JRP	COND JUMP R/PL	X	R	HOLD	D	HOLD	HOLD	PL
8	RFCT	REPEAT LOOP, CNTR ≠ 0	≠0 =0	F PC	HOLD POP	F PC	HOLD POP	DEC HOLD	PL PL
9	RPCT	REPEAT PL, CNTR ≠ 0	≠0 =0	D PC	HOLD HOLD	D PC	HOLD HOLD	DEC HOLD	PL PL
10	CRTN	COND RTN	X	PC	HOLD	F	POP	HOLD	PL
11	CJPP	COND JUMP PL & POP	X	PC	HOLD	D	POP	HOLD	PL
12	LDCT	LD CNTR & CONTINUE	X	PC	HOLD	PC	HOLD	LOAD	PL
13	LOOP	TEST END LOOP	X	F	HOLD	PC	POP	HOLD	PL
14	CONT	CONTINUE	X	PC	HOLD	PC	HOLD	HOLD	PL
15	TWB	THREE-WAY BRANCH	≠0 =0	F D	HOLD POP	PC PC	POP POP	DEC HOLD	PL PL

NOTE 1. If $\overline{CCEN}$ = LOW & $\overline{CC}$ = HIGH, hold; else load.

Figure 2. Table of Instructions

Instruction Set

The MA2910 provides 16 instructions which select the address of the next microinstruction to be executed. 4 of the instructions are unconditional and their effect depends only on the instruction. 10 of the instructions have an effect which is partially controlled by external conditions. 3 of the instructions have an effect which is partially controlled by the contents of the internal register/counter. In this discussion it is assumed the CI is tied HIGH.

In the 10 conditional instructions, the result of the data-dependent test is applied to $\overline{CC}$. If the $\overline{CC}$ input is LOW, the test is considered passed, and the action specified in the name occurs; otherwise, the test has failed and an alternate (often simply the execution of the next sequential microinstruction) occurs. Testing of $\overline{CC}$ may be disabled for a specific microinstruction by setting $\overline{CCEN}$ HIGH, which unconditionally forces the action specified in the name; that is it forces a pass.Other ways of using $\overline{CCEN}$ include; (1) tying it HIGH, which is useful if no microinstruction is data-dependent; (2) tying it LOW if data-dependent instructions are never forced unconditionally; or (3) tying it to the source of MA2910 instruction bit I_0, which leaves instructions 4,6 and 10 as data-dependent but leaves others unconditional. All of these tricks save one bit of microcode width.

The effect of three instructions depend upon the contents of the register/counter. Unless the counter holds a value of zero, it is decremented; if it does hold zero, it is held and a different microprogram next address is selected.These instructions are useful for executing a microinstruction loop a finite number of times. Instruction 15 is affected both by the external condition code and the internal register/counter.

The most effective technique for understanding the MA2910 is to simply take each instruction and review its operation. In order to provide some feel for the actual execution of these instructions, examples of all 16 instructions are included.

The examples given should be interpreted in the following manner: The intent is to show microprogram flow as various microprogram memory words are executed.

For example, the CONTINUE instruction (number 14) simply means that the contents of the microprogram memory word 50 are executed, then the contents of word 51 are executed. This is followed by the contents of 52 and 53. The microprogram addresses used in the examples were arbitrarily chosen and have no meaning other than to show instruction flow. The exception to this is the first example, JUMP ZERO, which forces the microprogram location counter to address ZERO. Each dot refers to the time that the contents of the microprogram memory word is in the pipeline register. While no special symbology is used for the conditional instructions, the following text will explain what the conditional choices are in each example.

Instruction 0: JZ (Jump to Zero, or Reset).
This instruction unconditionally specifies that the address of the next microinstruction is zero. Many designs use this feature for power-up sequences and provide the power-up firmware beginning at microprogram memory word location 0.

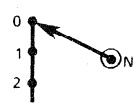


Figure 3: 0 JUMP ZERO (JZ)

Instruction 1: Conditional Jump-to-Subroutine.
This instruction is a conditional Jump-to-Subroutine via the address provided in the pipeline register. As shown in figure 4, the machine might have executed words at address 50, 51, and 52. When the contents of address 52 is in the pipeline register the next address control function is the CONDITIONAL JUMP-TO-SUBROUTINE. Here, if the test is passed, the next instruction executed will be the contents of microprogram memory location 90. If the test has failed, the JUMP-TO-SUBROUTINE will not be executed; the contents of microprogram memory location 53 will be executed instead.

Thus, the Conditional Jump-to-Subroutine instruction at location 52 will cause the instruction either in location 90 or in location 53 to be executed next. If the test input is such that the location 90 is selected, value 53 will be pushed onto the internal stack. This provides the return linkage for the machine when the subroutine beginning at location 90 is completed. In this example, the subroutine was completed at location 93 and a RETURN-FROM-SUBROUTINE would be found at location 93.

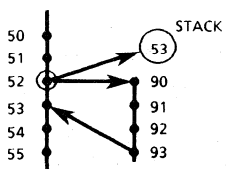


Figure 4: 1 COND JSB PL (CJS)

Instruction 2: Jump-Map.
This is an unconditional instruction which causes the MAP output to be enabled so that the next microinstruction location is determined by the address supplied via the mapping PROMs. Normally, the JUMP MAP instruction is used at the end of the instruction fetch sequence for the machine.

In the example of Figure 5, microinstructions at locations 50,51, 52 and 53 might have been the fetch sequence and at its completion at location 53, the jump map function would be contained in the pipeline register. This example shows the mapping PROM outputs to be 90; therefore, an unconditional jump to microprogram memory address 90 is performed.

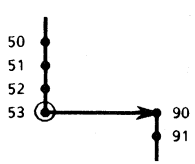


Figure 5: 2 JUMP MAP (JMAP)

Instruction 3: Conditional Jump Pipeline.
This instruction derives its branch address from the pipeline register branch address value (BR_0-BR_{11}). This instruction provides a technique for branching to various microprogram sequences depending upon the test condition inputs. Quite often, state machines are designed which simply execute tests on various inputs waiting for the condition to come true. When the true condition is reached, the machine then branches and executes a set of microinstructions to perform some functions. This usually has the effect of resetting the input under test until some point in the future.

The example shows the conditional jump via the pipeline register address at location 52. When the contents of microprogram memory word 52 are in the pipeline register, the next address will be either location 53 or 30, in this example. If the test is passed, the value currently in the pipeline register (30) will be selected. If the test fails, the next address selected will be contained in the microprogram counter which, in this example, is location 53.

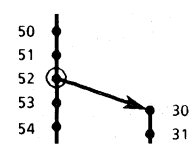


Figure 6: 3 COND JUMP PL (CLP)

Instruction 4: Push/Conditional, Load Counter.
This instruction is used primarily for setting up loops in microprogram firmware. In this example, when instruction 52 is in the pipeline register, a PUSH will be made onto the stack and the counter will be loaded based on the condition. When a PUSH occurs, the value pushed is always the next sequential instruction address. In this case, the address is 53. If the test fails, the counter is not loaded; if it is passed, the counter is loaded with the value contained in the pipeline register branch address field.

Thus, a single microinstruction can be used to set up a loop to be executed a specific number of times. Instruction 8 will describe how to use the pushed value and the register/counter for looping.

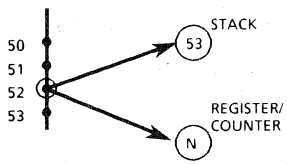


Figure 7: 4 PUSH/COND LD CNTR (PUSH)

Instruction 5: Conditional Jump-to-Subroutine.
This instruction is a Conditional Jump-to-Subroutine via the register/counter of the contents of the PIPELINE register. A PUSH is always performed and one of two subroutines executed. In this example, either the subroutine beginning at address 80 or the subroutine beginning at address 90 will be performed. A RETURN-FROM-SUBROUTINE (instruction number 10) returns the microprogram flow to address 55.

In order for this microinstruction control sequence to operate correctly, both the next address fields of instruction 53 and the next address fields of instruction 54 would have to contain the proper value. Lets assume that the branch address fields of instruction 53 contain the value 90 so that it will be in the MA2910 register/counter when the contents of the address 54 are in the pipeline register.

This requires that the instruction at address 53 loads the register/counter. Now,during the execution of instruction 5 (at address 54), if the test failed, the contents of the register (value = 90) will select the address of the next microinstruction. If the test input passes, the pipeline register contents (value = 80) will determine the address of the next microinstruction. Therefore, this instruction provides the ability to select one of two subroutines to be executed based on a test condition.

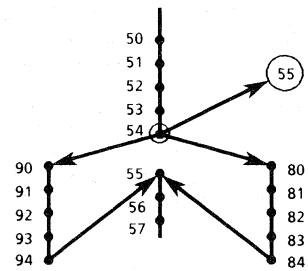


Figure 8: 5 COND JSB R/PL (JSRP)

Instruction 6: Conditional Jump Vector.
This instruction provides the capability to take the branch address from a third source heretofore not discussed. In order for this instruction to be useful, the MA2910 output VECT is used to control a three-state control input of a register, buffer, or PROM containing the next microprogram address. This instruction provides one technique for performing interrupt type branching at the microprogram level. Since this instruction is conditional, a pass causes the next address to be taken from the vector source, while failure causes the next address to be taken from the microprogram counter.

In the example, if the Conditional Jump Vector instruction is contained at location 52, execution will continue at vector address 20 if the $\overline{CC}$ input is LOW and the microinstruction at address 53 will be executed if the $\overline{CC}$ input is HIGH.

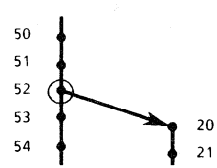


Figure 9: 6 COND JUMP VECTOR (CJV)

Instruction 7: Conditional Jump.
Conditional Jump via the contents of the MA2910 Register/Counter or the contents of the Pipeline register. This instruction is very similar to instruction 5; the Conditional Jump-to-subroutine via R or PL. The major difference between instruction 5 and instruction 7 is that no push onto the stack is performed with 7.

The example depicts this instruction as a branch to one of the two locations depending on the test condition. The example assumes the pipeline register contains the value 70 when the contents of address 52 is being executed. As the contents of address 53 is clocked into the pipeline register, the value 70 is loaded into the register/counter in the MA2910. The value 80 is available when the contents of the address 53 is in the pipeline register. Thus, control is transferred to either address 70 or address 80 depending on the test condition.

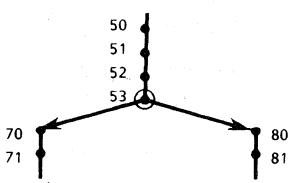


Figure 10: 7 COND JUMP R/PL (JRP)

Instruction 8: Repeat Loop, Counter ≠ Zero.
This microinstruction makes use of the decrementing capability of the register/counter. To be useful, some previous instruction, such as 4, must have loaded a count value into the register/counter. This instruction checks to see whether the register/counter contains a non-zero value. If so, the register/counter is decremented, and the address of the next microinstruction is taken from the top of the stack.

If the register/counter contains zero, the loop exit condition is occurring; control falls through to the next sequential microinstruction by selecting µPC; the stack is POP'd by decrementing the stack pointer, but the contents of the top of the stack are thrown away.

In this example, location 50 is most likely to have contained a Push/Conditional Load Counter instruction which would have caused address 51 to be PUSHed on the stack and the counter to be loaded with the proper value for looping the desired number of times.

In this example, since the loop test is made at the end of the instructions to be repeated (microaddress 54), the proper value to be loaded by the instructions at address 50 is one less than the desires number of passes through the loop.

This method allows a loop to be executed 1 to 4096 times. If it desired to execute the loop from 0 to 4095 times, the firmware should be written to make the loop exit test immediately after loop entry.

Single-microinstruction loops provide a highly efficient capability for executing a specific microinstruction a fixed number of times. Examples include fixed rotates, byte swap, fixed point multiply, and fixed point divide.

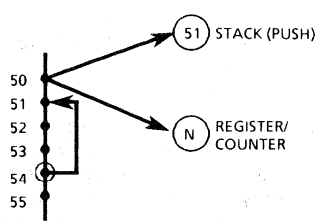


Figure 11: 8 REPEAT LOOP, CNTR ≠ 0 (RFCT)

Instruction 9: Repeat Pipeline Register, Counter ≠ Zero .
This instruction is similar to instruction 8 except that the branch address now comes from the pipeline register rather than the file. In some cases, this instruction may be thought of as a one-word file extension; that is, by using this instruction, a loop with the counter can still be performed when subroutines are nested nine deep. This instruction's operation is very similar to that of instruction 8. The differences are that on this instruction, a failed test condition causes the source of the next microinstruction address to be the D inputs; and, when the test condition is passed, this instruction does not perform a POP because the stack is not being used.

In this example, the REPEAT PIPELINE, COUNTER ≠ ZERO instruction is instruction 52 and is shown as a single microinstruction loop. The address in the pipeline register would be 52. Instruction 51 in this example could be the LOAD COUNTER AND CONTINUE instruction (number 12). While the example shows a single microinstruction loop, by simply changing the address in a pipeline register, multi-instruction loops can be performed in this manner for a fixed number of times as determined by the counter.

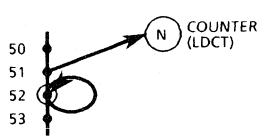


Figure 12: 9 REPEAT PL, CNTR ≠ 0 (RPCT)

Instruction 10: Conditional return form Subroutine.
As the name implies, this instruction is used to branch from the subroutine back to the next microinstruction address following the subroutine call. Since this instruction is conditional, the return is performed only if the test is passed.

If the test is failed, the next sequential microinstruction is performed. This example depicts the use of the conditional RETURN-FROM-SUBROUTINE instruction in both the conditional and the unconditional modes.

This example first shows a JUMP-TO-ROUTINE at instruction location 52 where control is transferred to location 90. At location 93, a conditional RETURN-FROM-SUBROUTINE instruction is performed. If the test is passed, the stack is accessed and the program will transfer to the next instruction at address 53. If the test is failed, the next microinstruction at address 94 will be executed, the program will continue to address 97 where the subroutine is complete. To perform an unconditional RETURN-FROM-SUBROUTINE, the conditional RETURN-FROM-SUBROUTINE instruction is executed unconditionally; the microinstruction at address 97 is programmed to force $\overline{CCEN}$ HIGH, disabling the test and the forced PASS causes an unconditional return.

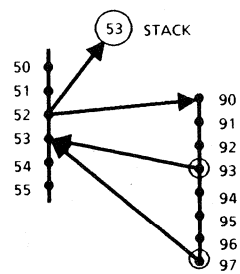


Figure 13: 10 COND RETURN (CRTN)

Instruction 11: Conditional Jump Pipeline register address and POP stack.
This instruction provides another technique for loop termination and stack maintenance. The example shows a loop being performed from address 55 back to address 51. The instructions at locations 52,53, and 54 are all conditional JUMP and POP instructions. At address 52, if the $\overline{CC}$ input is LOW, a branch will be made to address 70 and the stack will be properly maintained via a POP. Should the test fail, the instruction at location 53 (the next sequential instruction) will be executed. Likewise, at address 53, either the instruction at 90 or 54 will be subsequently executed, respective to the test being passed or failed. The instruction at 54 follows the same rules, going to either 80 or 55.

An instruction sequence as described here, using the Conditional Jump Pipeline and POP instruction, is very useful when several inputs are being tested and the microprogram is looping waiting for any of the inputs being tested to occur before proceeding to another sequence of instructions. This provides the powerful jump-table programming technique at the firmware level.

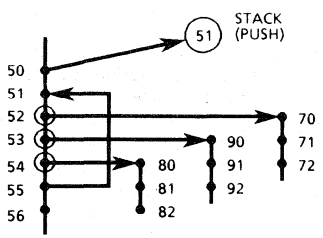


Figure 14: 11 COND JUMP PL & POP (CJPP)

Instruction 12: Load Counter and Continue.
This instruction simply enables the counter to be loaded with the value at its parallel inputs. These inputs are normally connected to the pipeline branch address field which (in the architecture being described here) serves to supply either a branch address or a counter value depending upon the microinstruction being executed.

Altogether there are three ways of loading the counter - the explicit load by this instruction 12; the conditional load included as part of instruction 4; and use of $\overline{RLD}$ input along with any instructions.

The use of $\overline{RLD}$ with any instruction overrides any counting or decrementation specified in the instruction, calling for a load instead. Its use provides additional microinstruction power, at the expense of one bit of microinstruction width.

Instruction 12 is exactly equivalent to the combination of instruction 14 and $\overline{RLD}$ LOW. Its purpose is to provide a simple capability to load the register/counter in those implementations which do not provide microprogrammed control for $\overline{RLD}$.

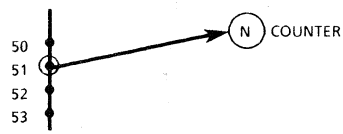


Figure 15: 12 LD CNTR & CONTINUE (LDCT)

Instruction 13: Test End-of-Loop.
This instruction provides the capability of conditionally exiting a loop at the bottom; that is, this is a conditional instruction that will cause the microprogram to loop via the file if the test is failed, else to continue to the next sequential instruction.

The example shows the TEST END-OF-LOOP micro-instruction at address 56. If the test fails, the microprogram will branch to address 52. Address 52 is on the stack because a PUSH instruction had been executed at address 51. If the test is passed at instruction 56, the loop is terminated and the next sequential micro-instruction at address 57 is executed which also causes the stack to be POP'd; thus accomplishing the required stack maintenance.

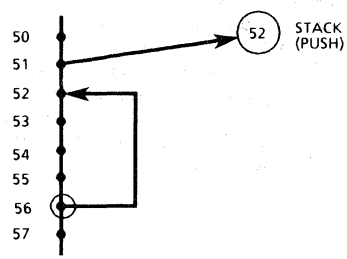


Figure 16: 13 TEST END LOOP (LOOP9

Instruction 14: CONTINUE. This simply causes the microprogram counter to increment so that the next sequential microinstruction is executed. This is the simplest microinstruction of all and should be the default instruction which the firmware requests whenever there is nothing better to do.

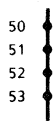


Figure 17: 14 CONTINUE (CONT)

Instruction 15, Three-Way-Branch.
This instruction is the most complex and provides for testing of both a data-dependent condition and the counter during one microinstruction and provides for selecting among one of three microinstruction addresses as the next microinstruction to be performed. Like instruction 8, a previous instruction will have loaded a count into the register/counter while pushing a microbranch address onto the stack.

Instruction 15 performs a decrement-and-branch-until-zero function similar to instruction 8. The next address is taken from the top of the stack until the count reaches zero. When the counter reaches zero the next address comes from the pipeline register. The above action continues as long as the test condition fails. If at any execution of instruction 15 the test condition is passed, no branch is taken and the microprogram counter register furnishes the next address. When the loop is ended, either by a count becoming zero, or by passing the conditional test, the stack is POP'd by decrementing the stack pointer, since interest in the value contained at the top of the stack is then complete.

The application of instruction 15 can enhance performance of a variety of machine-level instructions. For instance, (1) a memory search instruction to be terminated either by finding a desired memory content or by reaching the search limit; (2) variable-field-length arithmetic terminated early upon finding that the content of the portion of the field still unprocessed is all zeroes; (3) key search in a disc controller processing variable length records; (4) normalization of a floating point number.

As one example, consider the case of a memory search instruction. As shown, the instruction at microprogram address 63 can be instruction 4 (PUSH), which will push the value 64 onto the microprogram stack and load the number N, which is one less than the number of memory locations to be searched before ending the search. Location 64 contains a microinstruction which fetches the next operand from the memory area being searched and compares it with the search key. Location 65 contains a microinstruction which tests the result of the comparison and is a THREE-WAY BRANCH for microprogram control. If no match is found, the test fails and the microprogram goes back to location 64 for the next operand address.

When the count becomes zero, the microprogram branches to location 72, and carries out the instruction at location 72, if no match is found. If a match occurs on any execution of the THREE-WAY BRANCH at location 65, control falls through to location 66 which handles the case. Whether the instruction ends by finding a match or not, the stack will have been POP'd once thus removing the value 64 from the top of the stack.

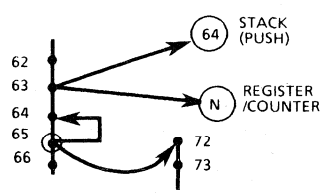


Figure 18: 15 THREE-WAY BRANCH (TWB)

Architecture

One Level Pipeline Based (Recommended)

One level pipeline provides better speed than most other architectures as the Microprogram Memory and the MA2901 array are in parallel paths.

This is the recommended architecture for all MA2900 designs.

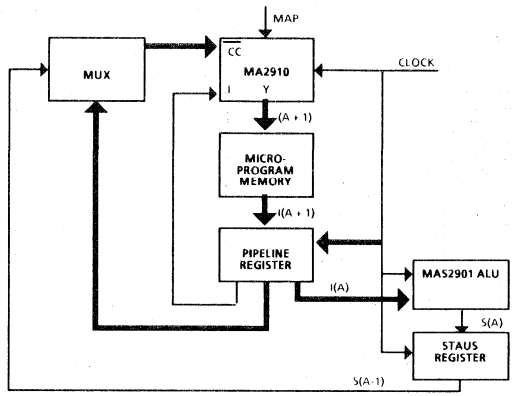


Figure 19: One Level Pipeline Based.

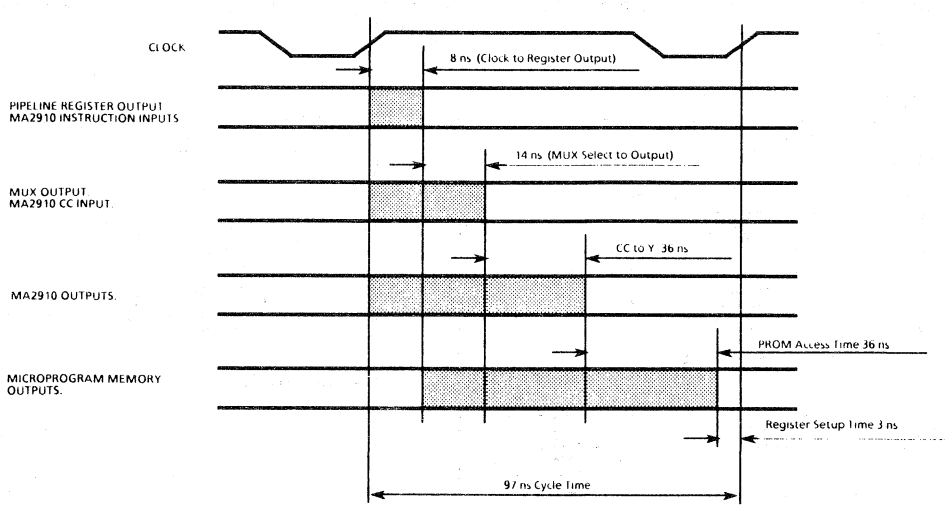


Figure 20: Timing relationships in the CCU.

Instruction Based
A Register at the Microprogram Memory output contains the microinstruction being executed. The Microprogram Memory and MA2901 delay are in series. Conditional branches are executed on the same cycle as the ALU operation generating the condition.

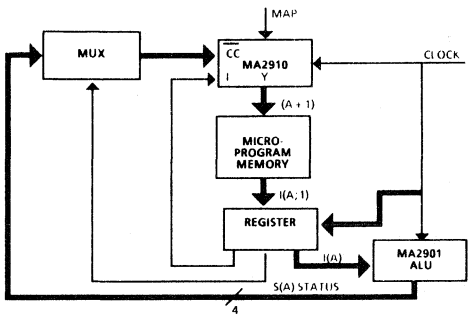


Figure 20: Instruction Based

Address Based
The Register at the MA2910 output contains the microinstruction being executed. The Microprogram Memory and MA2901 are in series within the critical path. This architecture is of comparable speed to the Instruction Based architecture, but requires fewer register bits, since only the address (typically 10 to 12 bits) is stored instead of the instruction.

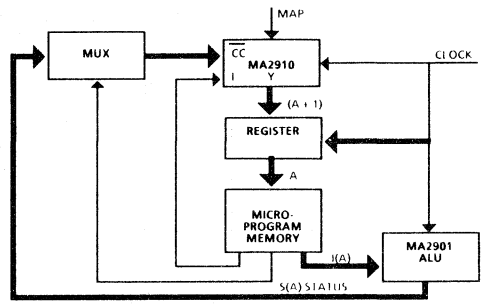


Figure 22: Address Based

Data Based
The Status Register provides conditional branch control based on results of the previose ALU cycle. The Microprogram memory and the MA2901 are in series within the critical path.

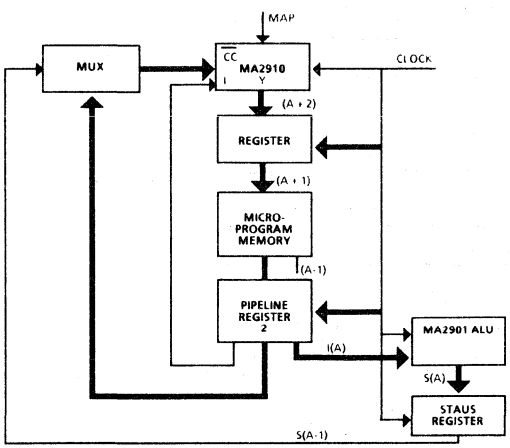


Figure 21: Data Based

Two Level pipeline Based
This architecture provides the highest possible speed. It is, however, more difficult to program as the selection of a microinstruction occurs two instructions ahead of its execution.

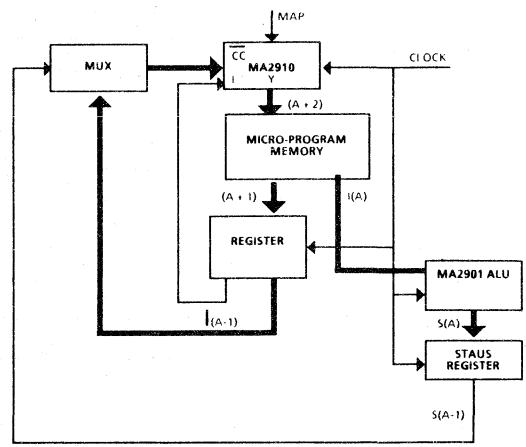


Figure 23: Two Level Pipeline Based

DC Characteristics and Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0.5	10	V
V_I	Input voltage	-0.3	V_{DD} + 0.3	V
-	Current through any pin	-20	+ 20	mA
T_A	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Figure 24: Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4

Symbol	Parameter	Conditions	Total dose radiation not exceeding $3x10^5$ Rad (Si)			Units
			Min.	Typ.	Max.	
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	Input high voltage	-	2.0	-	-	V
V_{IL}	Input low voltage	-	-	-	0.8	V
V_{OH}	Output high voltage	I_{OH} = -2mA	2.4	-	-	V
V_{OL}	Output low voltage	I_{OL} = 5mA	-	-	0.4	V
I_{IN}	Input leakage current (Note 1)	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-	-	± 10	uA
I_{OZ}	Tristate leakage current (Note 1)	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-	-	± 50	uA
I_{DD}	Power supply current	Static, V_{DD} = 5.5V	-	0.1	10	mA

V_{DD} = 5V ± 10%, over full operating temperature range.
Note 1: Worst case at T_A = + 125°C, guarenteed at T_A = -55°C.

Figure 25: Operating Electrical Characteristics

AC Electrical Parameters

1. V_{DD} = 5V ± 10%. C_{CL} = 50pF
2. Operating temperature is specified when ordering (see ordring information section on last page).
3. Enable/Disable times measured to 0.5V change on output voltage level with C_L = 5.0pF
4. Time Measurement Reference Level = 1.5 Volts.
5. Input Pulse = V_{SS} to 3.0 Volts.
6. Set-up and hold times measured relative to CP

Input	t_S	t_h
$D_I \rightarrow R$	17	0
$D_I \rightarrow PC$	27	0
I_0-I_3	32	0
CC	45	0
CCEN	45	0
CI	15	0
RLD	15	0

Figure 26: Set-up and Hold Times

Input	Y	PL, VECT, MAP	FULL
D_0-D_{11}	30	-	-
I_0-I_3	48	30	-
CC	45	-	-
CCEN	45	-	-
CP	60	-	32
OE Enable (Note1.)	18	-	-
OE Disable (Note1.)	18	-	-

Figure 28: Combinational Delays

Minimum Clock LOW Time	20	ns
Minimum Clock HIGH Time	35	ns
Minimum Clock Period	55	ns

Figure 27: Clock Requirements

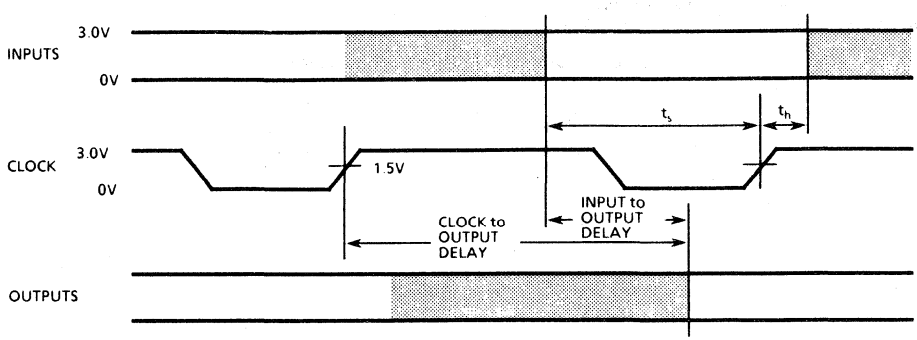


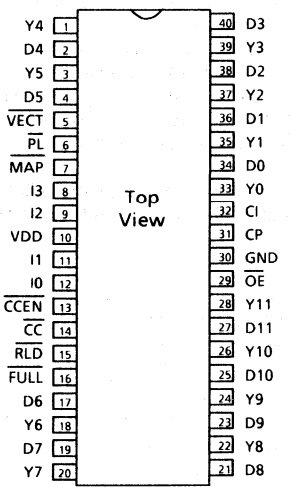
Figure 29: AC Timings

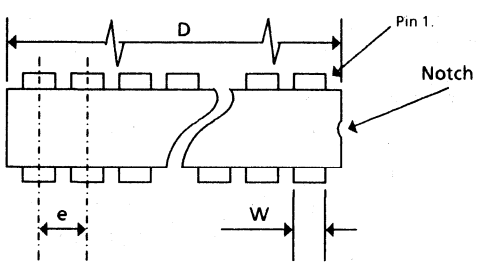
MA2910
Radiation Hard Microprogram Controller

Out lines and Pin Assignments

Ref.	Min.	Nom.	Max.
A			5.60 (0.220)
A_1	0.38 (0.015)		1.53 (0.060)
b	0.35 (0.014)		0.59 (0.023)
c	0.20 (0.008)		0.36 (0.014)
D			51.31 (2.020)
e		2.54 (0.100) typ	
e_1		15.24 (0.600) typ	
H	4.71 (0.185)		5.38 (0.212)
M_E			15.90 (0.626)
Dimensions in mm (inches)			

MEDL XG405





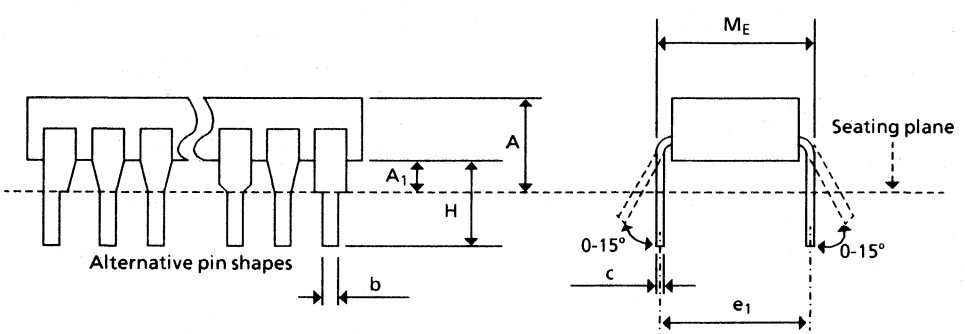


Figure 30: 40-Lead Ceramic DIL (solder seal) - package style C

GEC PLESSEY
SEMICONDUCTORS

RadiationTolerance

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

Total Dose (Function to specification)	3×10^5 Rad(Si)
Transient Upset (survivability)	$>10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	1×10^5 neutrons/cm^2
Single Event Upset (GSO 10% worst case)	$<10^{-10}$ errors/bitday
Latch-up	Not possible

Table 32: Radiation Hardness Parameters

Ordering Information

Unique circuit designator.

MAx2910xxxxx

Radiation Tolerance

S Radiation hard processing
R 100 kRads (Si) guaranteed
Q 300 kRads (Si) guaranteed

Package Type

C Ceramic DIL
N Naked Die

QA/QCI Process
(see section 9, part 4)

Test Process
(see section 9, part 3)

Assembly Process
(see section 9, part 2)

Reliability Level

L Rel 0
C Rel 1
D Rel 2
E Rel 3/4/5/STACK
B Class B
S Class S

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.

section 5
MEMORIES

GEC PLESSEY

SEMICONDUCTORS

MA5101

Radiation Hard 256x4 Bit Static RAM

S10304FDS Issue 1.2 October 1990

Features

- 3µm CMOS-SOS technology
- Latch-up free
- Fast access time 90ns typical
- Total dose 10^5 rad (Si)
- Transient upset > 10^{10} rad (Si) /sec
- SEU < 10^{-10} errors/bit day
- Single 5V supply
- All Inputs & outputs fully TTL & CMOS compatible
- Fully static operation
- Three state output
- Low standby current 10µA typical
- -55°C to + 125°C operation

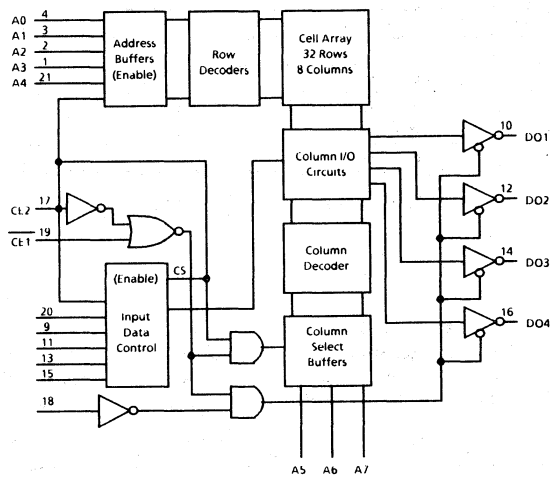


Figure 1: Block Diagarm

General Description

The MA5101 1k Static RAM is configured as 256x4 bits and manufactured using MEDL's CMOS-SOS high performance, radiation hard, 3µm technology.

The device has separate input and output terminals. An output disable function is provided so that data inputs and outputs may be wire OR'ed for use in common data I/O systems. The design uses a 6 transistor cell and has full static operation with no clock or timing strobe required. Address input buffers are deselected when CE2 is in the low state and minimum standby current is drawn.

$\overline{CE1}$	CE2	OD	R/$\overline{W}$	D_{in}	Output	Mode
H	X	I_{SBI}	X	I_{SBI}	High Z	Not selected
L	H	I_{DD}	H	I_{DD}	D_{OUT}	Read
L	L	I_{DD}	L	I_{DD}	High Z	Write
H	X	I_{SBI}	X	I_{SBI}	High Z	Not selected
L	H	I_{DD}	H	I_{DD}	D_{OUT}	Read
L	L	I_{DD}	L	I_{DD}	High Z	Write

Table 1: Truth Table

5

DC Characteristics & Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0.5	7	V
V_I	Input voltage	-0.3	V_{DD} + 0.3	V
T_A	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Table 2: Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes for tables 3 & 4:
1. The characteristics shown apply to pre radiation at T_A = -55°C to + 125°C with V_{DD} = 5V ± 10% and to post 100kRad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ± 10%.
2. Worst case at T_A = + 125°C, guaranteed but not tested at T_A = -55°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	Input high voltage	-	$V_{DD}/2$	-	V_{DD}	V
V_{IL}	Input low voltage	-	V_{SS}	-	0.8	V
V_{OH}	Output high voltage	I_{OH} = -1.0mA	2.4	-	-	V
V_{OL}	Output low voltage	I_{OL} = 2mA	-	-	0.4	V
I_{LI}	Input leakage current (note 2)	V_{IN} = V_{DD} or V_{SS} on all inputs	-	-	± 10	uA
I_{LO}	Output leakage current (note 2)	CE1 = $V_{DD}/2$, V_{OUT} = 0 to V_{DD}	-	-	± 20	uA
I_{DD}	Dynamic operating current	CE1<0.80V, f_{RC} = 1MHz, CE2, A_{0-7} switching, ouputs open, all other inputs V_{DD}	-	10	15	mA
I_{SB}	Standby supply current	CE2<0.2V	-	10	500	uA

Table 3: DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DR}	V_{CC} for Data Retention	CE2<0.2V	2.0	-	-	V
I_{DDR}	Data Retention Current	CE2<0.2V, V_{DR} = 2.0V	-	5	250	µA

Table 4: Data Retention Characteristics

MA5101

Radiation Hard 256x4 Bit Static RAM

AC Electrical Characteristics

Notes for tables 5 & 6:

1. The characteristics shown apply to pre radiation at T_A = -55°C to + 125°C with V_{DD} = 5V ± 10% and to post 100kRad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ± 10%.
2. Input pulse = V_{SS} to 3.0V.
3. Times measurement reference level = 1.5V.
4. Input Rise and Fall times ≤ 5ns.
5. Output load 1TTL gate and CL = 60pF.

Symbol	Parameter	Min.	Max.	Units
t_{KC}	Read Cycle Time	140	-	ns
t_A	Access Time	-	130	ns
t_{CO1}	Chip Enable $\overline{CE1}$ to Output	-	140	ns
t_{CO2}	Chip Enable CE2 to Output	-	140	ns
t_{OD}	Output Disable to Output	10	70	ns
t_{DF}	Output Disable to High Z State	10	50	ns
t_{OH1}	Previous Data Read Valid with respect to Address Change	0	-	ns
t_{OH2}	Previous Data Read Valid with respect to Chip Enable	0	-	ns

Table 5: Read Cycle AC Electrical Characteristics

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Write Cycle Time	140	-	ns
t_{CW1}	Chip Enable $\overline{CE1}$ to Write	80	-	ns
t_{CW2}	Chip Enable CE2 to Write	80	-	ns
t_{AW}	Write Delay	20	-	ns
t_{DW}	Data Set Up Time	30	-	ns
t_{DH}	Data Hold	0	-	ns
t_{WR}	Write Recovery Time	0	-	ns
t_{WP}	Write Recovery	0	20	ns
t_{DS}	Output Disable Set Up	20	-	ns

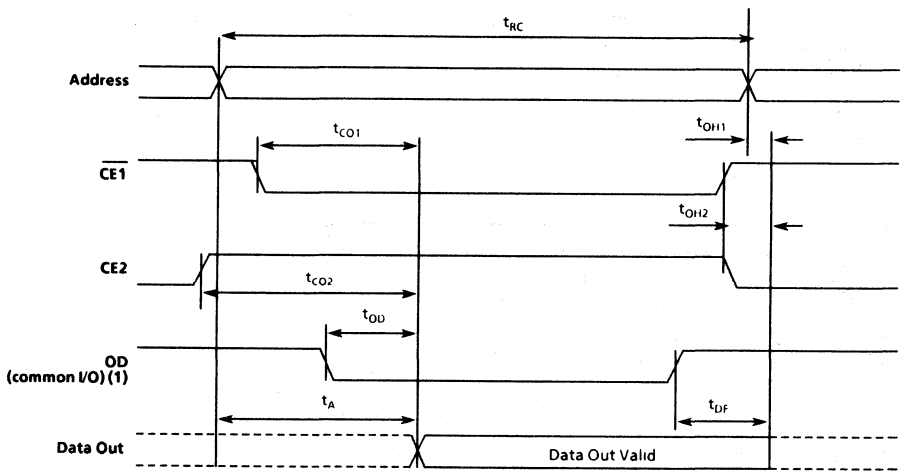
Table 6: Write Cycle AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	6	10	pF
C_{OUT}	Output Capacitance	V_O = 0V	-	8	12	pF

Note: T_A = 25°C and f = 1MHz

Table 7: Capacitance

Timing Waveforms



1. OD may be tied low for separate I/O operation.
2. During write cycle, OD is HIGH for common I/O and "DONT CARE" for separate I/O operation.

Figure 2: Read Cycle Timing Waveforms

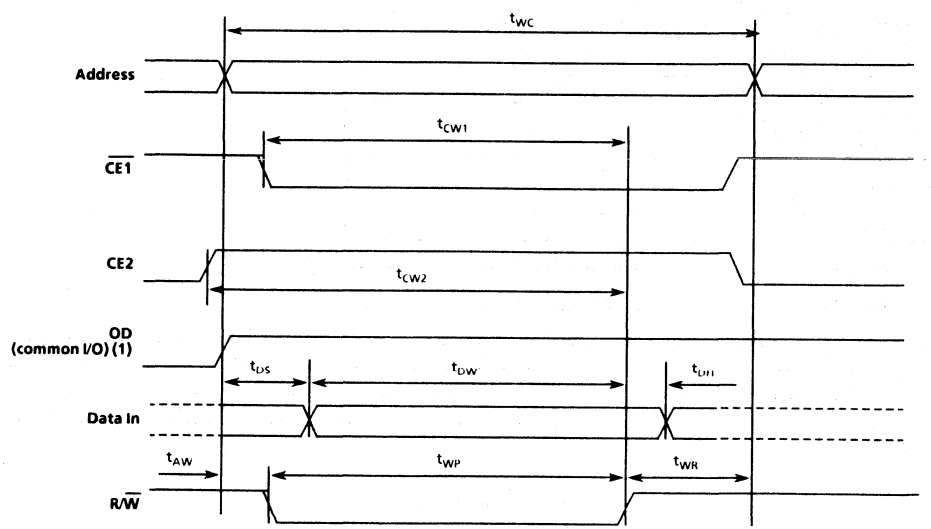
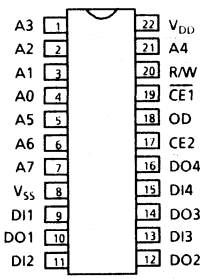


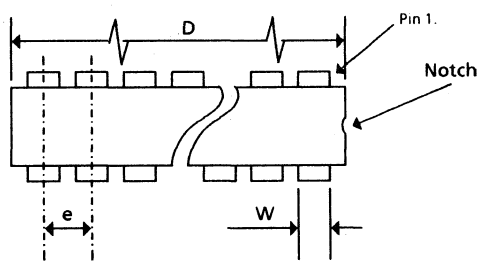
Figure 3: Read Cycle 2 Timing Waveforms

MA5101

Radiation Hard 256x4 Bit Static RAM

Pin Assignment & Package Outline





Ref.	Min.	Nom.	Max.
A	-	-	5.60 (0.220)
A_1	0.38 (0.015)	-	1.53 (0.060)
b	0.35 (0.014)	-	0.59 (0.023)
c	0.20 (0.008)	-	0.36 (0.014)
D	-	-	27.94 (1.100)
e	-	2.54(0.100) typ.	-
e_1	-	10.16 (0.400) typ.	-
H	4.71 (0.185)	-	5.38 (0.212)
M_E	-	-	17.95 (0.313)
Z	-	-	1.27 (0.050)
W	-	-	1.53 (0.060)
Dimensions in mm (inches)			

MEDL XG462

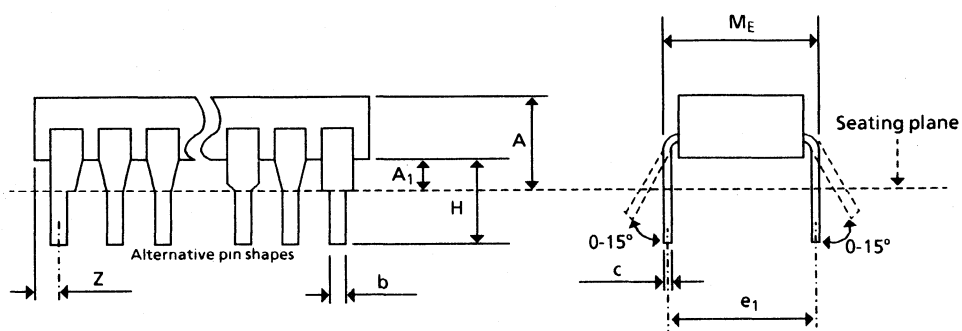


Figure 4a & b. 22-Lead Ceramic DIL (solder seal) - package style C

RadiationTolerance

Total Dose (Function to specification)	$1x10^5$ Rad(Si)
Transient Upset (suvivability)	$>10^{10}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>10^{15}$ neutrons/cm^2
Single Event Upset (GSO 10% worst case)	$<10^{-10}$ errors/bitday
Latch-up	Not possible

Table 8: Radiation Tolerance

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

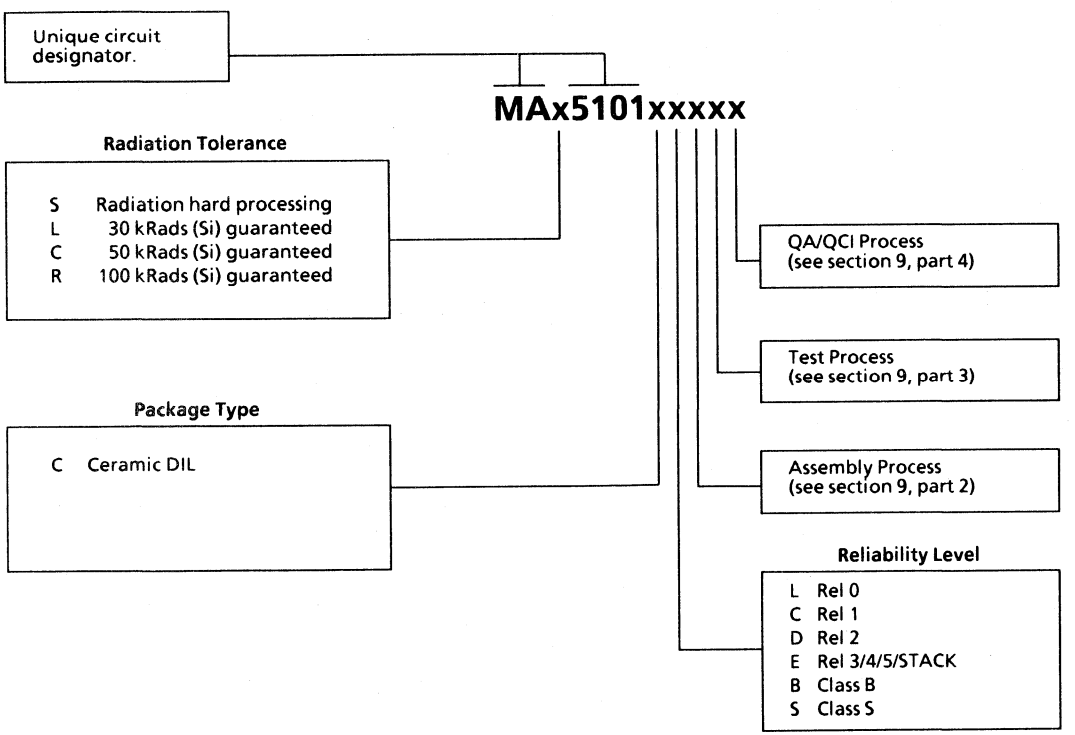
Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

MA5101

Radiation Hard 256x4 Bit Static RAM

Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



GEC PLESSEY

SEMICONDUCTORS

MA5104

Radiation Hard 4096x1 Bit Static RAM

C10305FDS Issue 1.3 October 1990

Features

- 3µm CMOS-SOS technology
- Latch-up free
- Fast access time 90ns typical
- Total dose 10^5 rad (Si)
- Transient upset $5x10^{10}$ rad (Si) /sec
- SEU $3.1x10^{-10}$ errors/bit day
- Single 5V supply
- All Inputs & outputs fully TTL & CMOS compatible
- Fully static operation
- Three state output
- Low standby current 10µA typical
- -55°C to + 125°C operation

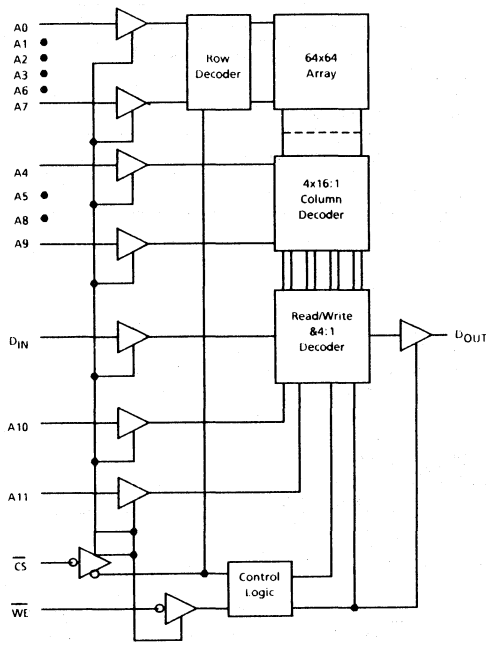


Figure 1: Block Diagarm

General Description

The MA5104 4k Static RAM is configured as 4096x1 bits and manufactured using MEDL's CMOS-SOS high performance, radiation hard, 3µm technology.

The device has separate input and output terminals controlled by Chip Select and Write Enable. The design uses a 6 transistor cell and has full static operation with no clock or timing strobe required. Address input buffers are deselected when Chip Select is in the HIGH state.

$\overline{CS}$	$\overline{WE}$	Mode	Output Pin
H	H	Not selected	High Z
H	L	Not selected	High Z
L	H	Selected (Read)	Data out
L	L	Selected (Write)	High Z

Table 1: Truth Table

5

DC Characteristics & Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0.5	8	V
V_I	Input voltage	-0.3	V_{DD} + 0.3	V
T_A	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Table 2: Absolute Maximum Ratings

Notes for tables 3 & 4:
1. The characteristics shown apply to pre radiation at T_A = -55°C to + 125°C with V_{DD} = 5V ± 10% and to post 100kRad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ± 10%.
2. Worst case at T_A = + 125°C, guaranteed but not tested at T_A = -55°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	Input high voltage	-	$V_{DD}/2$	-	V_{DD}	V
V_{IL}	Input low voltage	-	V_{SS}	-	0.8	V
V_{OH}	Output high voltage	I_{OH} = -1mA	2.4	-	-	V
V_{OL}	Output low voltage	I_{OL} = 2mA	-	-	0.4	V
I_{LI}	Input leakage current (note 2)	All inputs except $\overline{CS}$	-	-	± 10	uA
I_{OZ}	Output leakage current (note 2)	Output disabled, $V_{OUT} = V_{SS}$ or V_{DD}	-	-	± 20	uA
I_{PUI}	Input pull-up current	$V_{IN} = V_{SS}$ on $\overline{CS}$ input only	-	-	-100	uA
I_{PDI}	Input leakage current	$V_{IN} = V_{SS}$ on $\overline{CS}$ input only	-	-	5	uA
I_{DDL}	Standby supply current	Chip disabled	-	50	1000	uA
I_{DD}	Power supply current	f_{RC} = 1MHz, $\overline{CS}$ = 50% mark:space	-	12	16	mA

Table 3: DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DR}	V_{CC} for Data Retention	$\overline{CS} = V_{DR}$	2.0	-	-	V
I_{DDR}	Data Retention Current	$\overline{CS} = V_{DR}$, V_{DR} = 2.0V	-	30	500	µA

Table 4: Data Retention Characteristics

MA5104

Radiation Hard 4096x1 Bit Static RAM

AC Electrical Characteristics

Notes for tables 5 & 6:

1. The characteristics shown apply to pre radiation at T_A = -55°C to + 125°C with V_{DD} = 5V ± 10% and to post 100kRad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ± 10%.
2. Input pulse = V_{SS} to 3.0V.
3. Times measurement reference level = 1.5V.
4. Input Rise and Fall times ≤ 5ns.
5. Transition is measured at ± 500mV from steady state. This parameter is sampled and not 100% tested.
6. Input Rise and Fall times ≤ 5ns.

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Read Cycle Time	135	-	ns
t_A	Access Time	-	135	ns
t_{CA}	Chip select to output valid	-	135	ns
$t_{CX\ (note\ 4)}$	Chip select to output active	10	-	ns
t_{COT}	Chip select to output THREE STATE	10	50	ns
t_{OHA}	Output Hold from address change	10	-	ns

Table 5: Read Cycle AC Electrical Characteristics

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Write Cycle Time	135	-	ns
t_{AW}	Address to Write set up time	10	-	ns
t_{WP}	Write pulse width	50	-	ns
t_{WR}	Write Recovery Time	5	-	ns
t_{WP}	Data Set Up Time	35	-	ns
t_{DH}	Data hold time	5	-	ns
t_{WOT}	Write Enable to output THREE STATE	10	50	ns

Table 6: Write Cycle AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	6	10	pF
C_{OUT}	Output Capacitance	V_O = 0V	-	8	12	pF

Note: T_A = 25°C and f = 1MHz

Table 7: Capacitance

Timing Waveforms

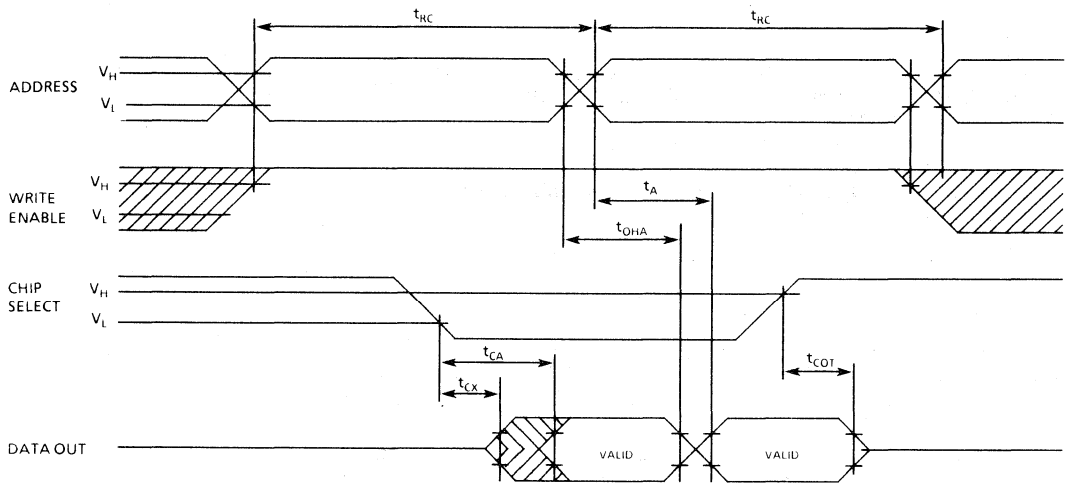


Figure 3: Read Cycle Switching Time Waveforms

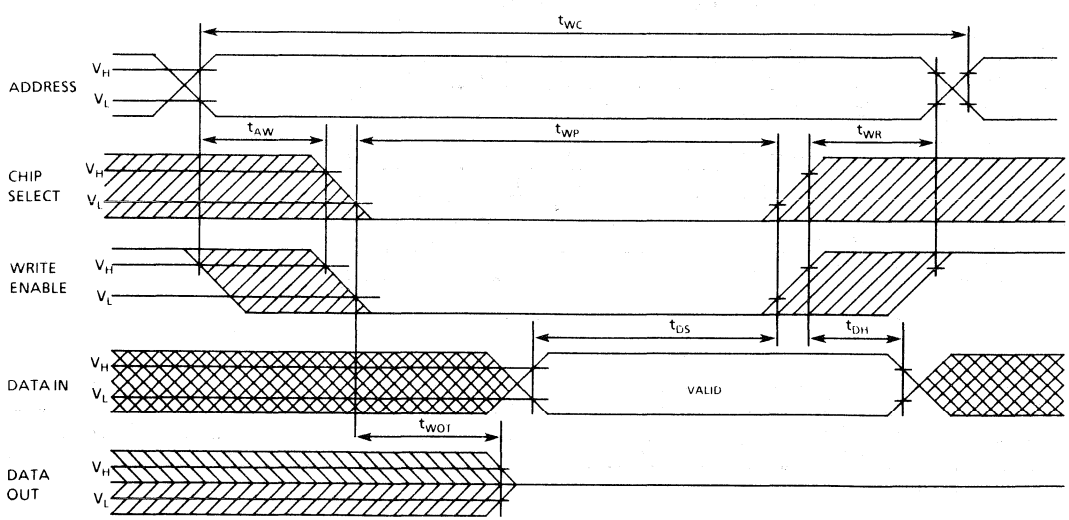
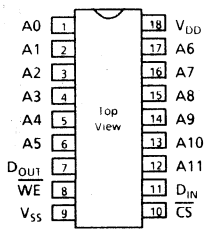


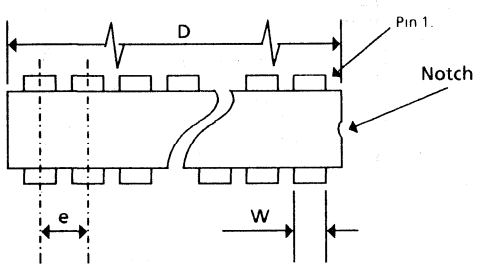
Figure 4: Write Cycle Switching Time Waveforms

MA5104

Radiation Hard 4096x1 Bit Static RAM

Pin Assignment & Package Outlines





Ref.	Min.	Nom.	Max.
A			0.220
A_1	0.015		0.060
b	0.014		0.023
c	0.008		0.014
D			0.910
e		0.100 typ	
e_1		0.300 typ	
H	0.175		0212
M_E			0.326
Dimensions in inches			

MEDL XG406

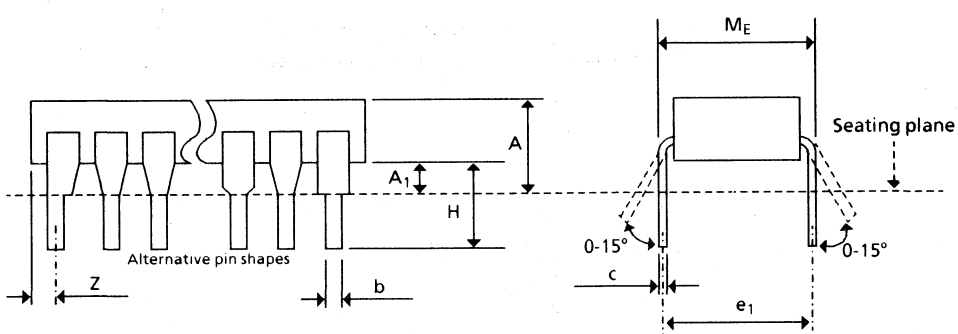
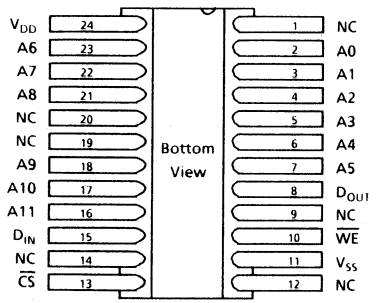


Figure 4a & b. 18-Lead Ceramic DIL (solder seal) - package style C



Ref.	Min.	Nom.	Max.
A			2.67 (0.105)
A_1	0.25 (0.010)		1.02 (0.040)
b	0.38 (0.015)		0.48 (0.019)
c	0.10 (0.004)		0.18 (0.007)
D	14.86 (0.585)		15.62 (0.615)
e		2.54 (0.050)	
L	6.73 (0.265)		7.75 (0.305)
M	9.91 (0.390)		10.41 (0.410)
M_L	7.6 (0.30)		
Z	0.13 (0.005)		1.14 (0.045)

Dimensions in mm (inches)

MEDL XG472

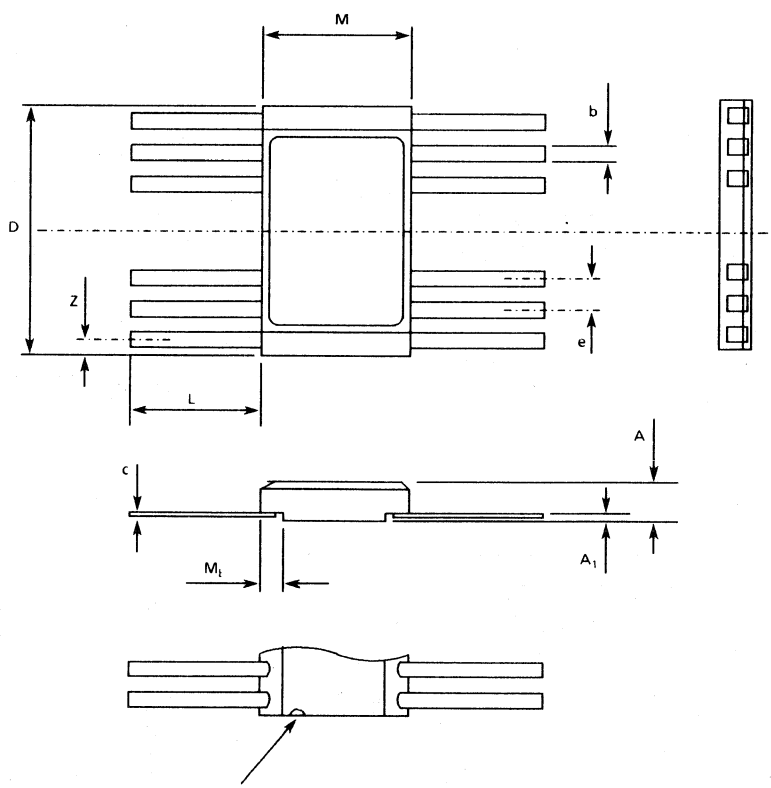


Figure 5a & b: 24 lead Ceramic Flatpack(solder seal)
Package style F

MA5104

Radiation Hard 4096x1 Bit Static RAM

RadiationTolerance

Total Dose (Function to specification)	$1x10^5$ Rad(Si)
Transient Upset (survivability)	$5x10^{10}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>10^{15}$ neutrons/cm^2
Single Event Upset (GSO 10% worst case)	$3.1x10^{-10}$ errors/bitday
Latch-up	Not possible

Table 8: Radiation Tolerance

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

5

Ordering Information

Unique circuit designator.

MAx5104xxxxx

Radiation Tolerance

- S Radiation hard processing
- L 30 kRads (Si) guaranteed
- C 50 kRads (Si) guaranteed
- R 100 kRads (Si) guaranteed

Package Type

- C Ceramic DIL
- F Flatpack (solder seal)

QA/QCI Process (see section 9, part 4)

Test Process (see section 9, part 3)

Assembly Process (see section 9, part 2)

Reliability Level

- L Rel 0
- C Rel 1
- D Rel 2
- E Rel 3/4/5/STACK
- B Class B
- S Class S

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.

MA5114

Radiation Hard 1024x4 Bit Static RAM

S10306FDS Issue 1.4 October 1990

Features

- 3µm CMOS-SOS technology
- Latch-up free
- Fast access time 90ns typical
- Total dose 10^5 rad (Si)
- Transient upset $5x10^{10}$ rad (Si) /sec
- SEU $3.1x10^{-10}$ errors/bit day
- Single 5V supply
- All Inputs & outputs fully TTL & CMOS compatible
- Fully static operation
- Three state output
- Low standby current 50µA typical
- -55°C to + 125°C operation
- Data retention at 2V supply.

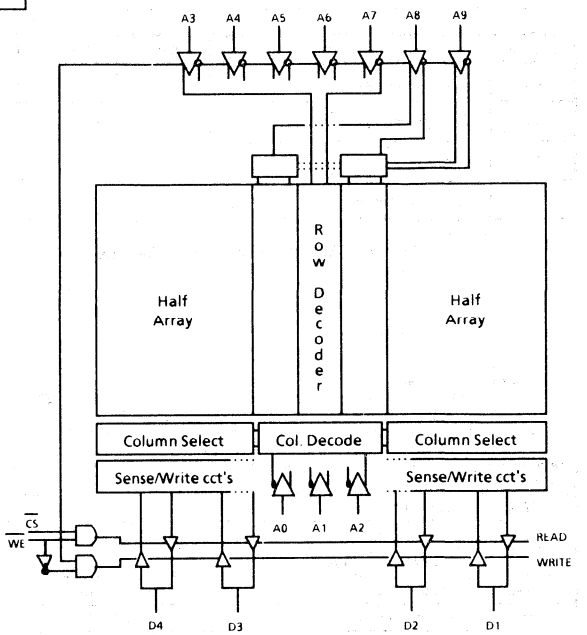


Figure 1: Block Diagarm

General Description

The MA5114 4k Static RAM is configured as 1024x4bits and manufactured using MEDL's CMOS-SOS high performance, radiation hard, 3µm technology.

The design uses a 6 transistor cell and has full static operation with no clock or timing strobe required. Address input buffers are deselected when Chip Select is in the HIGH state.

$\overline{CS}$	$\overline{WE}$	Mode	I/O Pin
H	H	Not selected	High Z
H	L	Not selected	High Z
L	H	Selected (Read)	Data out
L	L	Selected (Write)	Data in

Table 1: Truth Table

Radiation Hard 1024x4 Bit Static RAM

DC Characteristics & Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0.5	8	V
V_I	Input voltage	-0.3	V_{DD} + 0.3	V
T_A	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Table 2: Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes for tables 3 and 4:
1. The characteristics shown apply to pre radiation at T_A = -55°C to + 125°C with V_{DD} = 5V ± 10% and to post 100kRad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ± 10%.
2. Worst case at T_A = + 125°C, guaranteed but not tested at T_A = -55°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	Input high voltage	-	$V_{DD}/2$	-	V_{DD}	V
V_{IL}	Input low voltage	-	V_{SS}	-	0.8	V
V_{OH}	Output high voltage	I_{OH} = -1mA	2.4	-	-	V
V_{OL}	Output low voltage	I_{OL} = 2mA	-	-	0.4	V
I_{LI}	Input leakage current (note 2)	All inputs except $\overline{CS}$	-	-	± 10	uA
I_{OZ}	Output leakage current (note 2)	Output disabled, $V_{OUT} = V_{SS}$ or V_{DD}	-	-	± 20	uA
I_{PUI}	Input pull-up current	$V_{IN} = V_{SS}$ on $\overline{CS}$ input only	-	-	-100	uA
I_{PDI}	Input leakage current	$V_{IN} = V_{SS}$ on $\overline{CS}$ input only	-	-	5	uA
I_{DDL}	Standby supply current	Chip disabled	-	50	1000	uA
I_{DD}	Power supply current	f_{RC} = 1MHz, $\overline{CS}$ = 50% mark:space	-	12	16	mA

Table 3: DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DR}	V_{CC} for Data Retention	$\overline{CS} = V_{DR}$	2.0	-	-	V
I_{DDR}	Data Retention Current	$\overline{CS} = V_{DR}$, V_{DR} = 2.0V	-	30	500	µA

Table 4: Data Retention Characteristics

AC Electrical Characteristics

Notes for tables 5 and 6:
1. The characteristics shown apply to pre radiation at T_A = -55°C to + 125°C with V_{DD} = 5V ± 10% and to post 100kRad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ± 10%.
2. Input pulse = V_{SS} to 3.0V.
3. Times measurement reference level = 1.5V.
4. Input Rise and Fall times ≤ 5ns.
5. Transition is measured at ± 500mV from steady state. This parameter is sampled and not 100% tested.
6. Input Rise and Fall times ≤ 5ns.

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Read Cycle Time	135	-	ns
t_A	Access Time	-	135	ns
t_{CA}	Chip select to output valid	-	135	ns
t_{CX} (note 4)	Chip select to output active	10	-	ns
t_{COT} (note 4)	Chip select to output Tri State	10	50	ns
t_{OHA}	Output Hold from address change	10	-	ns

Table 5: Read Cycle AC Electrical Characteristics

5

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Write Cycle Time	135	-	ns
t_{AW}	Address to Write set up time	10	-	ns
t_{WP}	Write pulse width	50	-	ns
t_{WR}	Write Recovery Time	5	-	ns
t_{DS}	Data Set Up Time	35	-	ns
t_{DH}	Data hold time	5	-	ns
t_{WOT} (note 5)	Write Enable to output Tri State	10	50	ns
t_{CW}	Chip Selection to Write Low	25	-	ns

Table 6: Write Cycle AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	6	10	pF
C_{OUT}	Output Capacitance	V_O = 0V	-	8	12	pF

Note: T_A = 25°C and f = 1MHz

Table 7: Capacitance

Timing Waveforms

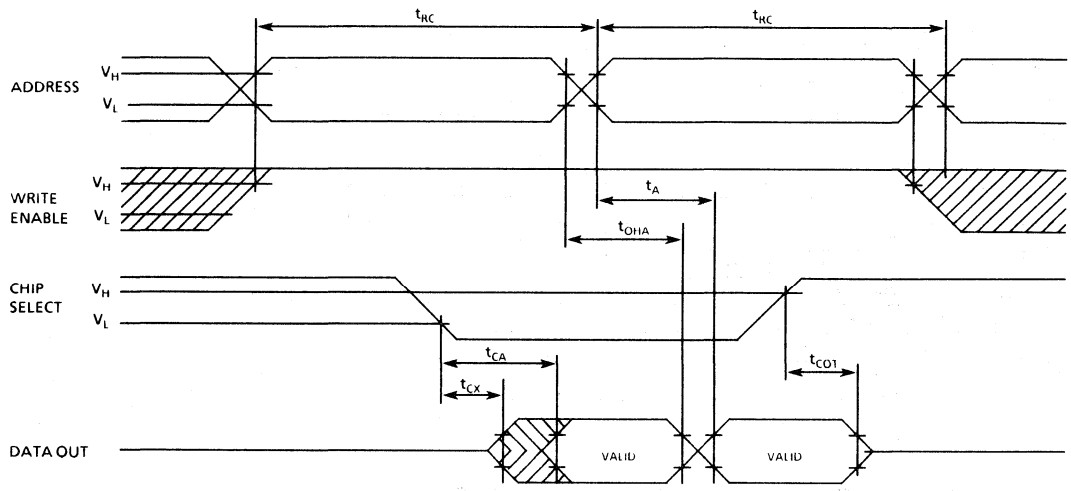


Figure 3: Read Cycle Switching Time Waveforms

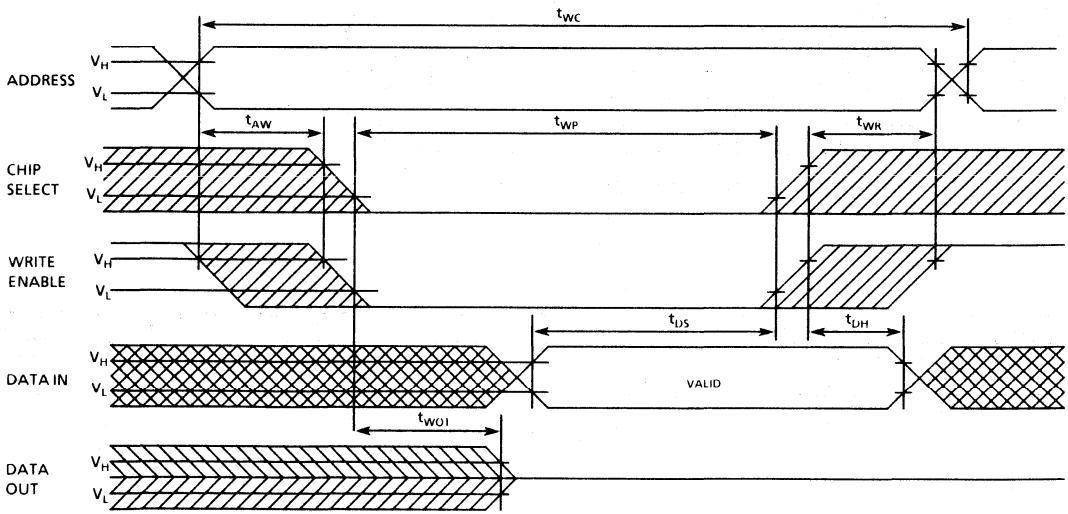
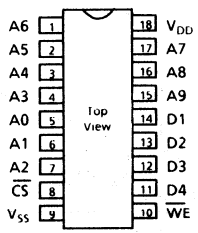


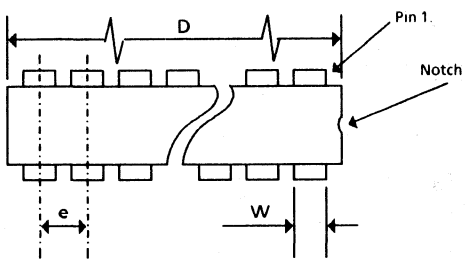
Figure 4: Write Cycle Switching Time Waveforms

MA5114

Radiation Hard 1024x4 Bit Static RAM

Pin Assignment & Package Outlines





Ref.	Min.	Nom.	Max.
A			0.220
A_1	0.015		0.060
b	0.014		0.023
c	0.008		0.014
D			0.910
e		0.100 typ	
e_1		0.300 typ	
H	0.175		0212
M_L			0.326

Dimensions in inches

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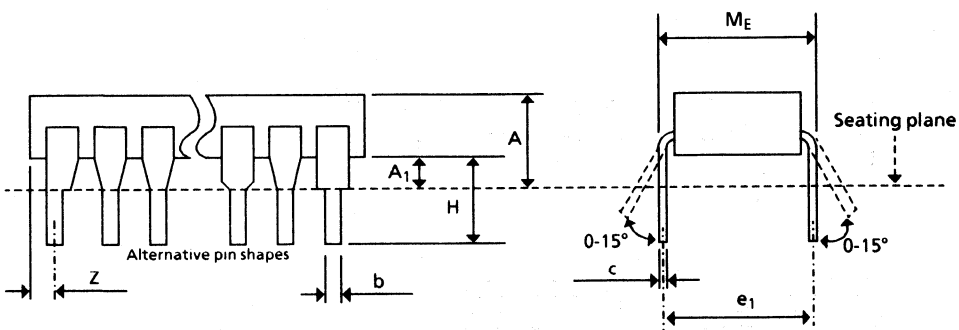
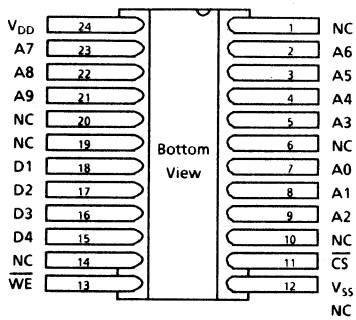


Figure 4a and 4b: 18-Lead Ceramic DIL (solder seal) - package style C

Radiation Hard
1024X4 Bit Static RAM



Ref.	Min.	Nom.	Max.
A			2.67 (0.105)
A_1	0.25 (0.010)		1.02 (0.040)
b	0.38 (0.015)		0.48 (0.019)
c	0.10 (0.004)		0.18 (0.007)
D	14.86 (0.585)		15.62 (0.615)
e		2.54 (0.050)	
L	6.73 (0.265)		7.75 (0.305)
M	9.91 (0.390)		10.41 (0.410)
M_E	7.6 (0.30)		
Z	0.13 (0.005)		1.14 (0.045)
Dimensions in mm (inches)			

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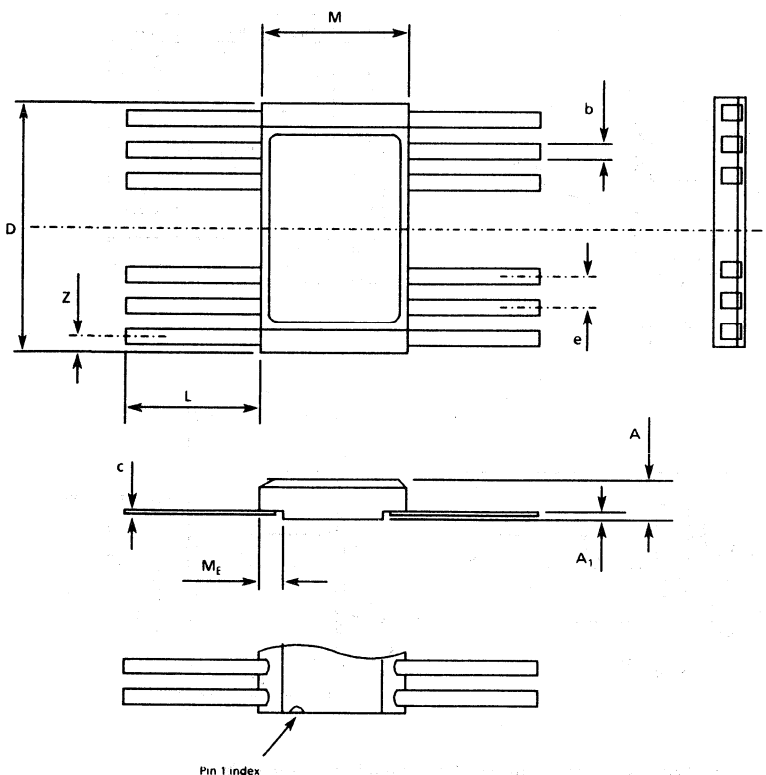
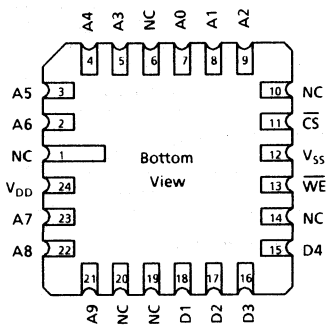
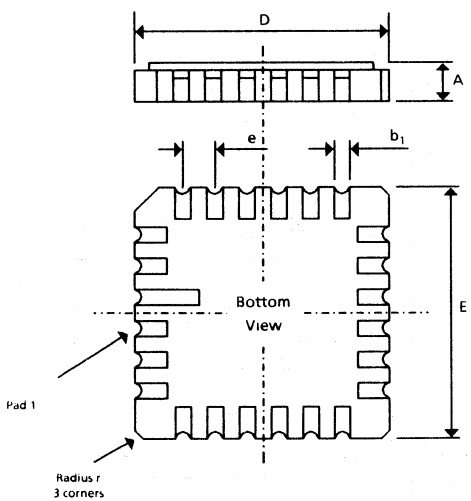


Figure 5a and 5b: 24 lead Ceramic Flatpack(solder seal)
Package style F

MA5114

Radiation Hard 1024X4 Bit Static RAM





Ref.	Min.	Nom.	Max.
A			2.16 (0.096)
b_1		0.51 (0.020)	
D	(0.345)		12.57 (0.355)
E	(0.345)		12.57 (0.355)
e		1.02 (0.040)	
r		0.19 (0.0075)	
Dimensions in mm (inches)			

MEDL XG470

Figure 6a and 6b: 24-pad Leadless Chip Carrier (Package style L)

RadiationTolerance

Total Dose (Function to specification)	$1x10^5$ Rad(Si)
Transient Upset (survivability)	$5x10^{10}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>10^{15}$ neutrons/cm^2
Single Event Upset (GSO 10% worst case)	$3.1x10^{-10}$ errors/bitday
Latch-up	Not possible

Table 8: Radiation Tolerance

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

Ordering Information

Unique circuit designator.

MAx5114xxxxx

Radiation Tolerance

- S Radiation hard processing
- L 30 kRads (Si) guaranteed
- C 50 kRads (Si) guaranteed
- R 100 kRads (Si) guaranteed

Package Type

- C Ceramic DIL
- F Flatpack (solder seal)
- L Leadless Chip Carrier

QA/QCI Process
(see section 9, part 4)

Test Process
(see section 9, part 3)

Assembly Process
(see section 9, part 2)

Reliability Level

- L Rel 0
- C Rel 1
- D Rel 2
- E Rel 3/4/5/STACK
- B Class B
- S Class S

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.

GEC PLESSEY

SEMICONDUCTORS

MA6116/6216

Radiation Hard 2048x8 Bit Static RAM

S10307FDS Issue 1.5 October 1990

Features

- 3μm CMOS-SOS technology
- Latch up free
- Fast access time 110ns (MA6116) and 85ns (MA6216) typical
- Total dose $1.5x10^5$ rad (Si)
- Transient upset $5x10^{10}$ rad (Si) /sec
- SEU $3.6x10^{-9}$ errors / bitday
- Single 5V supply
- TTL and CMOS compatible inputs
- Fully static operation
- Three state output
- Low standby current 100μA typical
- -55°C to + 125°C operation
- Data retention at 2V supply

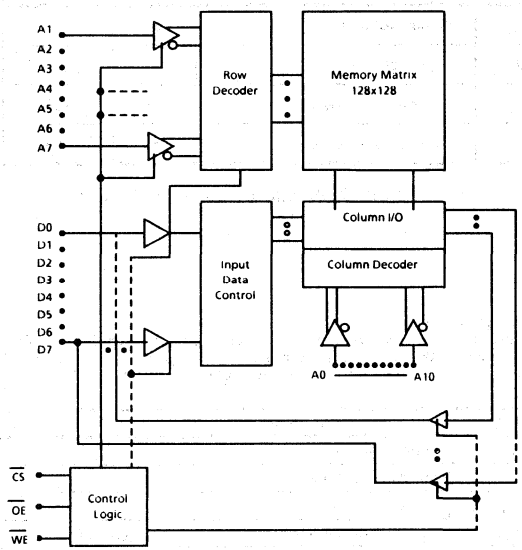


Figure 1: Block Diagram

General Description

The MA6116 16k Static RAM is configured as 2048x8 bits and manufactured using MEDL's CMOS-SOS high performance, radiation hard, 3μm technology. The MA6216 is manufactured using 2.5μm technology resulting in faster performance

The design uses a 6 transistor cell and has full static operation with no clock or timing strobe required. Address input buffers are deselected when chip select is in the HIGH state.

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{DD} Current	Output
H	X	X	Not selected	I_{DDI}	High Z
L	L	H	Read	I_{DD}	D_{out}
L	H	L	Write	I_{DD}	D_{in}
L	L	L	Write	I_{DD}	D_{in}

Table 1: Truth Table

5

DC Characteristics & Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0.5	8	V
V_I	Input voltage	-0.3	V_{DD} + 0.3	V
T_A	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Table 2: Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes for tables 3 and 4:
1 The characteristics shown apply to pre radiation at T_A = -55°C to + 125°C with V_{DD} = 5V ± 10% and to post 100kRad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ± 10%.
2. Worst case at T_A = + 125°C, guaranteed but not tested at T_A = -55°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	Input high voltage	-	$V_{DD}/2$	-	V_{DD}	V
V_{IL}	Input low voltage	-	V_{SS}	-	0.8	V
V_{OH}	Output high voltage	I_{OH} = -1mA	2.4	-	-	V
V_{OL}	Output low voltage	I_{OL} = 4mA	-	-	0.4	V
I_{LI}	Input leakage current (note 2)	All inputs except $\overline{CS}$	-	-	± 10	uA
I_{OZ}	Output leakage current (note 2)	Output disabled, V_{OUT} = V_{SS} or V_{DD}	-	-	± 20	uA
I_{DDL}	Standby supply current (MA6116)	Chip disabled	-	0.1	4	mA
I_{DDL}	Standby supply current (MA6216)	Chip disabled	-	0.1	5	mA
I_{DD}	Power supply current	f_{RC} = 1MHz, $\overline{CS}$ = 50% mark:space	-	20	40	mA

Table 3: DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DR}	V_{DD} for Data Retention	$\overline{CS}$ = V_{DR}	2.0	-	-	V
I_{DDR}	Data Retention Current (MA6116)	$\overline{CS}$ = V_{DR}, V_{DR} = 2.0V	-	50	2000	µA
I_{DDR}	Data Retention Current (MA6216)	$\overline{CS}$ = V_{DR}, V_{DR} = 2.0V	-	50	2500	µA

Table 4: Data Retention Characteristics

AC Electrical Characteristics: MA6116

Notes for tables 5 and 6:
1. The characteristics shown apply to pre radiation at T_A = -55°C to + 125°C with V_{DD} = 5V ± 10% and to post 100kRad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ± 10%.
2. Input pulse = V_{SS} to 3.0V.
3. Times measurement reference level = 1.5V.
4. Output load 1TTL gate and C_L = 100pF.
5. Transition is measured at ± 500mV from steady state. This parameter is sampled and not 100% tested.
6. Input Rise and Fall times < 5ns.
7. Input transition times to be < 1µs.

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Read cycle time	150	-	ns
t_{AA}	Address access time	-	130	ns
t_{ACS}	Chip select access time	-	140	ns
t_{CLX} (note 5)	Chip select to output in low Z	10	-	ns
t_{OE}	Output enable to output valid	-	80	ns
t_{OLZ} (note 5)	Output enable to output in Low Z	10	-	ns
t_{CHZ} (note 5)	Chip deselect to output in High Z	0	60	ns
t_{OHZ} (note 5)	Chip disable to output in High Z	0	60	ns
t_{OH}	Output hold from address change	10	-	ns

Table 5: Read Cycle AC Electrical Characteristics

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Write Cycle Time	150	-	ns
t_{CWH}	Chip selection to end of write	85	-	ns
t_{AW}	Address valid to end of Write	80	-	ns
t_{AS}	Address set up time	20	-	ns
t_{WP}	Write pulse width	50	-	ns
t_{WR}	Write recovery Time	5	-	ns
t_{DHZ} (note 5)	Output disable to output in High Z	0	60	ns
t_{WHZ} (note 5)	Write to output in High Z	0	60	ns
t_{DW}	Data to write time overlap	30	-	ns
t_{DH}	Data hold from write time	10	-	ns
t_{OW} (note 5)	Output active from end to write	5	-	ns
t_{CWL}	Chip selection to write low	25	-	ns

Table 6: Write Cycle AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	6	10	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	-	5	7	pF

Note. T_A = 25°C and f = 1MHz

Table 7: Capacitance

AC Electrical Characteristics: MA6216

Notes for tables 8 and 9:
1. The characteristics shown apply to pre radiation at T_A = -55°C to + 125°C with V_{DD} = 5V ± 10% and to post 100kRad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ± 10%.
2. Input pulse = V_{SS} to 3.0V.
3. Times measurement reference level = 1.5V.
4. Output load 1TTL gate and C_L = 100pF.
5. Transition is measured at ±500mV from steady state. This parameter is sampled and not 100% tested.
6. Input Rise and Fall times < 5ns.
7. Input transition times to be < 1µs.

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Read cycle time	100	-	ns
t_{AA}	Address access time	-	95	ns
t_{ACS}	Chip select access time	-	100	ns
t_{CLX} (note 5)	Chip select to output in low Z	10	-	ns
t_{OE}	Output enable to output valid	-	60	ns
t_{OLZ} (note 5)	Output enable to output in Low Z	10	-	ns
t_{CHZ} (note 5)	Chip deselect to output in High Z	0	50	ns
t_{OHZ} (note 5)	Chip disable to output in High Z	0	50	ns
t_{OH}	Output hold from address change	10	-	ns

Table 8: Read Cycle AC Electrical Characteristics

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Write Cycle Time	100	-	ns
t_{CWH}	Chip selection to end of write	75	-	ns
t_{AW}	Address valid to end of Write	70	-	ns
t_{AS}	Address set up time	10	-	ns
t_{WP}	Write pulse width	40	-	ns
t_{WR}	Write recovery Time	5	-	ns
t_{DHZ} (note 5)	Output disable to output in High Z	0	50	ns
t_{WHZ} (note 5)	Write to output in High Z	0	50	ns
t_{DW}	Data to write time overlap	25	-	ns
t_{DH}	Data hold from write time	10	-	ns
t_{OW} (note 5)	Output active from end to write	5	-	ns
t_{CWL}	Chip Selection to Write Low	25	-	ns

Table 9: Write Cycle AC Electrical Characteristics

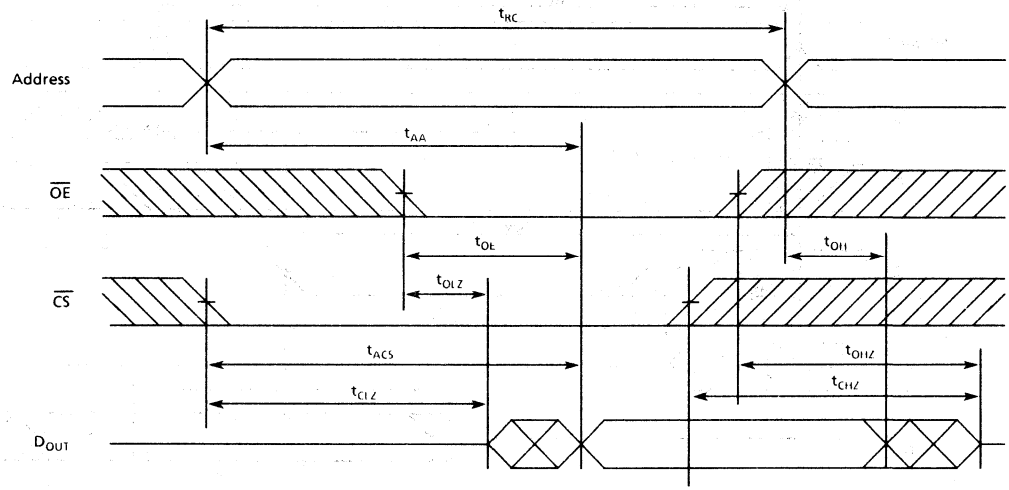
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	6	10	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	-	5	7	pF

Note: T_A = 25°C and f = 1MHz

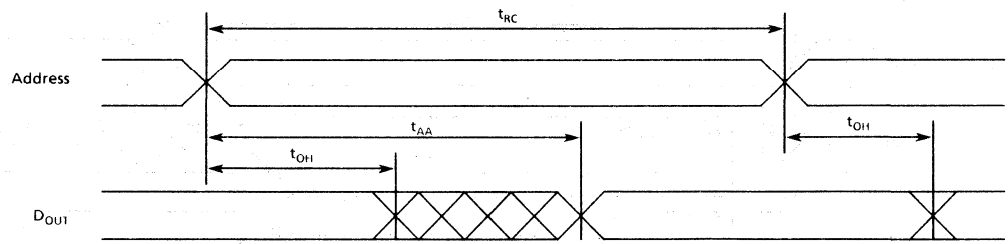
Table 10: Capacitance

Read Cycle Timing Waveforms

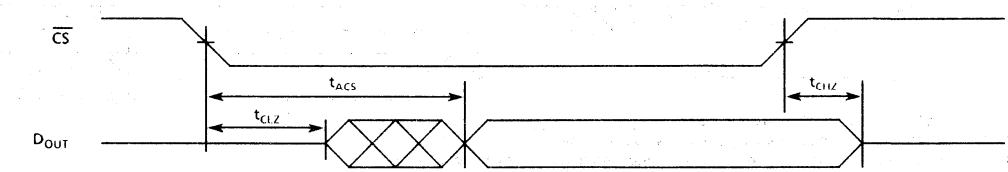
Cycle 1 figure 2 (see notes 1, and 5 below)



Cycle 2 figure 3 (see notes 1, 2, 4 and 5 below)



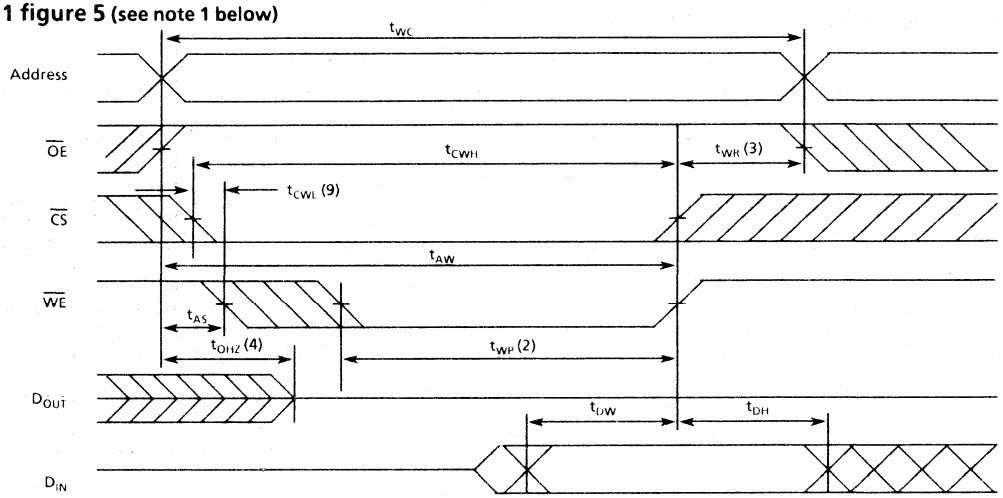
Cycle 3 figure 4 (see notes 1, 3, 4 and 5 below)



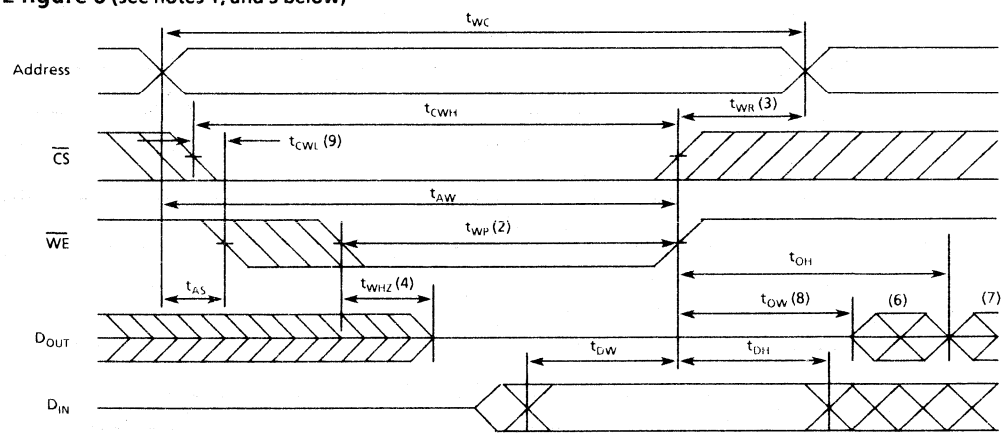
1 $\overline{WE}$ is high for Read Cycle.
2 Device is continuously selected. $\overline{CS} = V_{IL}$
3 Address Valid prior to or coincident with $\overline{CS}$ transition low
4 $\overline{OE} = V_{IL}$.
5. When $\overline{CS}$ is low, the address input must not be in the high impedance state.

Write Cycle Timing Waveforms

Cycle 1 figure 5 (see note 1 below)



Cycle 2 figure 6 (see notes 1, and 5 below)

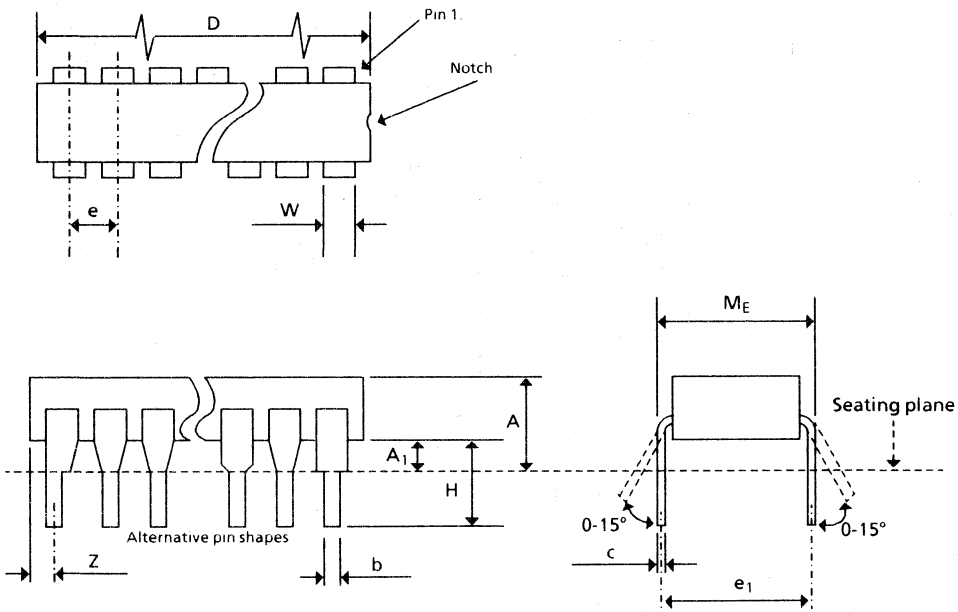


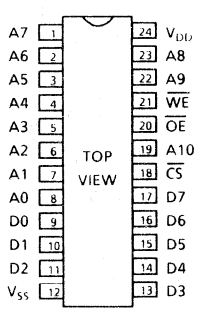
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must be applied.
5. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
6. D_{OUT} is the write data of the current address of this cycle. If $\overline{CS} = 1$, then D_{out} is three state.
7. D_{OUT} is the read data of the next address, if $\overline{CS} = 0$.
8. If the $\overline{CS}$ is low after t_{OW}, I/O pins are in the output state. If so, data input signals of opposite phase to the outputs must not be applied to the I/O pins.
9. t_{CWL} must be met to prevent memory corruption.

MA6116/6216

Radiation Hard 2048x8 Bit Static RAM

Package Outlines & Pin Assignments

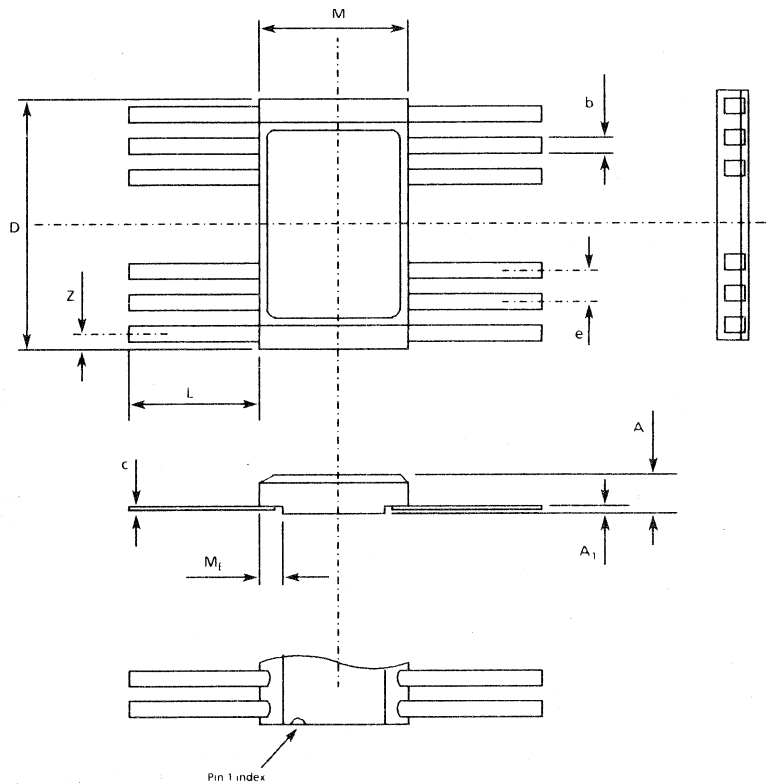


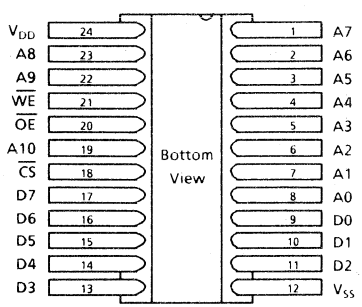


Ref.	Min.	Nom.	Max.
A	-	-	5.60 (0.220)
A_1	0.38 (0.015)	-	1.53 (0.060)
b	0.35 (0.014)	-	0.59 (0.023)
c	0.20 (0.008)	-	0.36 (0.014)
D	-	-	30.79 (1.212)
e	-	2.54(0.100) typ.	-
e_1	-	15.24(0.600) typ.	-
H	4.71 (0.185)	-	5.38 (0.212)
M_E	-	-	15.90 (0.626)
Z	-	-	1.27 (0.050)
W	-	-	1.53 (0.060)
Dimensions in mm (inches)			

MEDL XG403

Figure 7: 24-Lead Ceramic DIL (solder seal) - package style C





Ref.	Min.	Nom.	Max.
A			2.67 (0.105)
A_1	0.25 (0.010)		1.02 (0.040)
b	0.38 (0.015)		0.48 (0.019)
c	0.10 (0.004)		0.18 (0.007)
D	14.86 (0.585)		15.62 (0.615)
e		2.54 (0.050)	
L	6.73 (0.265)		7.75 (0.305)
M	9.91 (0.390)		10.41 (0.410)
M_E	7.6 (0.30)		
Z	0.13 (0.005)		1.14 (0.045)
Dimensions in mm (inches)			

MEDL XG472

Figure 8: 24-lead Ceramic Flatpack (solder seal) - Package style F

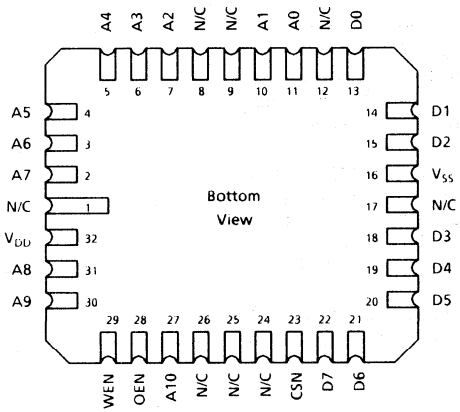
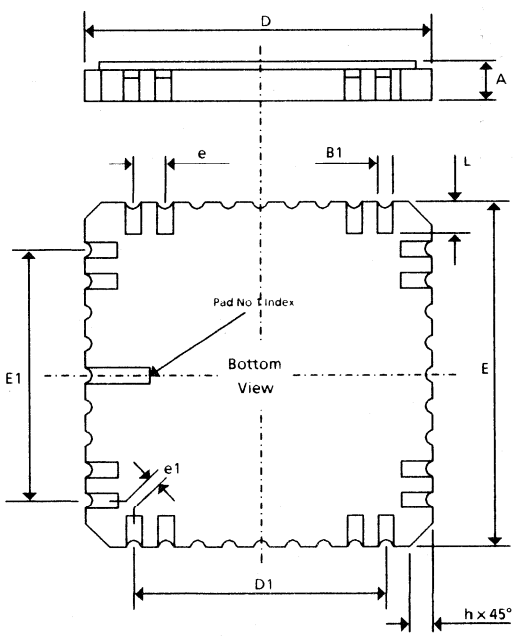


Figure 9: 32-pad Leadless Chip Carrier (Package style L)

5



Ref.	Max.	Nom.	Min.
A	0.090	-	0.072
B1	0.028	-	0.022
D	0.458	-	0.445
D1	-	0.300	-
E	0.560	-	0.545
E1	-	0.400	-
e	-	0.050	-
e1	-	-	0.015
h	-	0.040	-
i	-	0.020	-
L	-	0.050	-
L2	0.093	-	0.077

MEDL XG520

Figure 10: 32-pad Leadless Chip Carrier (Package style L)

RadiationTolerance

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

Total Dose (Function to specification)	1.0×10^5 Rad(Si)
Transient Upset (survivability)	5×10^{10} Rad(Si)/sec
Neutron Hardness (Function to specification)	$>10^{15}$ neutrons/cm^2
Single Event Upset (GSO 10% worst case)	3.6×10^{-9} errors/bitday
Latch-up	Not possible

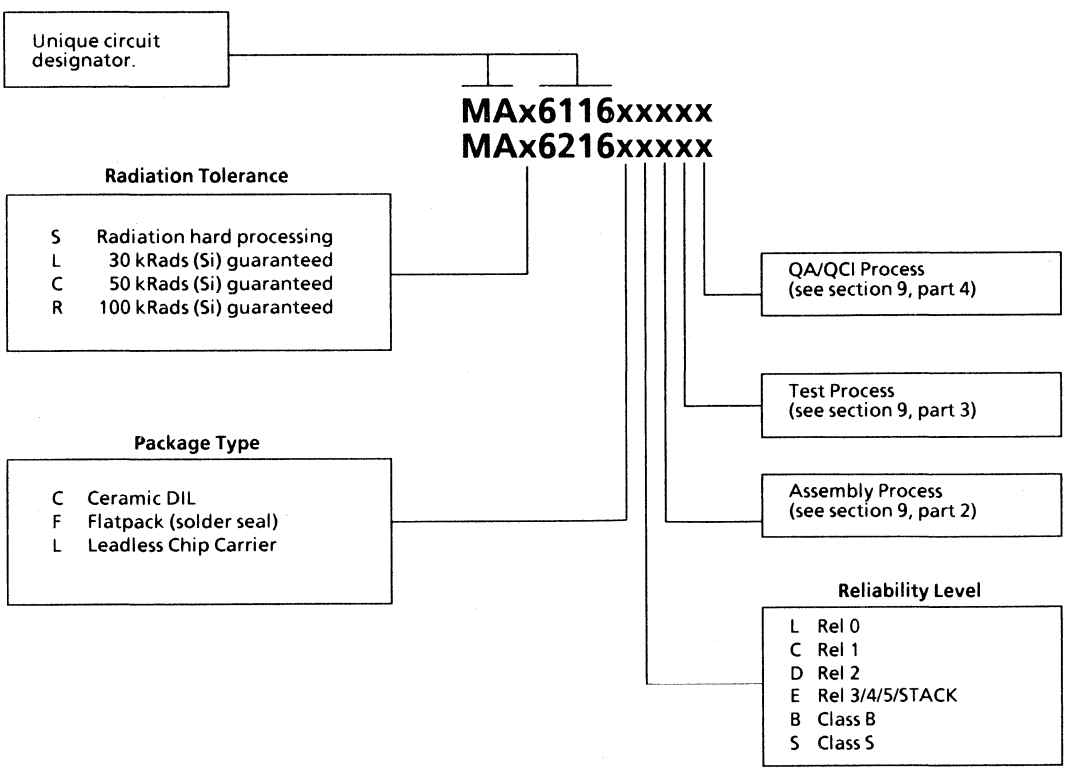
Table 11: Radiation Hardness Parameters

MA6116/6216

Radiation Hard 2048x8 Bit Static RAM

Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



GEC PLESSEY

SEMICONDUCTORS

S10300PDS Issue 2.3 October 1990

MA9067

Radiation Hard 16384x1 Bit Static RAM

(Preliminary Data)

Features

- **1.5µm CMOS-SOS technology**
- **Latch up free**
- **Fast access time 100ns typical**
- **Total dose 10^6 rad (Si)**
- **Transient upset > 10^{11} rad (Si) /sec**
- **SEU 4.3×10^{-11} errors / bitday**
- **Single 5V supply**
- **Three state output**
- **Low standby current 100µA typical**
- **-55°C to + 125°C operation**

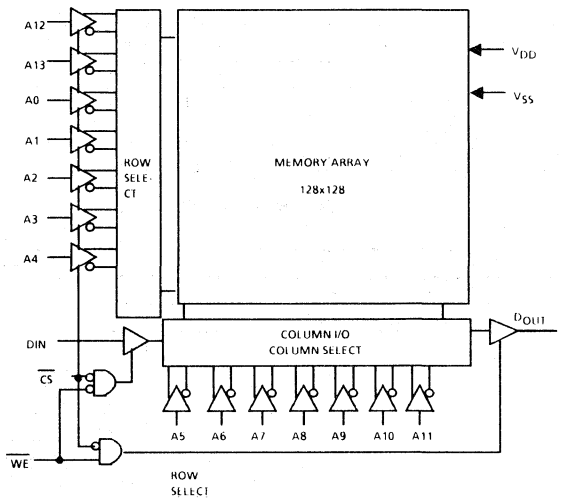


Figure 1: Block Diagram

General Description

The MA9067 16k Static RAM is configured as 16384x1 bits and manufactured using MEDL's CMOS-SOS high performance, radiation hard, 1.5µm technology.

The device has separate input and output terminals controlled by Chip Select and Write Enable. The design uses a 6 transistor cell with address input buffers deselected when chip select is in the high state.

$\overline{CS}$	$\overline{WE}$	Mode	Current	Output
H	X	Not Selected	I_{SBI}	High Z
L	H	Read	I_{DD}	D_{out}
L	L	Write	I_{DD}	High Z

Figure 2: Truth Table

5

Radiation Hard 16384x1 Bit Static RAM

(Preliminary Data)

DC Characteristics and Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0 5	7	V
V_I	Input voltage	-0 3	V_{DD} + 0.3	V
T_A	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 3: Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4 5	5.0	5 5	V
V_{IH}	Logical '1' Input Voltage	-	2.0	-	V_{DD}	V
V_{IL}	Logical '0' Input Voltage	-	V_{SS}	-	0.8	V
V_{OH1}	Logical '1' Output Voltage	I_{OH1} = -4mA	2 4	-		V
V_{OH2}	Logical '1' Output Voltage	I_{OH2} = -3mA	V_{DD}-0 5	-		V
V_{OL}	Logical '0' Output Voltage	I_{OL} = 8mA	-	-	0.4	V
I_{LI}	Input Leakage Current	$V_{IN} = V_{DD}$ or V_{SS} All inputs	-	-	± 20	µA
I_{LO}	Output Leakage Current	Chip disabled, $V_{OUT} = V_{DD}$ or V_{SS}	-	-	± 20	µA
I_{DD1}	Selected Static Current(TTL)	All inputs = 3V except $\overline{CS} \leq 0.8V$	-	18	30	mA
I_{DD2}	Selected Static Current(CMOS)	All inputs = V_{DD}-0.2V except $\overline{CS} = V_{SS}$ + 0.2v	-	100	4000	µA
I_{DD3}	Dynamic Operating Current (TTL)	f_{RC} = 1MHz, all inputs switching, V_{IH} = 3V	-	10	20	mA
I_{DD4}	Dynamic Operating Current (CMOS)	f_{RC} = 1MHz, all inputs switching, $V_{IH} = V_{DD}$-0.2V	-	3	7	mA
I_{SB1}	Standby Supply Current	$\overline{CS} = V_{DD}$-0 2V	-	100	4000	µA

Note: The above characteristics apply to pre radiation at T_A = -55°C to + 125°C with V_{DD} = 5V ± 10% and to post 100kRad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ± 10%.

Figure 4: Electrical Chacteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DR}	V_{CC} for Data Retention	$\overline{CS} = V_{DR}$	2 0	-	-	V
I_{DDR}	Data Retention Current	$\overline{CS} = V_{DR}$, V_{DR} = 2 0V		50	1600	µA

Figure 5: Data Retention Characteristics

AC Characteristics

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Read Cycle Time	125	-	ns
t_{AA}	Address Access Time	-	125	ns
t_{ACS}	Chip select Access time	-	125	ns
t_{CLZ} (note 5)	Chip Selection to Output in Low Z	5	-	ns
t_{CHZ} (note 5)	Chip Deselection to Output in High Z	0	50	ns
t_{OH}	Output Hold from Address change	5	-	ns
t_{PU}	Chip selection to Power-up time	0	-	ns
t_{PD}	Chip deselection to Power-down time	-	35	ns

Figure 6: Read Cycle Electrical Characteristics

Symbol	Parameter	Min.	Max.	Units
t_{CW}	Chip Selection to End of Write	125	-	ns
t_{WC}	Write Cycle Time	115	-	ns
t_{AW}	Address Valid to End of Write	115	-	ns
t_{AS}	Address Set Up Time	0	-	ns
t_{WP}	Write Pulse Width	95	-	ns
t_{WR}	Write Recovery Time	10	-	ns
t_{WHZ} (note 5)	Write to Output in High Z	0	40	ns
t_{DW}	Data to Write Time Overlap	40	-	ns
t_{DH}	Data Hold from Write	25	-	ns
t_{OW} (note 5)	Output Active from End to Write	0	40	ns

Figure 7: Write Cycle Electrical Characteristics

Notes for figures 6 & 7:

1. Input Pulse V_{SS} to 3.0 Volts.
2. Times Measurement Reference Level 1.5 Volts.
3. Input Rise and Fall Times ≤ 5ns
4. Output Load 1TTL Gate and C_L = 60pF
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.
6. The above characteristics apply to pre radiation at T_A = -55°C to +125°C with V_{DD} = 5V ± 10% and to post 100kRad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ± 10%.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	3	5	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	-	5	7	pF

TA = 25°C, f = 1MHz

Figure 8: Capacitance

Read Cycle Timing Waveforms

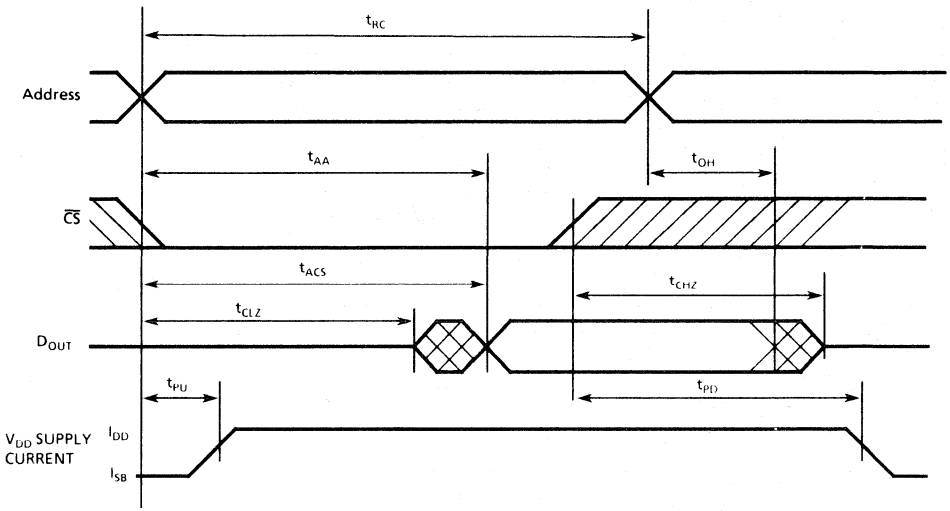


Figure 9: Cycle 1 (see notes 1, 3, and 4 below)

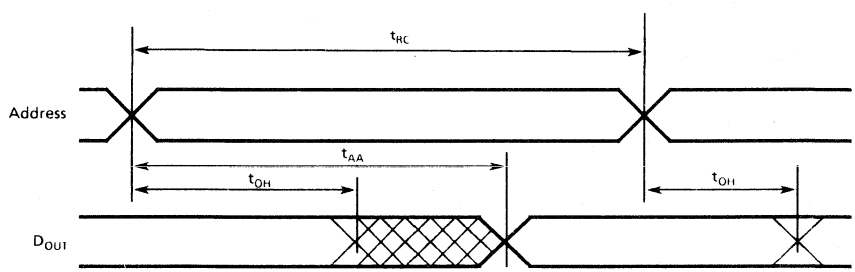
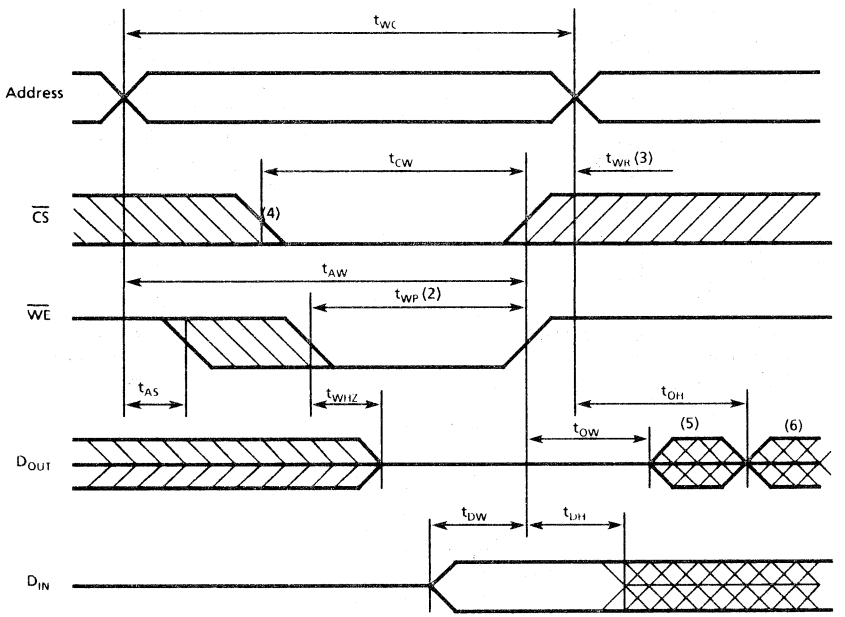


Figure 10: Cycle 2 (see notes 1, 2, and 4 below)

Notes for figures 9 & 10:
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected. $\overline{CS} = V_{IL}$
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. When $\overline{CS}$ is low, the address input must not be in the high impedance state.

Write Cycle Timing Waveforms



1. $\overline{WE}$ must be high during all address transitions
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remains in a high impedance state.
5. D_{OUT} is identical to the write data in this cycle
6. D_{OUT} is the read data of the next address.

Figure 11: Write Cycle Timing Waveforms

5

GEC PLESSEY
SEMICONDUCTORS

Radiation Hard 16384 x 1 Bit Static RAM

(Preliminary Data)

Pin Assignments

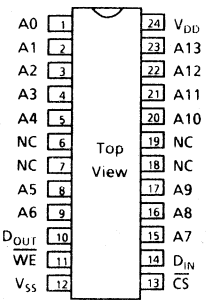


Figure 12: 24-lead Ceramic DIL (solder seal)
Pin Assignment option 1
Package style C

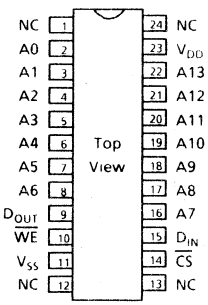


Figure 13: 24-lead Ceramic DIL (solder seal)
Pin Assignment option 2
Package style C

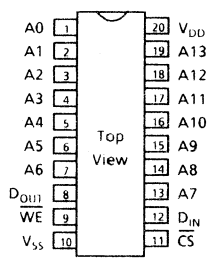


Figure 14: 20-lead Ceramic DIL (solder seal)
Package style C

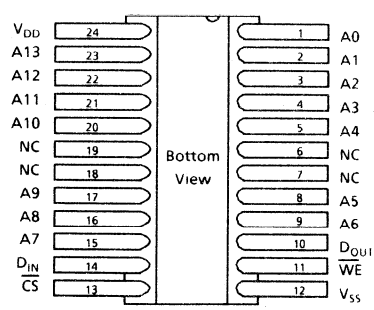


Figure 15: 24-lead Ceramic Flatpack(solder seal)
Pin Assignment option 1
Package style F

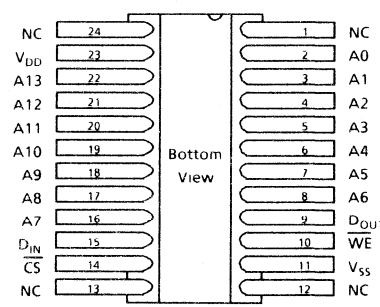


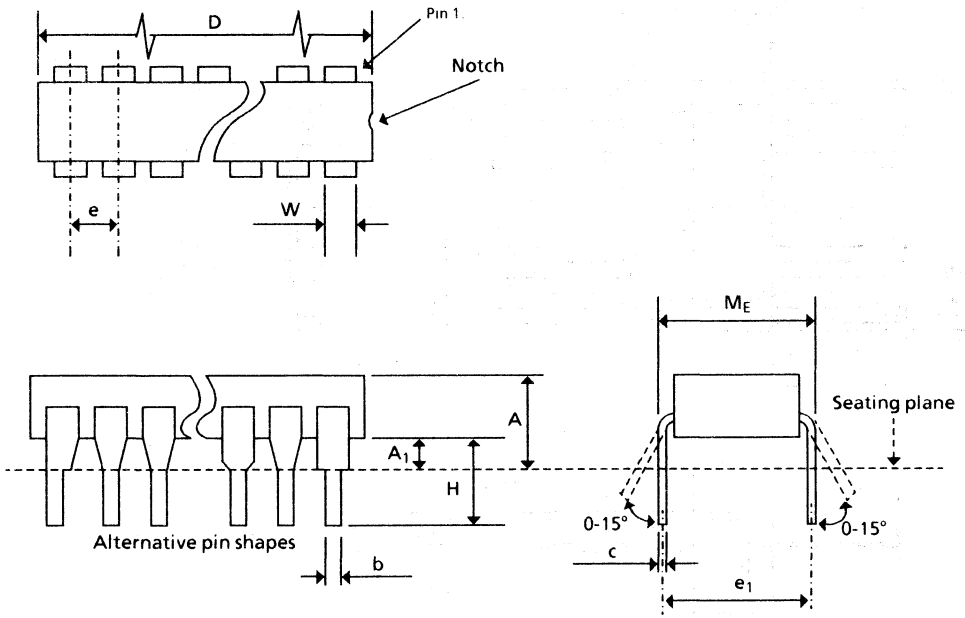
Figure 16: 24-lead Ceramic Flatpack(solder seal)
Pin Assignment option 2
Package style F

MA9067

Radiation Hard 16384 x 1 Bit Static RAM

(Preliminary Data)

Package Outlines



20-Lead

Ref.	Min.	Nom.	Max.
A	-	-	5.60 (0.220)
A_1	0.38 (0.015)	-	1.53 (0.060)
b	0.35 (0.014)	-	0.59 (0.023)
c	0.20 (0.008)	-	0.36 (0.014)
D	23.11 (0.910)	-	25.65 (1.010)
e	-	2.54(0.100) typ.	-
e_1	-	8.13 (0.300) typ.	-
H	4.71 (0.185)	-	5.38 (0.212)
M_E	-	-	7.95 (0.313)
W	-	-	1.53 (0.060)

Dimensions in mm (inches)

MEDL XG483

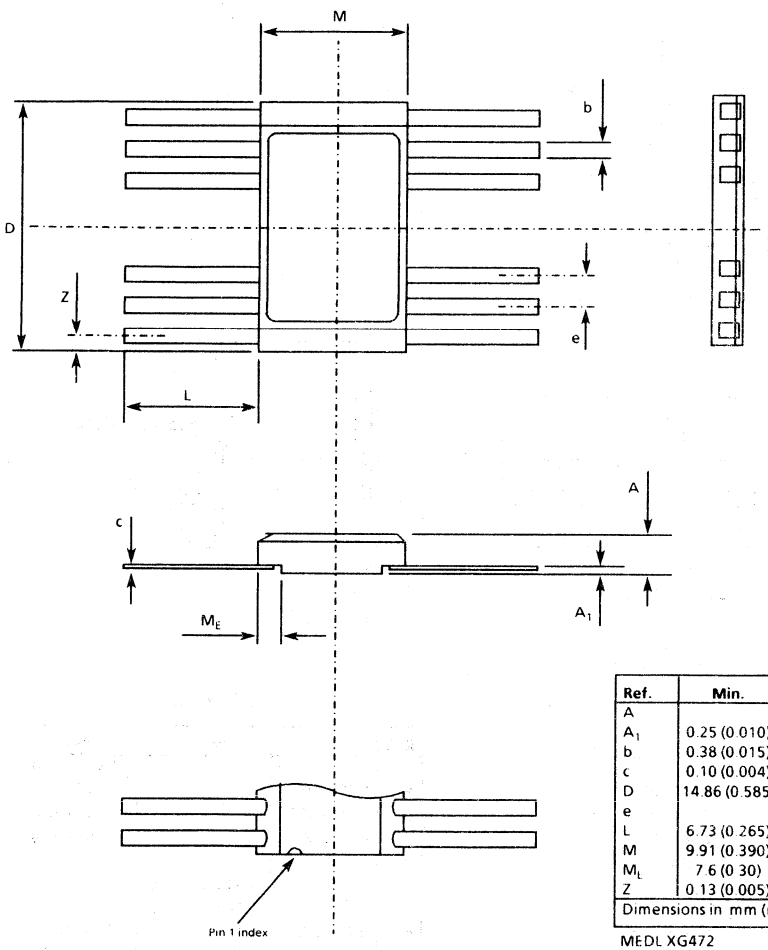
24-Lead

Ref.	Min.	Nom.	Max.
A	-	-	5.60 (0.220)
A_1	0.38 (0.015)	-	1.53 (0.060)
b	0.35 (0.014)	-	0.59 (0.023)
c	0.20 (0.008)	-	0.36 (0.014)
D	-	-	30.79 (1.212)
e	-	2.54(0.100) typ.	-
e_1	-	15.24(0.600) typ.	-
H	4.71 (0.185)	-	5.38 (0.212)
M_E	-	-	15.90 (0.626)
W	-	-	1.53 (0.060)

Dimensions in mm (inches)

MEDL XG403

Figure 17: 20/24-Lead Ceramic DIL (solder seal) - package style C



Ref.	Min.	Nom.	Max.
A			2.67 (0.105)
A_1	0.25 (0.010)		1.02 (0.040)
b	0.38 (0.015)		0.48 (0.019)
c	0.10 (0.004)		0.18 (0.007)
D	14.86 (0.585)		15.62 (0.615)
e		2.54 (0.050)	
L	6.73 (0.265)		7.75 (0.305)
M	9.91 (0.390)		10.41 (0.410)
M_L	7.6 (0.30)		
Z	0.13 (0.005)		1.14 (0.045)

Dimensions in mm (inches)

MEDL XG472

Figure 18: 24-lead Ceramic Flatpack (solder seal) - Package style F

MA9067

Radiation Hard 16384 x 1 Bit Static RAM

(Preliminary Data)

RadiationTolerance

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

Total Dose (Function)	10^5 Rad(Si)
Transient Upset (Survivability)	$1x10^{11}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>10^{11}$ neutrons/cm^2
Single Event Upset (GSO 10% worst case)	$4.3x10^{-11}$ errors/bitday
Latch-up	Not possible

Figure 18: Radiation Tolerance

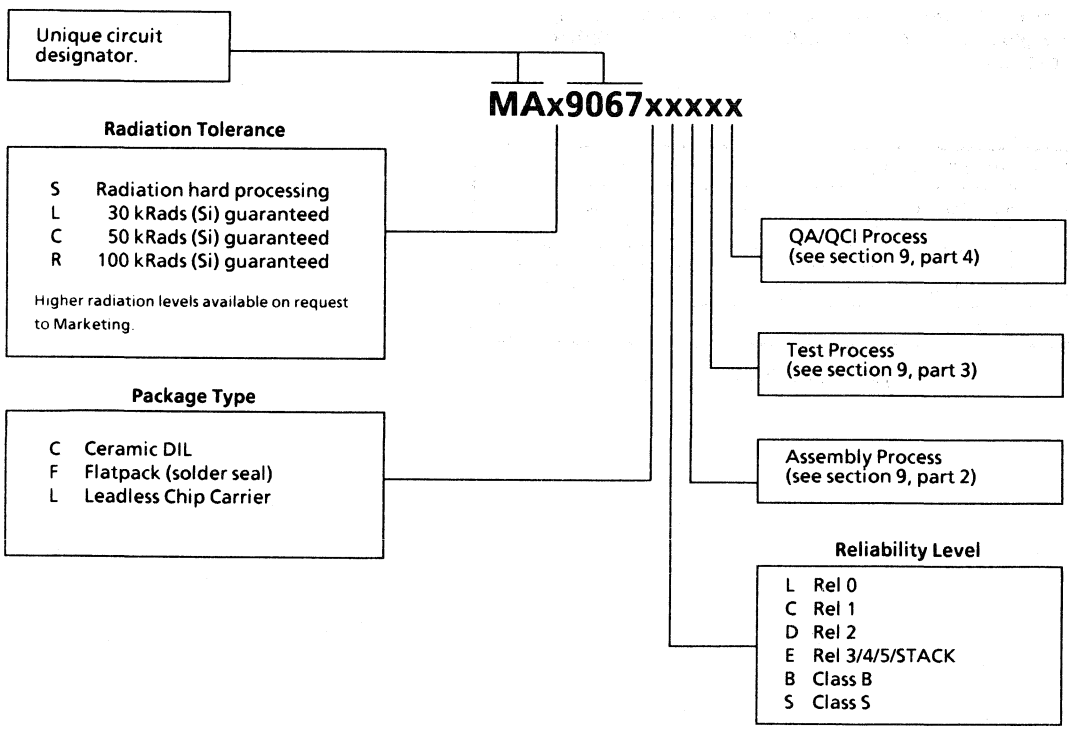
MA9067

GEC PLESSEY
SEMICONDUCTORS

Radiation Hard
16384 x 1 Bit Static RAM
(Preliminary Data)

Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



GEC PLESSEY

SEMICONDUCTORS

S10300PDS Issue 2.4 October 1990

MA9167

Radiation Hard 16384x1 Bit Static RAM

(Preliminary Data)

Features

- 1.5µm CMOS-SOS technology
- Latch up free
- Fast access time 50ns typical
- Total dose 10^6 rad (Si)
- Transient upset > 10^{11} rad (Si) /sec
- SEU 4.3x10^{-11} errors / bitday
- Single 5V supply
- Three state output
- Low standby current 100µA typical
- -55°C to + 125°C operation

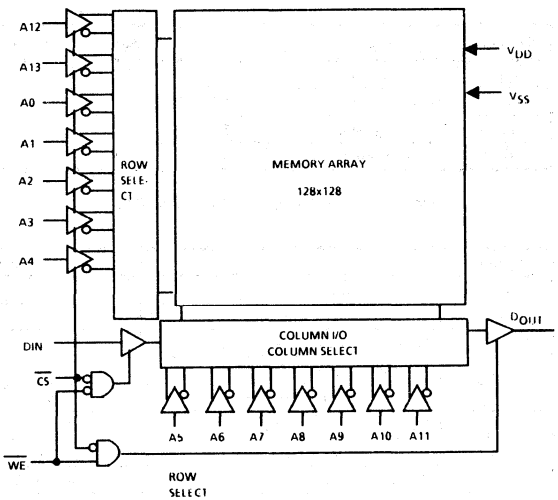


Figure 1: Block Diagram

General Description

The MA9167 16k Static RAM is configured as 16384x1 bits and manufactured using MEDL's CMOS-SOS high performance, radiation hard, 1.5µm technology.

The device has separate input and output terminals controlled by Chip Select and Write Enable. The design uses a 6 transistor cell with address input buffers deselected when chip select is in the high state.

$\overline{CS}$	$\overline{WE}$	Mode	Current	Output
H	X	Not Selected	I_{SBI}	High Z
L	H	Read	I_{DD}	D_{out}
L	L	Write	I_{DD}	High Z

Figure 2: Truth Table

5

Radiation Hard 16384x1 Bit Static RAM
(Preliminary Data)

DC Characteristics and Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0.5	7	V
V_I	Input voltage	-0.3	V_{DD} + 0.3	V
T_A	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 3: Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	Logical '1' Input Voltage	-	2.0	-	V_{DD}	V
V_{IL}	Logical '0' Input Voltage	-	V_{SS}	-	0.8	V
V_{OH1}	Logical '1' Output Voltage	I_{OH1} = -4mA	2.4	-		V
V_{OH2}	Logical '1' Output Voltage	I_{OH2} = -3mA	V_{DD}-0.5	-		V
V_{OL}	Logical '0' Output Voltage	I_{OL} = 8mA	-	-	0.4	V
I_{LI}	Input Leakage Current	$V_{IN} = V_{DD}$ or V_{SS} All inputs	-	-	± 10	µA
I_{LO}	Output Leakage Current	Chip disabled, $V_{OUT} = V_{DD}$ or V_{SS}	-	-	± 10	µA
I_{DD1}	Selected Static Current(TTL)	All inputs = 3V except $\overline{CS} \leq 0.8V$	-	18	30	mA
I_{DD2}	Selected Static Current(CMOS)	All inputs = V_{DD}-0.2V except $\overline{CS} = V_{SS}$ + 0.2v	-	100	2000	µA
I_{DD3}	Dynamic Operating Current (TTL)	f_{RC} = 1MHz, all inputs switching, V_{IH} = 3V	-	10	20	mA
I_{DD4}	Dynamic Operating Current (CMOS)	f_{RC} = 1MHz, all inputs switching, $V_{IH} = V_{DD}$-0.2V	-	3	6	mA
I_{SB1}	Standby Supply Current	$\overline{CS} = V_{DD}$-0.2V	-	100	2000	µA

Note: The above characteristics apply to pre radiation at T_A = -55°C to + 125°C with V_{DD} = 5V ± 10% and to post 300kRad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ± 10%.

Figure 4: Electrical Chacteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DR}	V_{CC} for Data Retention	$\overline{CS} = V_{DR}$	2.0	-	-	V
I_{DDR}	Data Retention Current	$\overline{CS} = V_{DR}$, V_{DR} = 2.0V	-	50	1000	µA

Figure 5: Data Retention Characteristics

AC Characteristics

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Read Cycle Time	75	-	ns
t_{AA}	Address Access Time	-	70	ns
t_{ACS}	Chip select Access time	-	70	ns
t_{CLZ} (note 5)	Chip Selection to Output in Low Z	15	-	ns
t_{CHZ} (note 5)	Chip Deselection to Output in High Z	0	25	ns
t_{OH}	Output Hold from Address change	15	-	ns
t_{PU}	Chip selection to Power-up time	0	-	ns
t_{PD}	Chip deselection to Power-down time	-	35	ns

Figure 6: Read Cycle Electrical Characteristics

Symbol	Parameter	Min.	Max.	Units
t_{CW}	Chip Selection to End of Write	45	-	ns
t_{WC}	Write Cycle Time	50	-	ns
t_{AW}	Address Valid to End of Write	45	-	ns
t_{AS}	Address Set Up Time	0	-	ns
t_{WP}	Write Pulse Width	30	-	ns
t_{WR}	Write Recovery Time	0	-	ns
t_{WHZ} (note 5)	Write to Output in High Z	0	20	ns
t_{DW}	Data to Write Time Overlap	25	-	ns
t_{DH}	Data Hold from Write	0	-	ns
t_{OW} (note 5)	Output Active from End to Write	0	20	ns

Figure 7: Write Cycle Electrical Characteristics

Notes for figures 6 and 7:

1. Input Pulse V_{SS} to 3.0 Volts
2. Times Measurement Reference Level 1 5 Volts
3. Input Rise and Fall Times ≤ 5ns
4. Output Load 1TTL Gate and C_L = 60pF
5. Transition is measured ± 500mV from steady state. This parameter is sampled and not 100% tested.
6. The above characteristics apply to pre radiation at T_A = -55°C to + 125°C with V_{DD} = 5V ± 10% and to post 300kRad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ± 10%.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	3	5	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	-	5	7	pF

TA = 25°C, f = 1MHz

Figure 8: Capacitance

Read Cycle Timing Waveforms

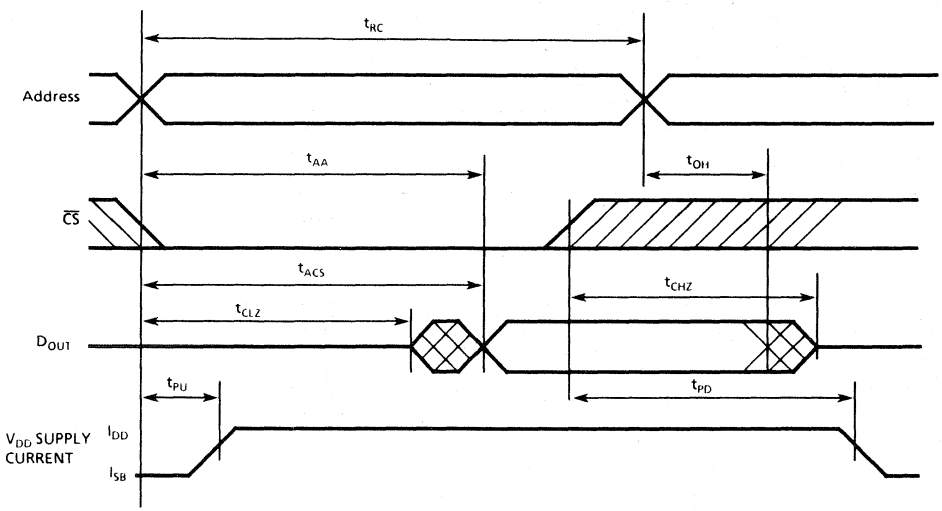


Figure 9: Cycle 1 (see notes 1, 3, and 4 below)

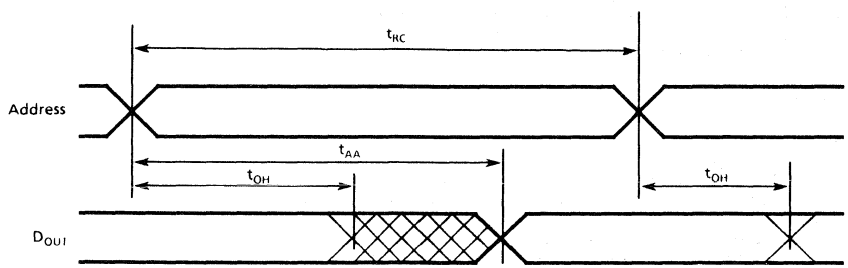


Figure 10: Cycle 2 (see notes 1, 2, and 4 below)

Notes for figures 9 & 10:
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected $\overline{CS} = V_{IL}$
3. Address Valid prior to or coincident with $\overline{CS}$ transition low.
4. When $\overline{CS}$ is low, the address input must not be in the high impedance state.

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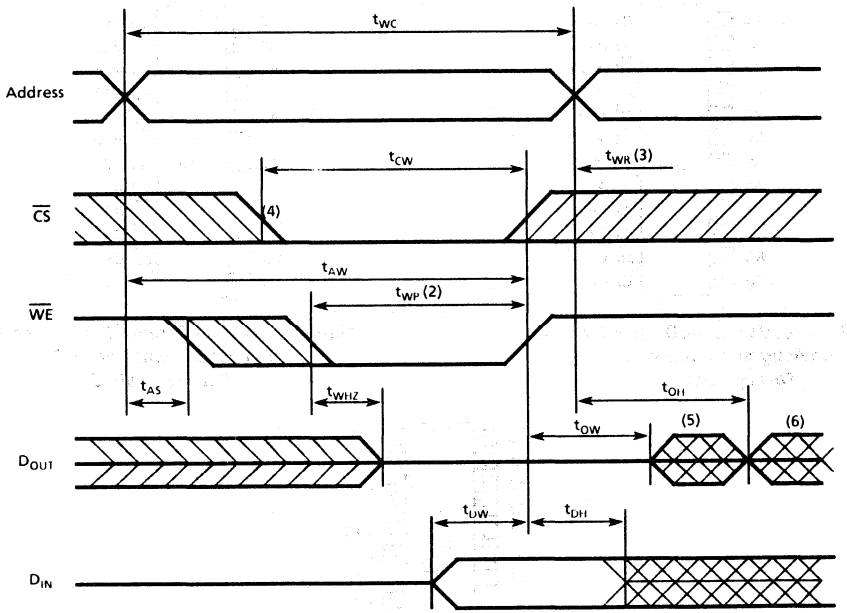
Radiation Hard 16384 x 1 Bit Static RAM

(Preliminary Data)

Write Cycle Timing Waveforms



1 $\overline{WE}$ must be high during all address transitions.
2 A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3 t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4 If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remains in a high impedance state.
5 D_{OUT} is identical to the write data in this cycle.
6 D_{OUT} is the read data of the next address.

Figure 11: Write Cycle Timing Waveforms

Radiation Hard 16384 x 1 Bit Static RAM

(Preliminary Data)

Pin Assignments

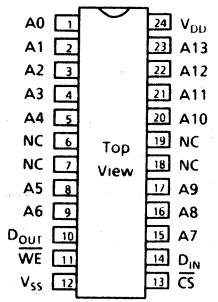


Figure 12: 24-lead Ceramic DIL (solder seal)
Pin Assignment option 1
Package style C

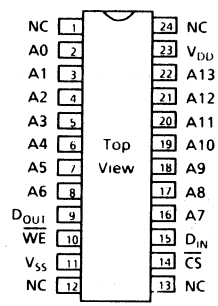


Figure 13: 24-lead Ceramic DIL (solder seal)
Pin Assignment option 2
Package style C

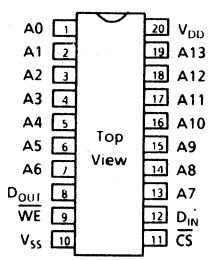


Figure 14: 20-lead Ceramic DIL (solder seal)
Package style C

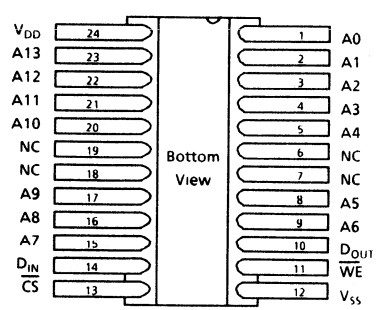


Figure 15: 24-lead Ceramic Flatpack (solder seal)
Pin Assignment option 1
Package style F

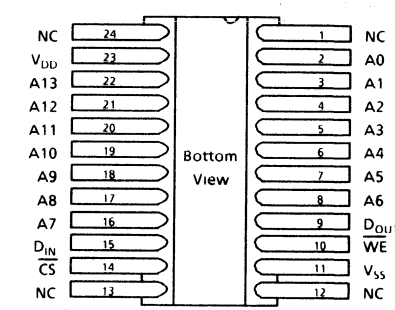


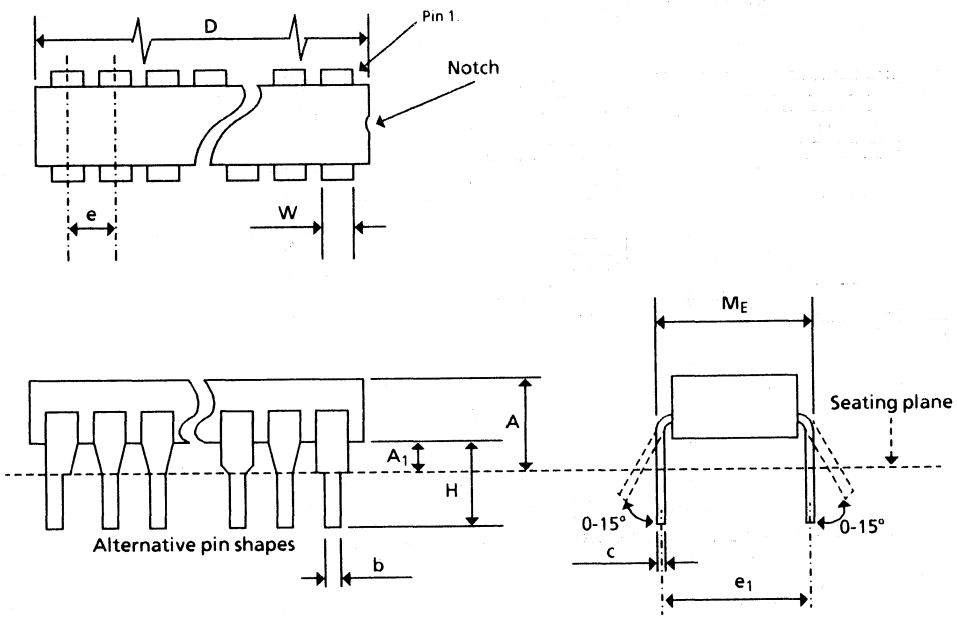
Figure 16: 24-lead Ceramic Flatpack (solder seal)
Pin Assignment option 2
Package style F

MA9167

Radiation Hard 16384 x 1 Bit Static RAM

(Preliminary Data)

Package Outlines



20-Lead

Ref.	Min.	Nom.	Max.
A	-	-	5.60 (0.220)
A_1	0.38 (0.015)	-	1.53 (0.060)
b	0.35 (0.014)	-	0.59 (0.023)
c	0.20 (0.008)	-	0.36 (0.014)
D	23.11 (0.910)	-	25.65 (1.010)
e	-	2.54(0.100) typ.	-
e_1	-	8.13 (0.300) typ.	-
H	4.71 (0.185)	-	5.38 (0.212)
M_E	-	-	7.95 (0.313)
W	-	-	1.53 (0.060)

Dimensions in mm (inches)

MEDL XG483

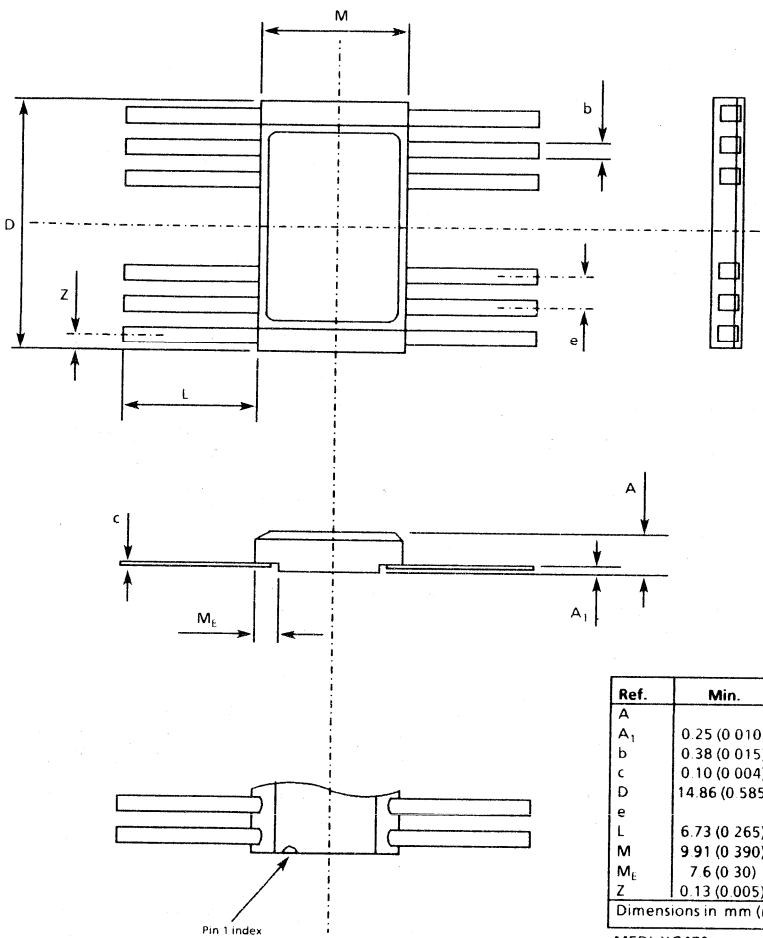
24-Lead

Ref.	Min.	Nom.	Max.
A	-	-	5.60 (0.220)
A_1	0.38 (0.015)	-	1.53 (0.060)
b	0.35 (0.014)	-	0.59 (0.023)
c	0.20 (0.008)	-	0.36 (0.014)
D	-	-	30.79 (1.212)
e	-	2.54(0.100) typ.	-
e_1	-	15.24(0.600) typ.	
H	4.71 (0.185)	-	5.38 (0.212)
M_E	-	-	15.90 (0.626)
W	-	-	1.53 (0.060)

Dimensions in mm (inches)

MEDL XG403

Figure 17: 20/24-Lead Ceramic DIL (solder seal) - package style C



Ref.	Min.	Nom.	Max.
A			2.67 (0.105)
A_1	0.25 (0.010)		1.02 (0.040)
b	0.38 (0.015)		0.48 (0.019)
c	0.10 (0.004)		0.18 (0.007)
D	14.86 (0.585)		15.62 (0.615)
e		2.54 (0.050)	
L	6.73 (0.265)		7.75 (0.305)
M	9.91 (0.390)		10.41 (0.410)
M_E	7.6 (0.30)		
Z	0.13 (0.005)		1.14 (0.045)

Dimensions in mm (inches)

MEDL XG472

Figure 18: 24-lead Ceramic Flatpack (solder seal) - Package style F

RadiationTolerance

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

Total Dose (Function)	$1x10^{6}$ Rad(Si)
Transient Upset (Survivability)	$1x10^{11}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>10^{11}$ neutrons/cm^2
Single Event Upset (GSO 10% worst case)	$4.3x10^{-11}$ errors/bitday
Latch-up	Not possible

Figure 18: Radiation Tolerance

MA9167

Radiation Hard
16384 x 1 Bit Static RAM
(Preliminary Data)

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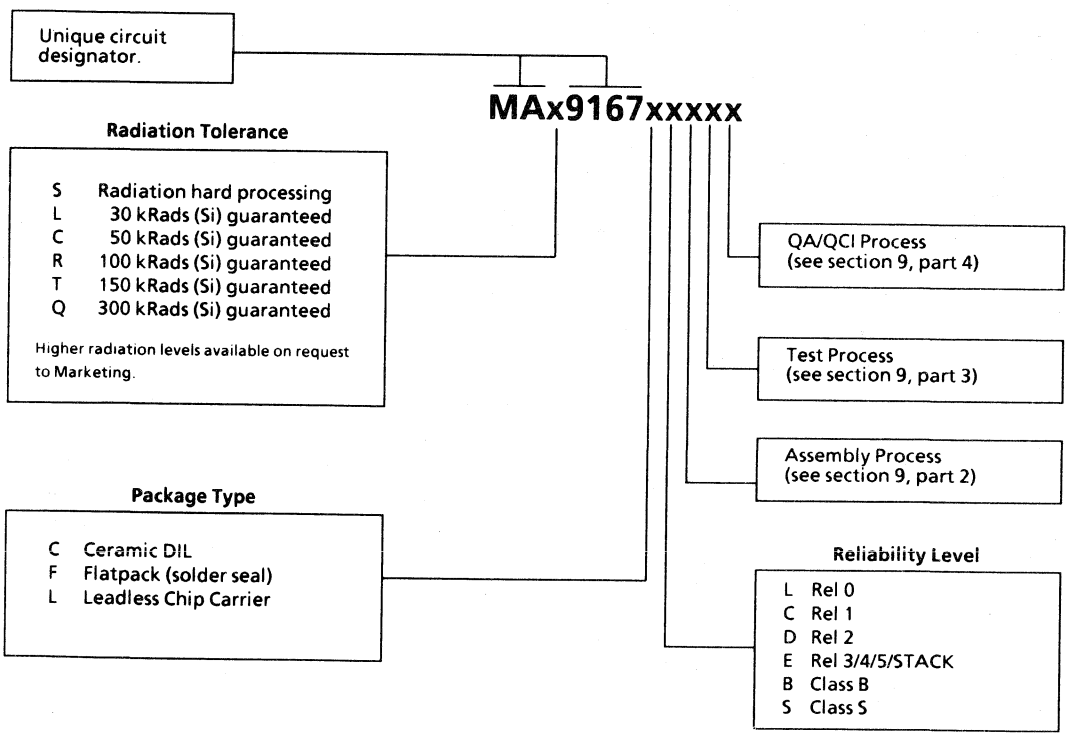
SEMICONDUCTORS

Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



S10309PDS Issue 2.3 October 1990

MA9187

Radiation Hard 65536x1 Bit Static RAM
(Preliminary Data)

Features

- 1.5µm CMOS-SOS technology
- Latch-up free
- Fast access time 45ns typical
- Total dose 10^6 rad (Si)
- Transient upset > 10^{11} rad (Si) /sec
- SEU 4.3×10^{-11} errors/bit day
- Single 5V supply
- All Inputs & outputs fully TTL & CMOS compatible
- Fully static operation
- Three state output
- Low standby current 100µA typical
- -55°C to +125°C operation

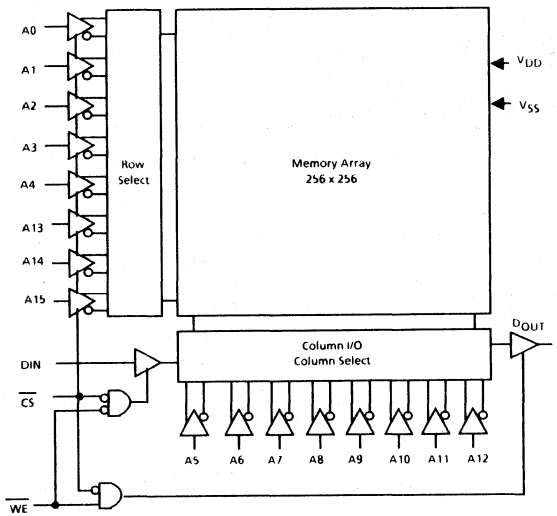


Figure 1: Block Diagarm

General Description

The MA9187 64k Static RAM is configured as 65536x1 bits and manufactured using MEDL's CMOS-SOS high performance, radiation hard, 1.5µm technology.

The device has separate input and output terminals controlled by Chip Select and Write Enable. The design uses a 6 transistor cell and has full static operation with no clock or timing strobe required. Address input buffers are deselected when Chip Select is in the high state.

$\overline{CS}$	$\overline{WE}$	Mode	V_{DD} Current	Output Pin
H	X	Deselected	I_{SBI}	High Z
L	H	Read	I_{DD}	D_{OUT}
L	L	Write	I_{DD}	High Z

Table 1: Truth Table

5

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SEMICONDUCTORS

Radiation Hard 65536x1 Bit Static RAM
(Preliminary Data)

DC Characteristics and Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0.5	7	V
V_I	Input voltage	-0.3	V_{DD} + 0.3	V
T_A	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2: Absolute Maximum Ratings

Notes for tables 3 and 4: Characteristics apply to pre radiation at T_A = -55°C to + 125°C with V_{DD} = 5V ± 10% and to post 300kRad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ± 10%.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	Input high voltage	-	2.0	-	V_{DD}	V
V_{IL}	Input low voltage	-	V_{SS}	-	0.8	V
V_{OH1}	Output high voltage	I_{OH1} = -4mA	2.4	-	-	V
V_{OH2}	Output high voltage	I_{OH2} = -3mA	V_{DD}-0.5	-	-	V
V_{OL}	Output low voltage	I_{OL} = 8mA	-	-	0.4	V
I_{LI}	Input leakage current	$V_{IN} = V_{DD}$ or V_{SS} on all inputs	-	-	± 10	uA
I_{LO}	Output leakage current	$V_{OUT} = V_{DD}$ or V_{SS} with chip disabled	-	-	± 10	uA
I_{DD1}	Selected static current (TTL)	All inputs = 3V except $\overline{CS}$ < 0.8V	-	18	30	mA
I_{DD2}	Selected static current (CMOS)	All inputs = V_{DD}-0.2V except $\overline{CS} = V_{SS}$ + 0.2V	-	100	4000	uA
I_{DD3}	Dynamic operating current (TTL)	f_{RC} = 1MHz, all inputs switching, V_{IH} = 3V	-	10	20	mA
I_{DD4}	Dynamic operating current (CMOS)	f_{RC} = 1MHz, all inputs switching, $V_{IH} = V_{DD}$-0.2V	-	3	7	mA
I_{SB1}	Standby supply current	$\overline{CS} = V_{DD}$-0.2V	-	100	4000	uA

Table 3: DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DR}	V_{CC} for Data Retention	$\overline{CS} = V_{DR}$	2.0	-	-	V
I_{DDR}	Data Retention Current	$\overline{CS} = V_{DR}$, V_{DR} = 2.0V	-	50	1500	µA

Table 4: Data Retention Characteristics

MA9187

Radiation Hard 65536x1 Bit Static RAM
(Preliminary Data)

AC Characteristics

Conditions of Test for tables 5 and 6:
1. Input pulse = V_{SS} to 3.0V.
2. Times measurement reference level = 1.5V.
3. Input Rise and Fall times ≤ 5ns.
4. Output load 1TTL gate and CL = 60pF.
5. Transition is measured at ± 500mv from steady state.
6. This parameter is sampled and not 100% tested.

Notes for tables 5, 6 and 7:
Characteristics apply to pre radiation at T_A = -55°C to + 125°C with V_{DD} = 5V ± 10% and to post 300kRad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ± 10%.

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Read Cycle Time	70	-	ns
t_{AA}	Address Access Time	-	70	ns
t_{ACS}	Chip Select Access time	-	70	ns
t_{CLZ} (condition 5, 6)	Chip Selection to Output in Low Z	15	-	ns
t_{CHZ} (condition 5, 6)	Chip Deselection to Output in High Z	0	20	ns
t_{OH}	Output Hold from Address change	15	-	ns
t_{PU} (condition 6)	Chip Selection to Power-up Time	0	-	ns
t_{PD} (condition 6)	Chip Deselection to Power-down Time	-	35	ns

Table 5: Read Cycle AC Electrical Characteristics

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Write Cycle Time	50	-	ns
t_{CW}	Chip Selection to End of Write	45	-	ns
t_{AW}	Address Valid to End of Write	45	-	ns
t_{AS}	Address Set Up Time	0	-	ns
t_{WP}	Write Pulse Width	30	-	ns
t_{WR}	Write Recovery Time	0	-	ns
t_{WHZ} (condition 5)	Write to Output in High Z	0	20	ns
t_{DW}	Data to Write Time Overlap	25	-	ns
t_{DH}	Data Hold from Write	0	-	ns
t_{OW} (condition 5)	Output Active from End of Write	0	20	ns

Table 6: Write Cycle AC Electrical Characteristics

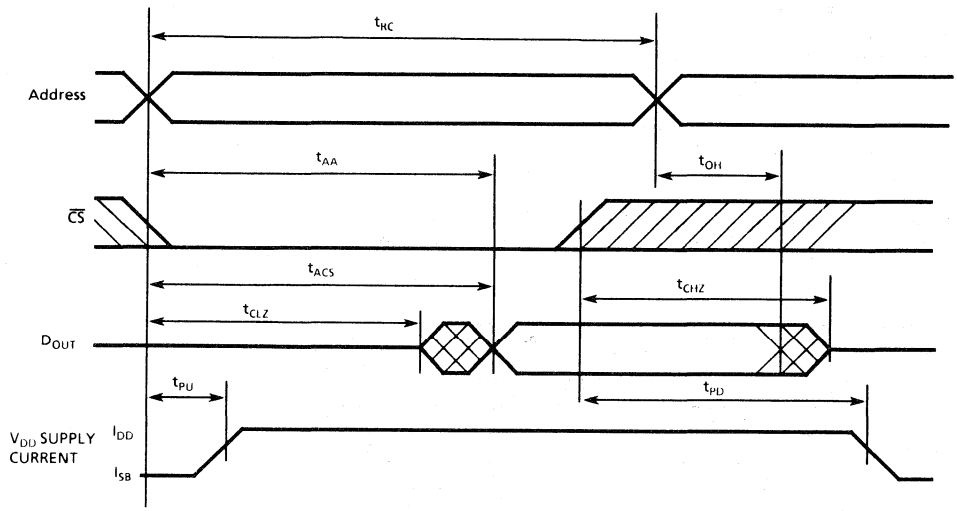
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	3	5	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	-	5	7	pF

Note: T_A = 25°C and f = 1MHz

Table 7: Capacitance

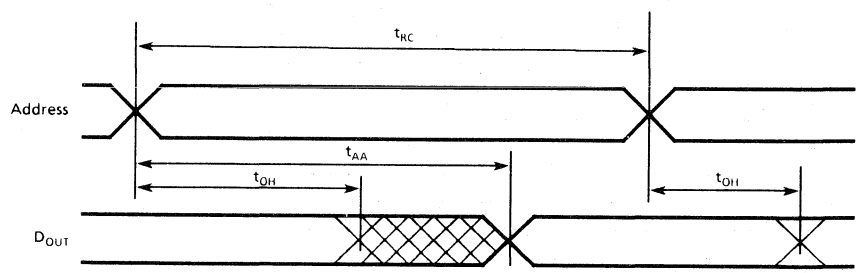
Radiation Hard 65536x1 Bit Static RAM
(Preliminary Data)

Read Cycle Timing Waveforms



1. $\overline{WE}$ is high for Read Cycle.
2. Address Valid prior to or coincident with $\overline{CS}$ transition low
3. When $\overline{CS}$ is low, the address input must not be in the high impedance state.

Figure 2: Read Cycle 1 Timing Waveforms



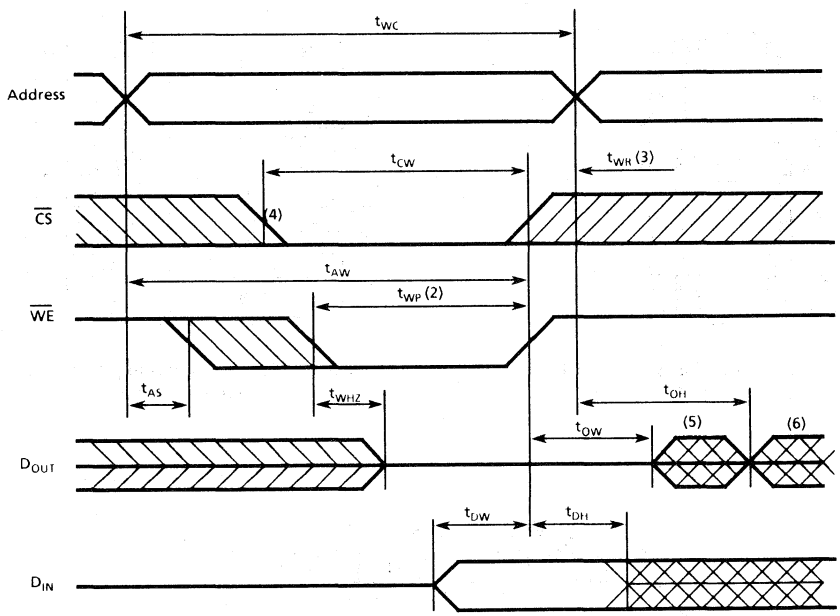
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected. $\overline{CS} = V_{IL}$
3. When $\overline{CS}$ is low, the address input must not be in the high impedance state.

Figure 3: Read Cycle 2 Timing Waveforms

MA9187

Radiation Hard 65536 x 1 Bit Static RAM
(Preliminary Data)

Write Cycle timing Waveforms



1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. D_{OUT} is identical to the write data in this cycle.
6. D_{OUT} is the read data of the next address.

Figure 4: Write Cyle Timing Waveforms

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Radiation Hard 65536 x 1 Bit Static RAM
(Preliminary Data)

Pin Assignments

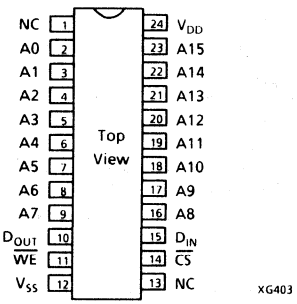


Figure 5: 24 lead Ceramic DIL (solder seal) Package style C

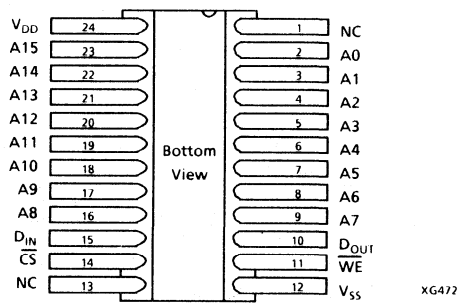


Figure 6: 24 lead Ceramic Flatpack(solder seal) Package style F

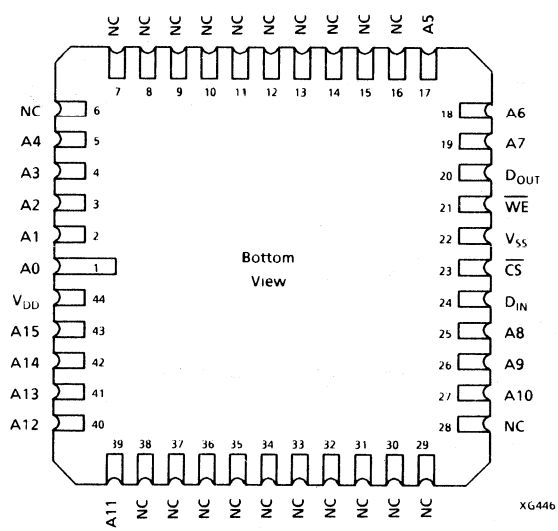
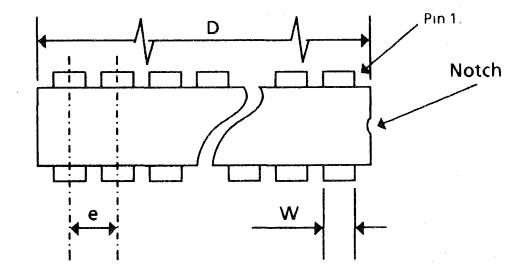


Figure 7: 44 Pad Leadless Chip Carrier - Package style L

MA9187

Radiation Hard 65536 x 1 Bit Static RAM
(Preliminary Data)

Package Outlines



Ref.	Min.	Nom.	Max.
A	-	-	5.60 (0.220)
A_1	0.38 (0.015)	-	1.53 (0.060)
b	0.35 (0.014)	-	0.59 (0.023)
c	0.20 (0.008)	-	0.36 (0.014)
D	-	-	30.79 (1.212)
e	-	2.54(0.100) typ	-
e_1	-	15.24(0.600) typ	-
H	4.71 (0.185)	-	5.38 (0.212)
M_E	-	-	15.90 (0.626)
Z	-	-	1.27 (0.050)
W	-	-	1.53 (0.060)
Dimensions in mm (inches)			

MEDL XG403

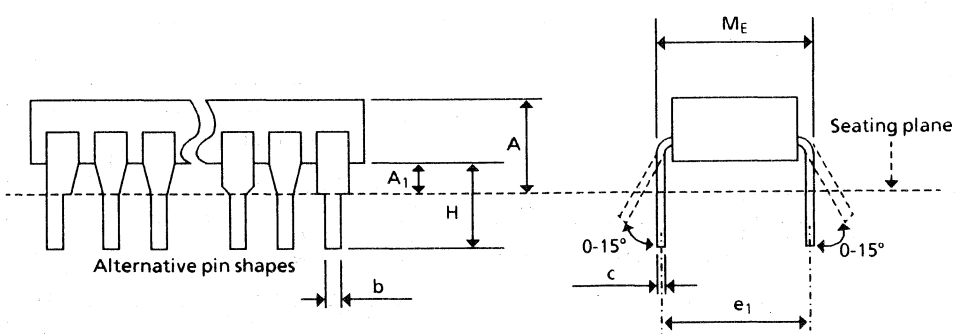
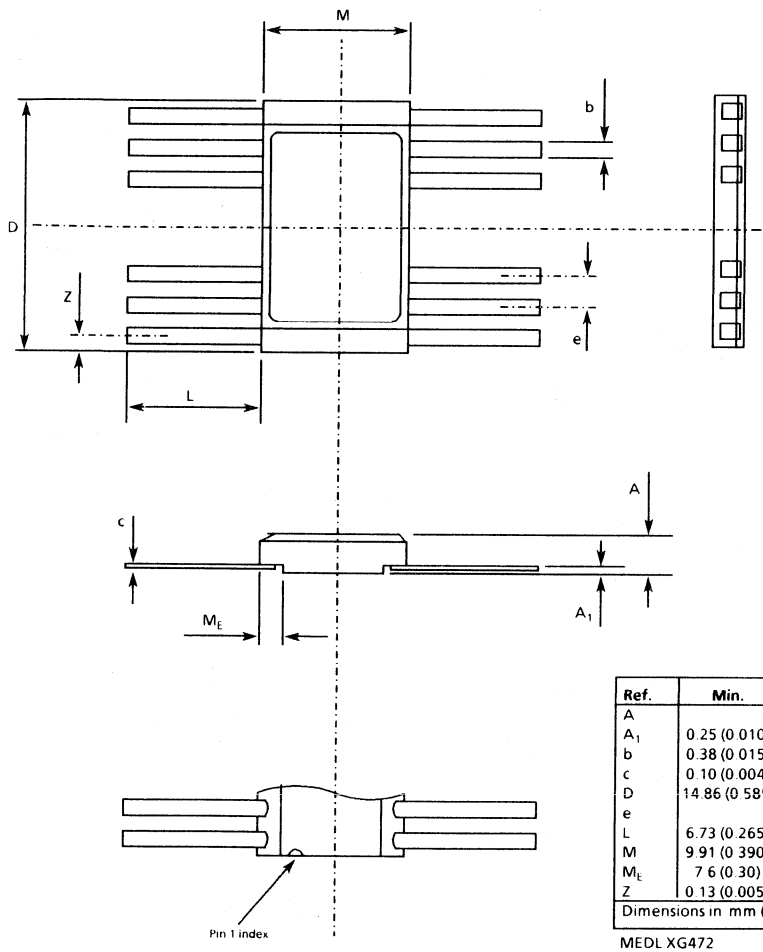


Figure 8: 24-Lead Ceramic DIL (solder seal) - package style C



Ref.	Min.	Nom.	Max.
A			2.67 (0.105)
A_1	0.25 (0.010)		1.02 (0.040)
b	0.38 (0.015)		0.48 (0.019)
c	0.10 (0.004)		0.18 (0.007)
D	14.86 (0.585)		15.62 (0.615)
e		2.54 (0.050)	
L	6.73 (0.265)		7.75 (0.305)
M	9.91 (0.390)		10.41 (0.410)
M_E	7.6 (0.30)		
Z	0.13 (0.005)		1.14 (0.045)

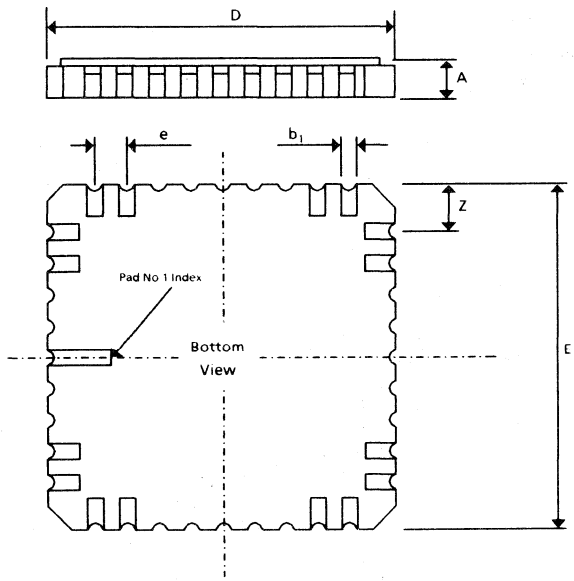
Dimensions in mm (inches)

MEDL XG472

Figure 9: 24-lead Ceramic Flatpack (solder seal) - Package style F

MA9187

Radiation Hard 65536 x 1 Bit Static RAM (Preliminary Data)



Ref.	Min.	Nom.	Max.
A			2.29 (0.090)
b_1		0.64 (0.025)	
D	16.33 (0.643)		16.81 (0.662)
E	16.33 (0.643)		16.81 (0.662)
e		1.27 (0.050)	
Z		1.91 (0.075) typ.	
Dimensions in mm (inches)			

MEDL XG446

Figure 10: 44-pad Leadless Chip Carrier (Package style L)

RadiationTolerance

Total Dose (Function)	$1x10^6$ Rad(Si)
Transient Upset (survivability)	$>10^{11}$ Rad(Si)/sec
Neutron Hardness	$>10^{15}$ neutrons/cm^2
Single Event Upset (GSO 10% worst case)	$4.3x10^{-11}$ errors/bitday
Latch-up	Not possible

Table 8: Radiation Tolerance

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet.

Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

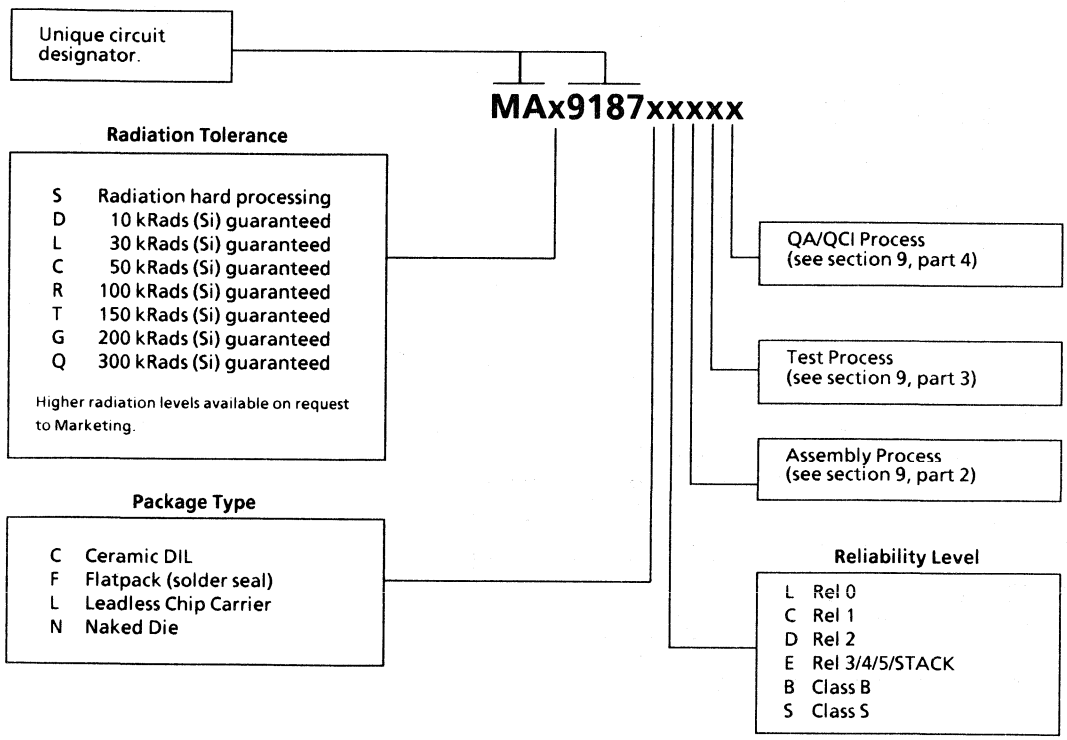
MA9187

GEC PLESSEY
SEMICONDUCTORS

Radiation Hard
65536 x 1 Bit Static RAM
(Preliminary Data)

Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



GEC PLESSEY

SEMICONDUCTORS

S10301ADS Issue 2.1 October 1990

MA9264

Radiation Hard 8192x8 Bit Static RAM

(Advance Data)

Features

- **1.5µm CMOS-SOS technology**
- **Latch up free**
- **Fast access time 45ns**
- **Total dose 10^6 rad (Si)**
- **Transient upset $>10^{11}$ rad (Si) /sec**
- **SEU $4.3x10^{-11}$ errors / bit day**
- **Single 5V supply**
- **Three state output**
- **Low standby current 100µA typical**
- **-55°C to + 125°C operation**

Block Diagram

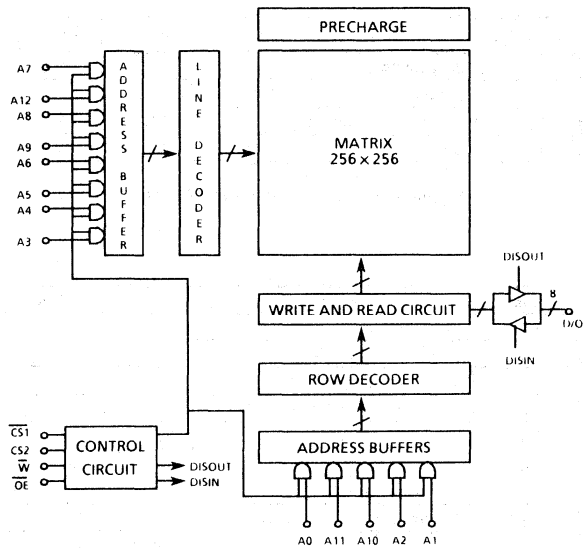


Figure 1: Block Diagram

General Description

The MA9264 64k Static RAM is configured as 8192x8 bits and manufactured using MEDL's CMOS-SOS high performance, radiation hard, 1.5µm technology.

The design uses a 6 transistor cell and has full static operation with no clock or timing strobe required. Address input buffers are deselected when chip select is in the HIGH state.

Operation mode	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{W}$	I/O	Power
Read	L	H	L	H	D OUT	ICCOP
Write	L	H	X	L	D IN	
Output disable	L	H	H	H	High Z	
Standby	H	X	X	X	High Z	ICCSB
	X	L	X	X		

Figure 2: Truth Table

Radiation Hard 8192x8 Bit Static RAM
(Advance Data)

DC Characteristics and Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0.5	7	V
V_I	Input voltage	-0.3	V_{DD} + 0.3	V
T_A	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Figure 3: Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	Logical '1' Input Voltage	-	2.0	-	V_{DD}	V
V_{IL}	Logical '0' Input Voltage	-	V_{SS}	-	0.8	V
V_{OH}	Logical '1' Output Voltage	I_{OH} = -2mA	2.4	-		V
V_{OL}	Logical '0' Output Voltage	I_{OL} = 4mA	-	-	0.4	V
I_{LI}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}, all inputs	-	-	± 10	µA
I_{LO}	Output Leakage Current	Chip disabled, V_{OUT} = V_{DD} or V_{SS}	-	-	± 10	µA
I_{DD1}	Selected Static Current(TTL)	All inputs = 3V except $\overline{CS}$ = <0.8V	-	14	30	mA
I_{DD2}	Selected Static Current(CMOS)	All inputs = V_{DD}-0.2V except $\overline{CS}$ = V_{SS} + 0.2V	-	100	2000	µA
I_{DD3}	Dynamic Operating Current (TTL)	f_{RC} = 1MHz, all inputs switching, V_{IH} = 3V	-	13	30	mA
I_{DD4}	Dynamic Operating Current (CMOS)	f_{RC} = 1MHz, all inputs switching, V_{IH} = V_{DD}-0.2V	-	8	16	mA
I_{SB1}	Standby Supply Current	$\overline{CS}$ = V_{DD}-0.2V	-	100	2000	µA

Note: The above characteristics apply to pre radiation at T_A = -55°C to + 125°C with V_{DD} = 5V ± 10% and to post 300kRad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ± 10%.

Figure 4: Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DR}	V_{CC} for Data Retention	$\overline{CS}$ = V_{DR}	2.0	-	-	V
I_{DDR}	Data Retention Current	$\overline{CS}$ = V_{DR}, V_{DR} = 2.0V	-	50	1000	µA

T_A = -55°C to + 125°C

Figure 5: Data Retention Characteristics

MA9264

Radiation Hard 8192x8 Bit Static RAM

(Advance Data)

AC Electrical Characteristics

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Read Cycle Time	70	-	ns
t_{AA}	Address Access Time	-	70	ns
t_{AC1}	Chip Select 1 access time	-	70	ns
t_{AC2}	Chip Select 2 access time	-	80	ns
t_{OL}	Output Enable to output valid time	-	15	ns
t_{CLZ} (Note 4)	Chip Select low to active output	-	30	ns
t_{CHZ} (Note 4)	Chip Select disable time	-	30	ns
t_{OHZ} (Note 4)	Output Enable to output in high Z	-	10	ns
t_{OH} (Note 4)	Output holdtime from address change	15	-	ns
t_{CP}	Chip select pulse width	70	-	ns

Figure 6: Read Cycle AC Electrical Characteristics

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Write Cycle Time	50	-	ns
t_{CW1}	Chip Select 1 to end of write	45	-	ns
t_{CW2}	Chip Select 2 to end of write	55	-	ns
t_{AW}	Address valid to end of write	45	-	ns
t_{AS}	Address set up time	5	-	ns
t_{WP}	Write pulse width	30	-	ns
t_{WR}	Address hold time/write recovery time	0	-	ns
t_{DW}	Input data valid to write high	25	-	ns
t_{DH}	Data hold from write time	5	-	ns
t_{WHZ} (Note 4)	Write low output in high Z	0	20	ns
t_{OW} (Note 4)	Output active from end of write	0	20	ns

Figure 7: Write Cycle AC Electrical Characteristics

Conditions of Test for figures 6 and 7:
1. Input pulse = V_{SS} to 3V.
2. Times measurement reference level = 1.5V.
3. Output load 1TTL gate and CL = 60pF.
4. Transition is measured at ± 500mv from steady state. This parameter is sampled and not 100% tested.
5. Input rise and fall times ≤ 5ns

Read Cycle Timing Waveforms

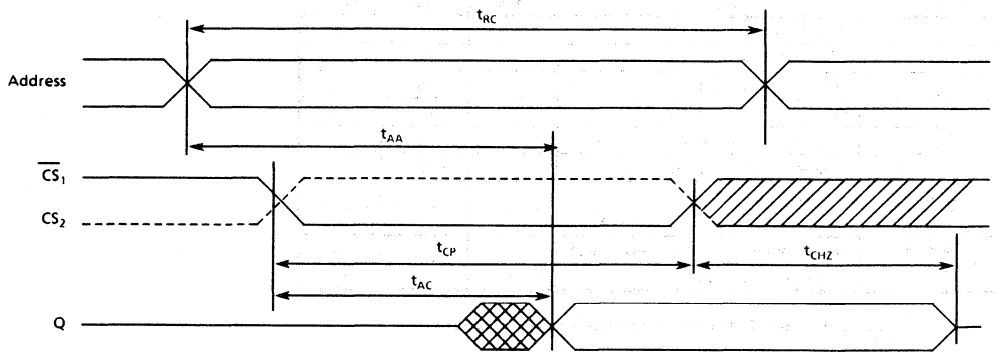


Figure 8: Cycle 1 (see notes 1, 3 and 4 below)

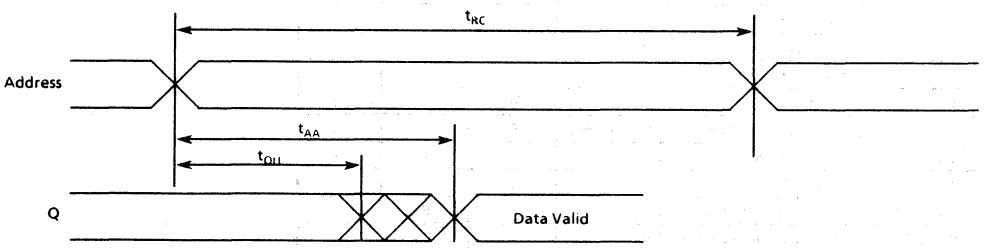


Figure 9: Cycle 2 (see notes 1, 2 and 4 below)

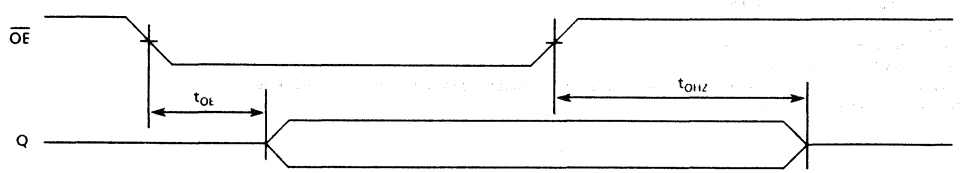


Figure 10: Cycle 3 (see notes 1, 3 and 4 below)

1 $\overline{W}$ must be high during address transitions.
2 Device is continuously selected, $\overline{CS}_1$ = V_{IL}, CS_2 = V_{IH}
3 Address Valid prior to or coincident with $\overline{CS}_1$ transition low.
4 When $\overline{CS}_1$ is low, the address must not be in the high impedance state

MA9264

Radiation Hard 8192x8 Bit Static RAM

(Advance Data)

Write Cycle Timing Waveforms

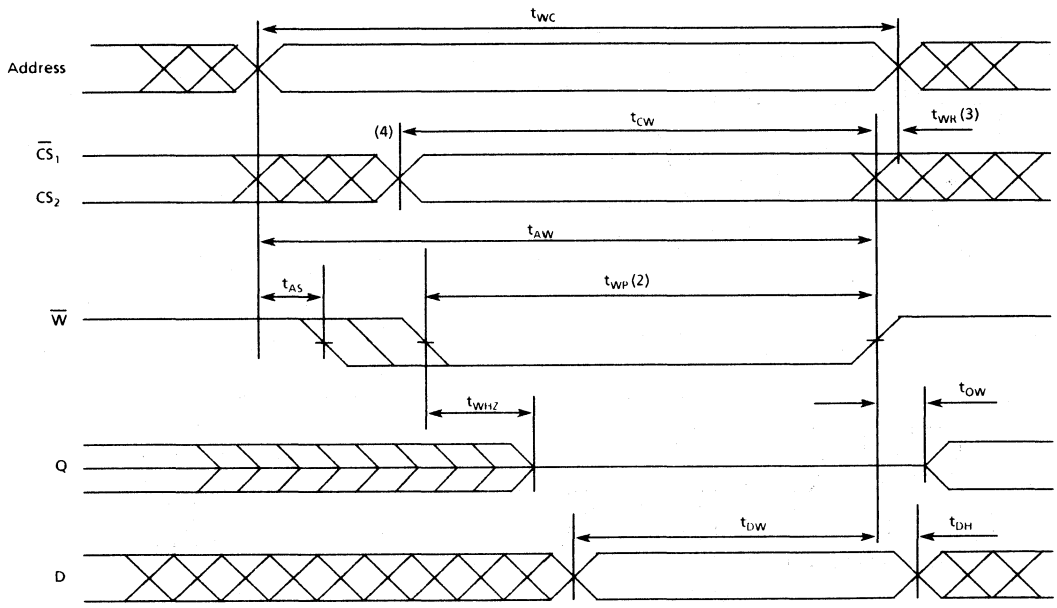


Figure 11: Write Cycle (see notes below)

1. $\overline{W}$ must be high during all address transitions
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{W}$.
3. t_{WR} is measured from either $\overline{CS}$ or $\overline{W}$ going high which ever is the earlier, to the end of the Write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously or after the $\overline{W}$ transition, the output remains a high impedance state.

Radiation Hard 8192x8 Bit Static RAM

(Advance Data)

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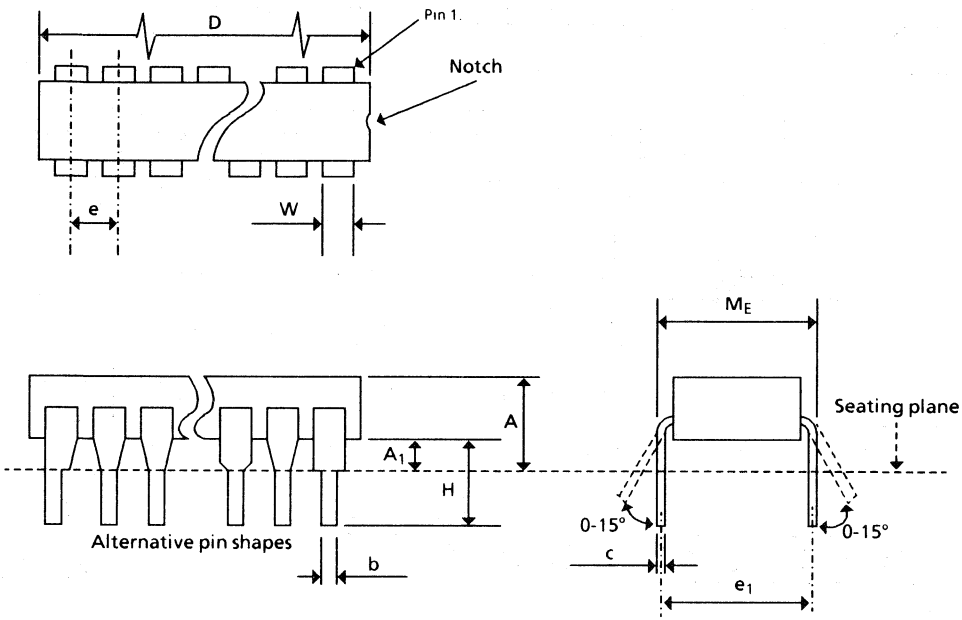
Outlines and Pin Assignments



Ref.	Min.	Nom.	Max.
A	-	-	5.60 (0.220)
A_1	0.38 (0.015)	-	1.53 (0.060)
b	0.35 (0.014)	-	0.59 (0.023)
c	0.20 (0.008)	-	0.36 (0.014)
D	-	-	36.02 (1.418)
e	-	2.54(0.100) typ.	-
e_1	-	15.24(0.600) typ.	-
H	4.71 (0.185)	-	5.38 (0.212)
M_E	-	-	15.90 (0.626)
W	-	-	1.53 (0.060)
Dimensions in mm (inches)			

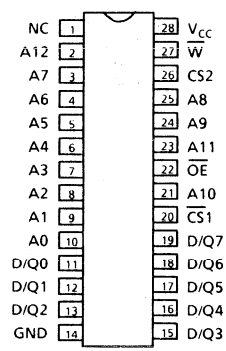
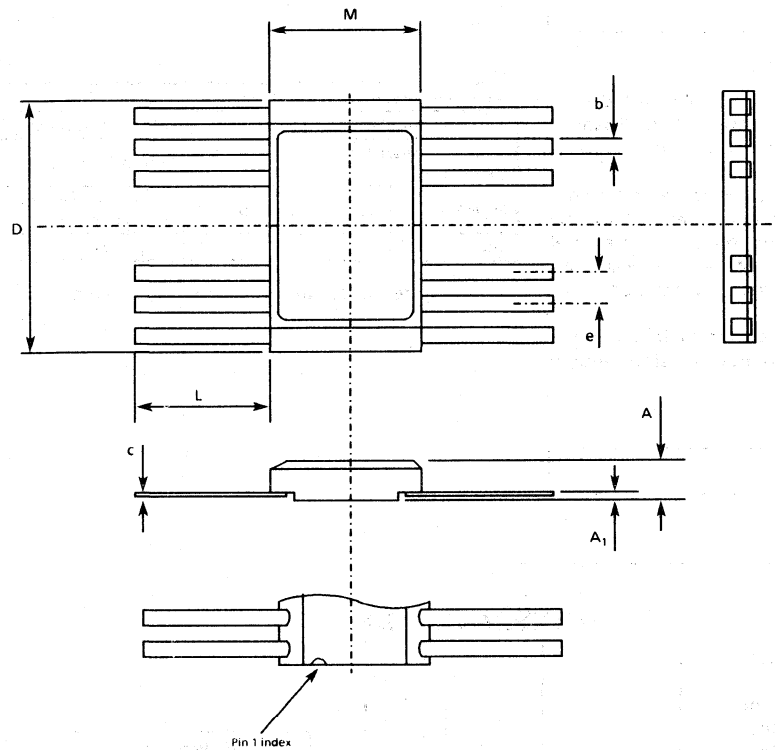


Figure 12: 28-Lead Ceramic DIL (solder seal) - package style C

MA9264

Radiation Hard 8192x8 Bit Static RAM

(Advance Data)



Ref.	Min.	Nom.	Max.
A	-	-	2.36 (0.093)
A_1	0.33 (0.013)	-	0.43 (0.017)
b	0.38 (0.015)	-	0.48 (0.019)
c	0.10 (0.004)	-	0.18 (0.007)
D	18.08 (0.712)	-	18.49 (0.728)
e	-	1.27 (0.050)	-
L	7.62 (0.300)	-	9.91 (0.390)
M	12.50 (0.492)	-	12.09 (0.508)
Dimensions in mm (inches)			

MEDL XG530

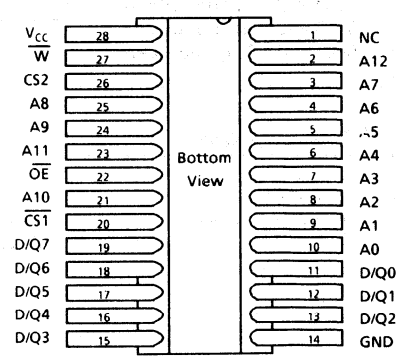


Figure 13: 28-lead Ceramic Flatpack (solder seal) - Package style F

Radiation Hard 8192x8 Bit Static RAM (Advance Data)

RadiationTolerance

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

Total Dose (Function to specification)	$1x10^6$ Rad(Si)
Transient Upset (Survivability)	$>1x10^{11}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ Rad(Si)/sec
Single Event Upset (GSO 10% worst case)	Upset free in all known space environmants
Latch-up	Not possible

Figure 14: Radiation Hardness Parameters

Ordering Information

Unique circuit designator.

MAx9264xxxxx

Radiation Tolerance

S	Radiation hard processing
R	100 kRads (Si) guaranteed
T	150 kRads (Si) guaranteed
Q	300 kRads (Si) guaranteed
H	1000 kRads (Si) guaranteed

Package Type

C	Ceramic DIL
F	Flatpack (solder seal)

QA/QCI Process (see section 9, part 4)

Test Process (see section 9, part 3)

Assembly Process (see section 9, part 2)

Reliability Level

L	Rel 0
C	Rel 1
D	Rel 2
E	Rel 3/4/5/STACK
B	Class B
S	Class S

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.

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SEMICONDUCTORS

MA9364

Radiation Hard 8192x8 Bit Static RAM

(Advance Data)

S10302ADS Issue 1.3 October 1990

Features

- **1.5µm CMOS-SOS technology**
- **Latch up free**
- **Fast access time 45ns**
- **Total dose 10^6 rad (Si)**
- **Transient upset $>10^{11}$ rad (Si) /sec**
- **SEU $4.3x10^{-11}$ errors / bit day**
- **Single 5V supply**
- **Three state output**
- **Low standby current 100µA typical**
- **-55°C to + 125°C operation**

Block Diagram

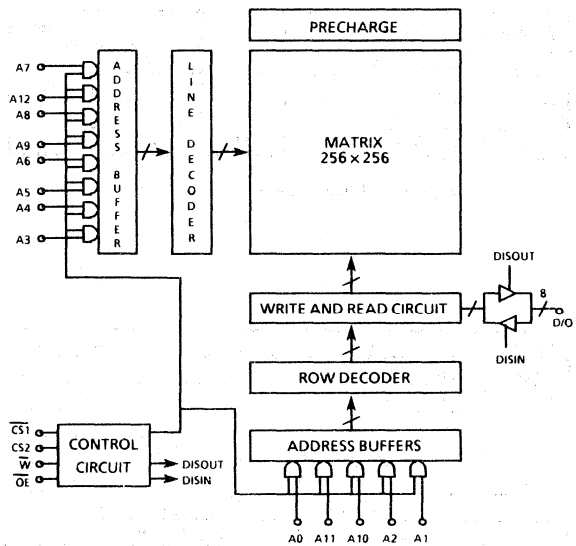


Figure 1: Block Diagram

General Description

The MA9364 64k Static RAM is configured as 8192x8 bits and manufactured using MEDL's CMOS-SOS high performance, radiation hard, 1.5µm technology.

The design uses a 6 transistor cell and has full static operation with no clock or timing strobe required. Address input buffers are deselected when chip select is in the HIGH state.

Operation mode	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{W}$	I/O	Power
Read	L	H	L	H	D OUT	ICCOP
Write	L	H	X	L	D IN	
Output disable	L	H	H	H	High Z	
Standby	H	X	X	X	High Z	ICCSB
	X	L	X	X		

Figure 2: Truth Table

5

Radiation Hard 8192x8 Bit Static RAM

(Advance Data)

DC Characteristics and Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0.5	7	V
V_I	Input voltage	-0.3	V_{DD} + 0.3	V
T_A	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Figure 3: Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	Logical '1' Input Voltage	-	0.8 V_{DD}	-	V_{DD}	V
V_{IL}	Logical '0' Input Voltage	-	V_{SS}	-	0.2 V_{DD}	V
V_{OH}	Logical '1' Output Voltage	I_{OH} = -2mA	V_{DD}-0.5	-		V
V_{OL}	Logical '0' Output Voltage	I_{OL} = 4mA	-	-	0.4	V
I_{LI}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}, all inputs	-	-	± 10	µA
I_{LO}	Output Leakage Current	Chip disabled, V_{OUT} = V_{DD} or V_{SS}	-	-	± 10	µA
I_{DD1}	Selected Static Current(CMOS)	All inputs = V_{DD}-0.2V except $\overline{CS}$ = V_{SS} + 0.2V	-	100	4000	µA
I_{DD2}	Dynamic Operating Current (CMOS)	f_{RC} = 1MHz, all inputs switching, V_{IH} = V_{DD}-0.2V	-	8	16	mA
I_{SB1}	Standby Supply Current	$\overline{CS}$ = V_{DD}-0.2V	-	100	4000	µA

Note: The above characteristics apply to pre radiation at T_A = -55°C to + 125°C with V_{DD} = 5V ± 10% and to post 300kRad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ± 10%.

Figure 4: Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DR}	V_{CC} for Data Retention	$\overline{CS}$ = V_{DR}	2.0	-	-	V
I_{DDR}	Data Retention Current	$\overline{CS}$ = V_{DR}, V_{DR} = 2.0V	-	50	1500	µA

T_A = -55°C to + 125°C

Figure 5: Data Retention Characteristics

MA9364

Radiation Hard 8192x8 Bit Static RAM

(Advance Data)

AC Electrical Characteristics

Conditions of Test for figures 6 and 7:
1. Input pulse = V_{SS} to 3V.
2. Times measurement reference level = 1.5V.
3. Output load 1TTL gate and CL = 60pF.
4. Transition is measured at ± 500mv from steady state. This parameter is sampled and not 100% tested.
5. Input rise and fall times ≤ 5ns

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Read Cycle Time	70	-	ns
t_{AA}	Address Access Time	-	70	ns
t_{AC1}	Chip Select 1 access time	-	70	ns
t_{AC2}	Chip Select 2 access time	-	80	ns
t_{OE}	Output Enable to output valid time	-	15	ns
t_{CLZ} (Note 4)	Chip Select low to active output	-	30	ns
t_{CHZ} (Note 4)	Chip Select disable time	-	30	ns
t_{OHZ} (Note 4)	Output Enable to output in high Z	-	10	ns
t_{OH} (Note 4)	Output holdtime from address change	15	-	ns
t_{CP}	Chip select pulse width	70	-	ns

Figure 6: Read Cycle AC Electrical Characteristics

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Write Cycle Time	50	-	ns
t_{CW1}	Chip Select 1 to end of write	45	-	ns
t_{CW2}	Chip Select 2 to end of write	55	-	ns
t_{AW}	Address valid to end of write	45	-	ns
t_{AS}	Address set up time	5	-	ns
t_{WP}	Write pulse width	30	-	ns
t_{WR}	Address hold time/write recovery time	0	-	ns
t_{DW}	Input data valid to write high	25	-	ns
t_{DH}	Data hold from write time	5	-	ns
t_{WHZ} (Note 4)	Write low output in high Z	0	20	ns
t_{OW} (Note 4)	Output active from end of write	0	20	ns

Figure 7: Write Cycle AC Electrical Characteristics

Read Cycle Timing Waveforms

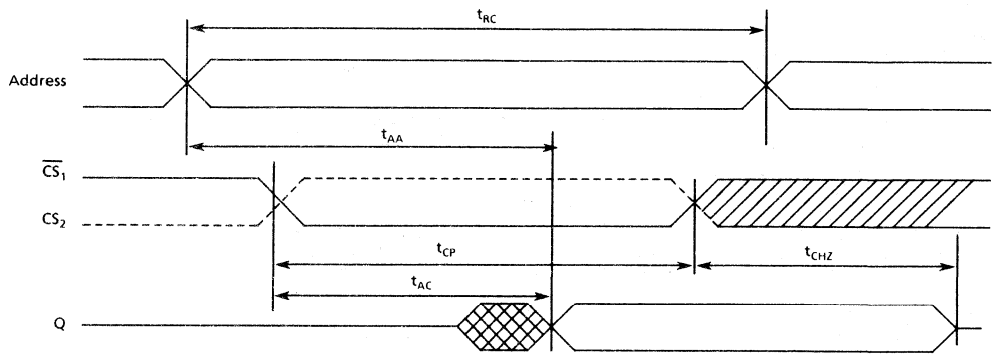


Figure 8: Cycle 1 (see notes 1, 3 and 4 below)

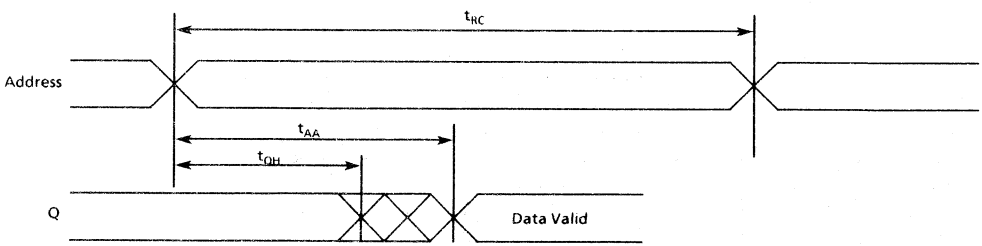


Figure 9: Cycle 2 (see notes 1, 2 and 4 below)

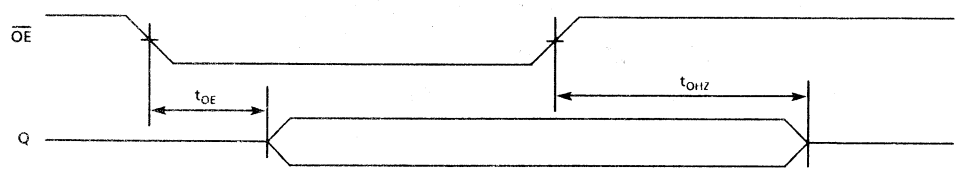


Figure 10: Cycle 3 (see notes 1, 3 and 4 below)

NOTES:
1. $\overline{W}$ must be high during address transitions.
2. Device is continuously selected, $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}
3. Address Valid prior to or coincident with $\overline{CS_1}$ transition low.
4. When $\overline{CS_1}$ is low, the address must not be in the high impedance state.

MA9364

Radiation Hard 8192x8 Bit Static RAM

(Advance Data)

Write Cycle Timing Waveforms

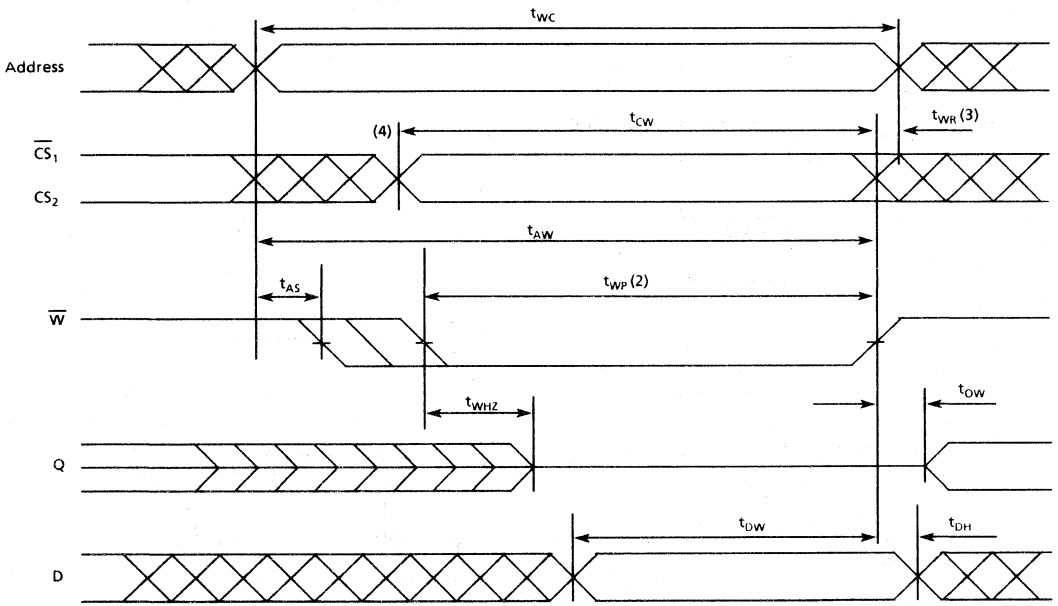


Figure 11: Write Cycle (see notes below)

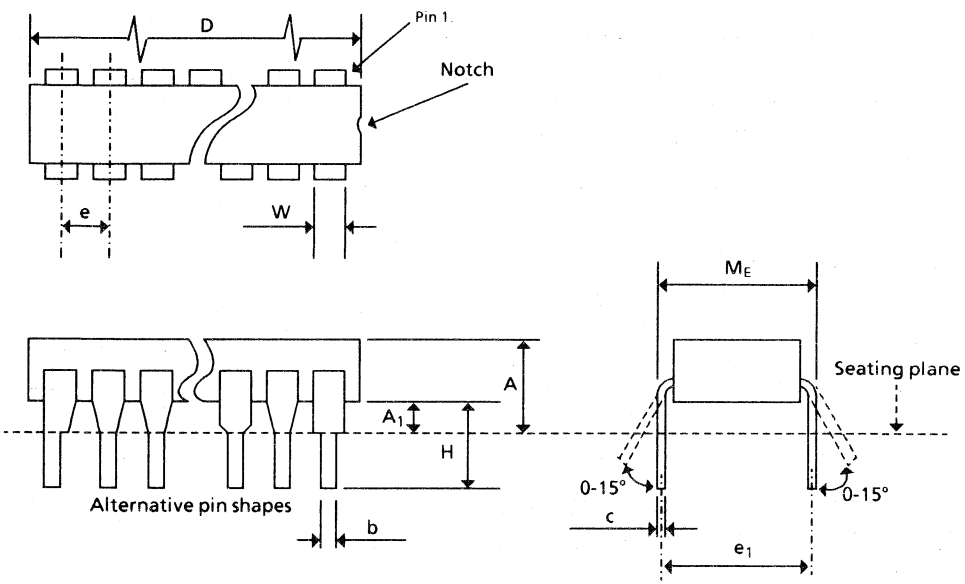
NOTES:
1. $\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS_1}$ and a low $\overline{W}$.
3. t_{WR} is measured from either $\overline{CS_1}$ or $\overline{W}$ going high which ever is the earlier, to the end of the Write cycle.
4. If the $\overline{CS_1}$ low transition occurs simultaneously or after the $\overline{W}$ transition, the output remains a high impedance state.

5

Radiation Hard 8192x8 Bit Static RAM

(Advance Data)

Outlines and Pin Assignments



Ref.	Min.	Nom.	Max.
A	-	-	5.60 (0.220)
A_1	0.38 (0.015)	-	1.53 (0.060)
b	0.35 (0.014)	-	0.59 (0.023)
c	0.20 (0.008)	-	0.36 (0.014)
D	-	-	36.02 (1.418)
e	-	2.54(0.100) typ.	-
e_1	-	15.24(0.600) typ.	-
H	4.71 (0.185)	-	5.38 (0.212)
M_E	-	-	15.90 (0.626)
W	-	-	1.53 (0.060)
Dimensions in mm (inches)			

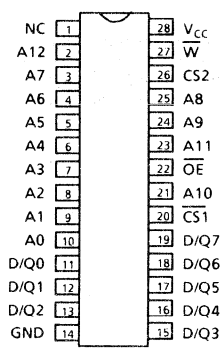
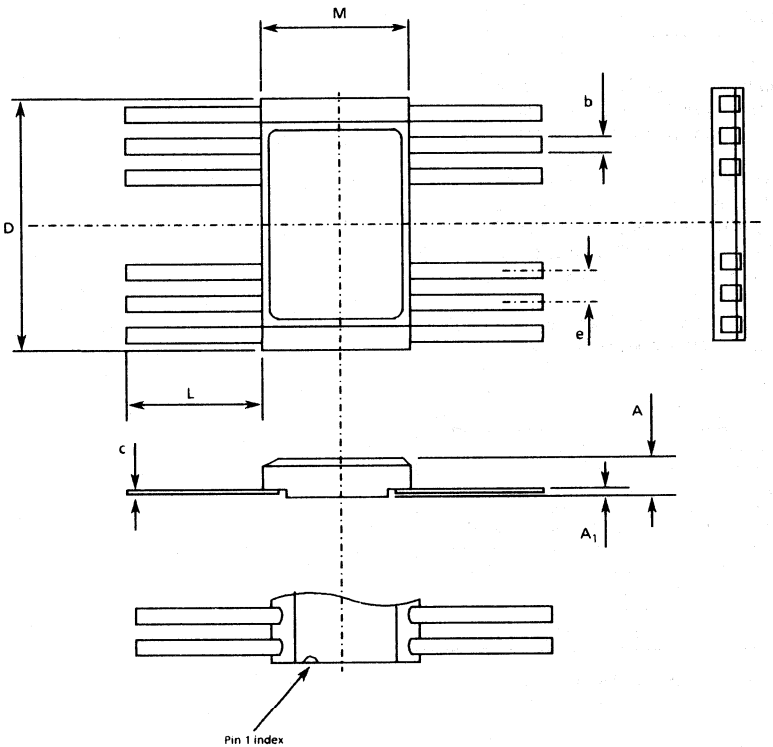


Figure 12: 28-Lead Ceramic DIL (solder seal) - package style C

MA9364

Radiation Hard 8192x8 Bit Static RAM

(Advance Data)



Ref.	Min.	Nom.	Max.
A			2.36 (0.093)
A_1	0.33 (0.013)		0.43 (0.017)
b	0.38 (0.015)		0.48 (0.019)
c	0.10 (0.004)		0.18 (0.007)
D	18.08 (0.712)		18.49 (0.728)
e		1.27 (0.050)	
L	7.62 (0.300)		9.91 (0.390)
M	12.50 (0.492)		12.09 (0.508)
Dimensions in mm (inches)			

MEDL XG530

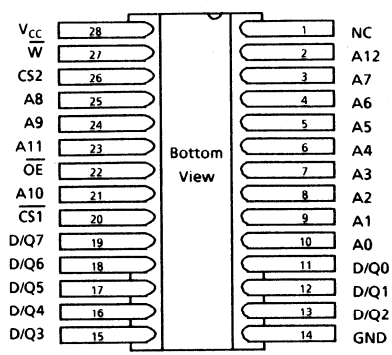


Figure 13: 28-lead Ceramic Flatpack (solder seal) - Package style F

Radiation Hard 8192x8 Bit Static RAM
(Advance Data)

RadiationTolerance

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

Total Dose (Function to specification)	$1x10^6$ Rad(Si)
Transient Upset (survivability)	$>1x10^{11}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ neutrons/cm^2
Single Event Upset (GSO 10% worst case)	Upset free in all known space environments
Latch-up	Not possible

Figure 14: Radiation Hardness Parameters

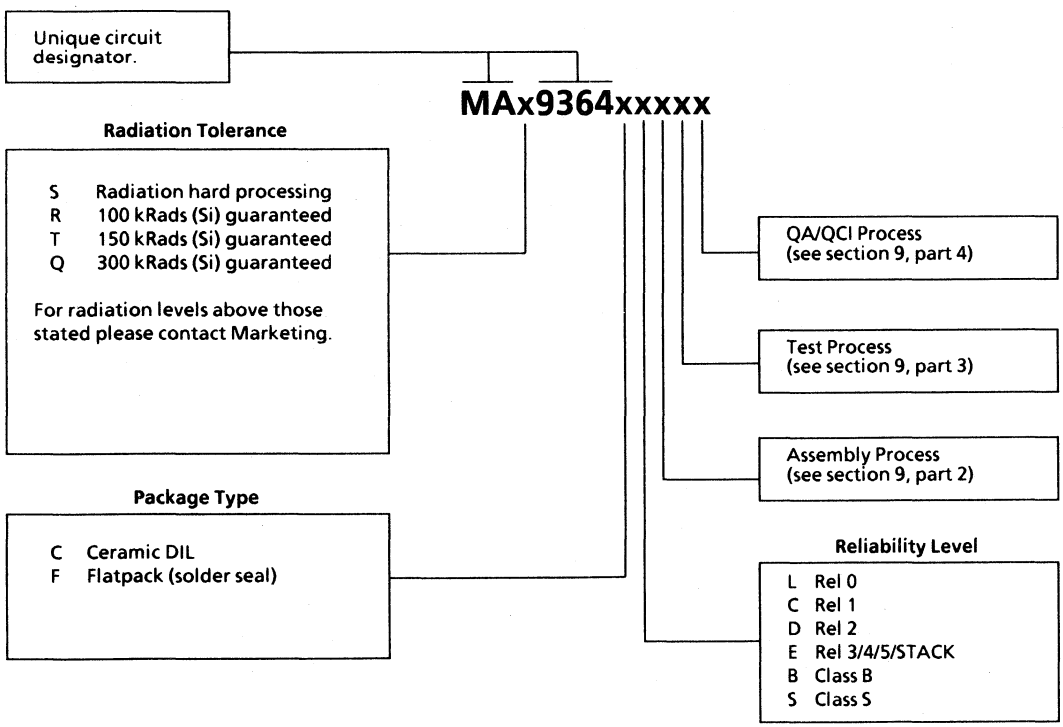
MA9364

Radiation Hard 8192x8 Bit Static RAM

(Advance Data)

Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



MA9287

Radiation Hard 65536x1 Bit Static RAM
(Preliminary Data)

S10303PDS Issue 2.3 October 1990

Features

- 1.5µm CMOS-SOS technology
- Latch-up free
- Fast access time 45ns typical
- Total dose 10^6 rad (Si)
- Transient upset > 10^{11} rad (Si) /sec
- SEU 4.3×10^{-11} errors/bit day
- Single 5V supply
- All Inputs & outputs fully CMOS compatible
- Fully static operation
- Three state output
- Low standby current 100µA typical
- -55°C to + 125°C operation

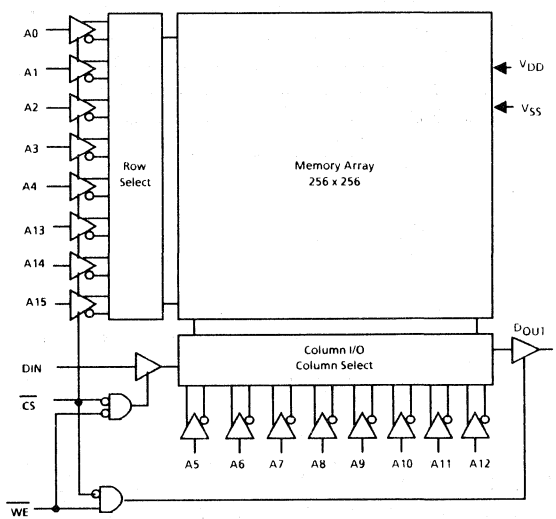


Figure 1: Block Diagarm

General Description

The MA9287 64k Static RAM is configured as 65536x1 bits and manufactured using MEDL's CMOS-SOS high performance, radiation hard, 1.5µm technology.

The device has separate input and output terminals controlled by Chip Select and Write Enable. The design uses a 6 transistor cell and has full static operation with no clock or timing strobe required. Address input buffers are deselected when Chip Select is in the high state.

$\overline{CS}$	$\overline{WE}$	Mode	V_{DD} Current	Output Pin
H	X	Deselected	I_{SBI}	High Z
L	H	Read	I_{DD}	D_{OUT}
L	L	Write	I_{DD}	High Z

Table 1: Truth Table

5

GEC PLESSEY

SEMICONDUCTORS

Radiation Hard 65536x1 Bit Static RAM
(Preliminary Data)

DC Ratings and Characteristics

Parameter	Min.	Max.	Units
Supply voltage	-0.5	7	V
Input voltage	-0.3	V_{DD} + 0.3	V
Operating temperature	-55	125	°C
Storage temperature	-65	150	°C

Table 2: Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes for tables 3 and 4: Characteristics apply to pre radiation at T_A = -55°C to + 125°C with V_{DD} = 5V ± 10% and to post 300kRad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ± 10%

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	Logical '1' Input Voltage	-	0.8V_{DD}	-	V_{DD}	V
V_{IL}	Logical '0' Input Voltage	-	V_{SS}	-	0.2V_{DD}	V
V_{OH}	Logical '1' Output Voltage	I_{OH} = -3mA	V_{DD}-0.5	-		V
V_{OL}	Logical '0' Output Voltage	I_{OL} = 8mA	-	-	0.4	V
I_{LI}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS} All inputs	-	-	± 10	µA
I_{LO}	Output Leakage Current	Chip disabled, V_{OUT} = V_{DD} or V_{SS}	-	-	± 10	µA
I_{DD1}	Selected Static Current(CMOS)	All inputs = V_{DD}-0.2V except $\overline{CS}$ = V_{SS} + 0.2v	-	100	4000	µA
I_{DD2}	Dynamic Operating Current (CMOS)	f_{RC} = 1MHz, all inputs switching, V_{IH} = V_{DD}-0.2V	-	3	7	mA
I_{SB1}	Standby Supply Current	$\overline{CS}$ = V_{DD}-0.2V	-	100	4000	µA

Table 3: Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DR}	V_{CC} for Data Retention	$\overline{CS}$ = V_{DR}	2.0	-	-	V
I_{DDR}	Data Retention Current	$\overline{CS}$ = V_{DR}, V_{DR} = 2.0V	-	50	1500	µA

Table 4: Data Retention Characteristics

AC Characteristics

Conditions of Test for tables 5 and 6:
1. Input pulse = V_{SS} to $0.8V_{DD}$.
2. Times measurement reference level = 1.5V.
3. Input Rise and Fall times ≤ 5ns.
4. Output load 1TTL gate and CL = 60pF.
5. Transition is measured at ±500mv from steady state.
6. This parameter is sampled and not 100% tested.

Notes for tables 5, 6 and 7:
Characteristics apply to pre-radiation at T_A = -55°C to + 125°C with V_{DD} = 5V ± 10% and to post 300k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ± 10%

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Read Cycle Time	70	-	ns
t_{AA}	Address Access Time	-	70	ns
t_{ACS}	Chip select Access time	-	70	ns
t_{CLZ} (note 5, 6)	Chip Selection to Output in Low Z	15	-	ns
t_{CHZ} (note 5, 6)	Chip Deselection to Output in High Z	0	20	ns
t_{OH}	Output Hold from Address change	15	-	ns
t_{PU} (note 6)	Chip Selection to Power-up Time	0	-	ns
t_{PD} (not 6)	Chip Deselection to Power-down Time	-	35	ns

Table 5: Read Cycle AC Electrical Characteristics

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Write Cycle Time	50	-	ns
t_{CW}	Chip Selection to End of Write	45	-	ns
t_{AW}	Address Valid to End of Write	45	-	ns
t_{AS}	Address Set Up Time	0	-	ns
t_{WP}	Write Pulse Width	30	-	ns
t_{WR}	Write Recovery Time	0	-	ns
t_{WHZ} (note 5)	Write to Output in High Z	0	20	ns
t_{DW}	Data to Write Time Overlap	25	-	ns
t_{DH}	Data Hold from Write	0	-	ns
t_{OW} (note 5)	Output Active from End to Write	0	20	ns

Table 6: Write Cycle AC Electrical Characteristics

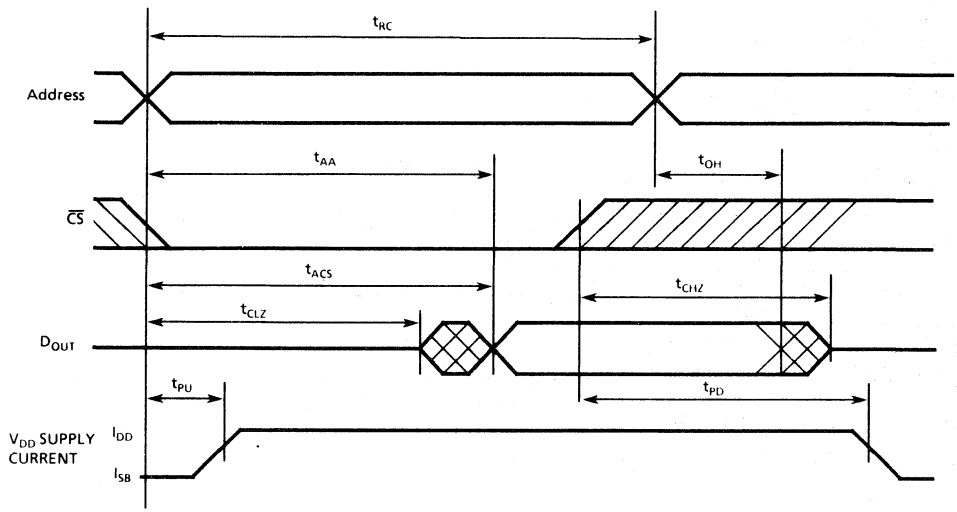
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	3	5	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	-	5	7	pF

Note. T_A = 25°C and f = 1MHz

Table 7: Capacitance

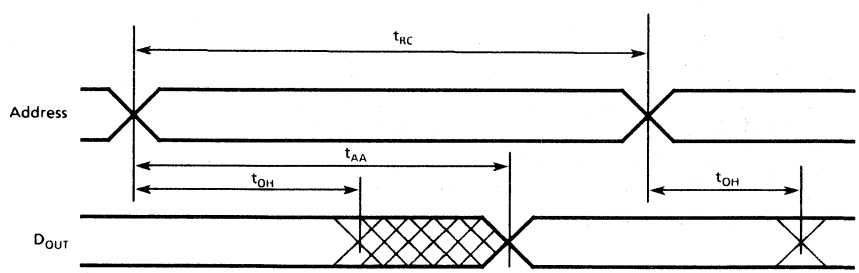
Radiation Hard 65536x1 Bit Static RAM
(Preliminary Data)

Timing Waveforms



1. $\overline{WE}$ is high for Read Cycle.
2. Address Valid prior to or coincident with $\overline{CS}$ transition low.
3. When $\overline{CS}$ is low, the address input must not be in the high impedance state.

Figure 2: Read Cycle 1

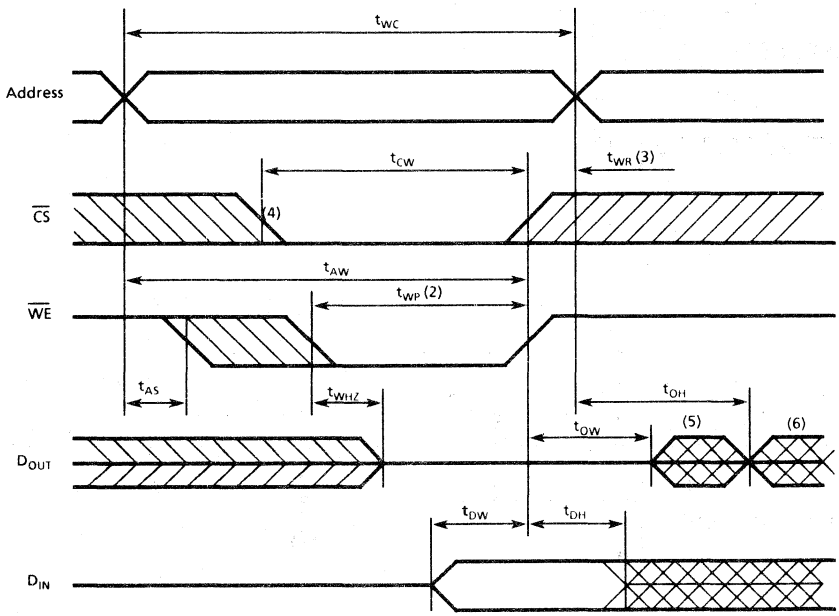


1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected. $\overline{CS} = V_{IL}$
3. When $\overline{CS}$ is low, the address input must not be in the high impedance state.

Figure 3: Read Cycle 2

MA9287

Radiation Hard 65536 x 1 Bit Static RAM
(Preliminary Data)



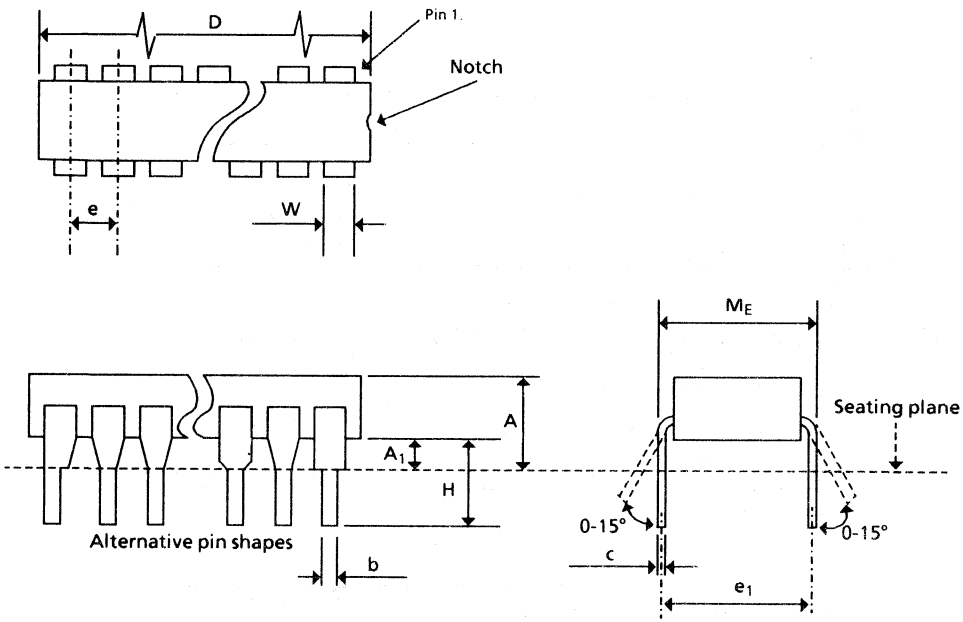
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with the WE low transitions or after the WE transition, output remain in a high impedance state.
5. D_{OUT} is identical to the write data in this cycle.
6. D_{OUT} is the read data of the next address.

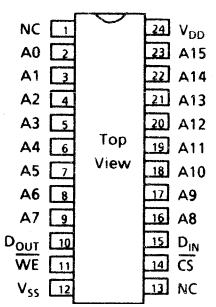
Figure 4: Write Cyle

Radiation Hard 65536 x 1 Bit Static RAM
(Preliminary Data)

GEC PLESSEY
SEMICONDUCTORS

Outlines and Pin Assignments





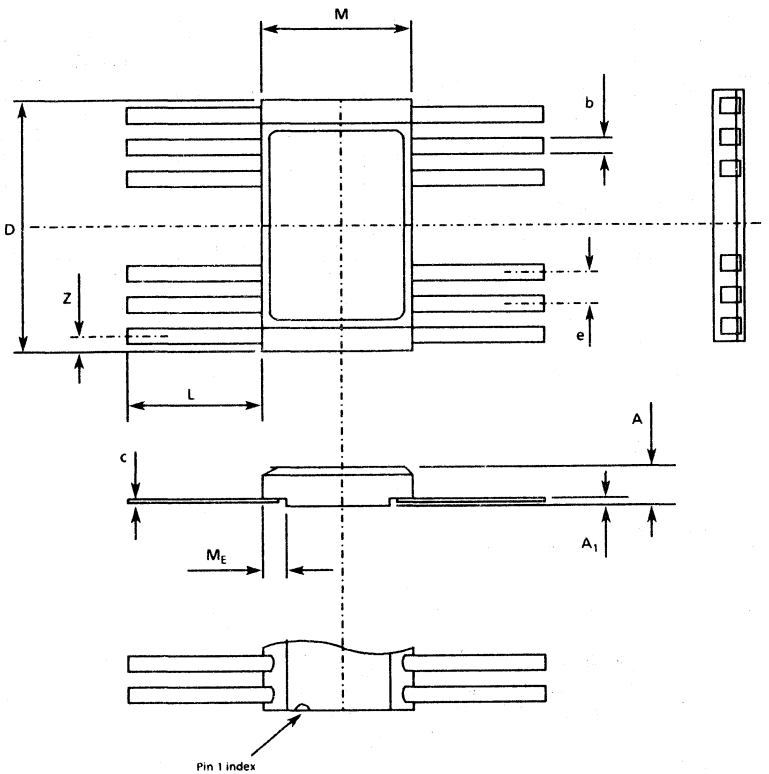
Ref.	Min.	Nom.	Max.
A	-	-	5.60 (0.220)
A_1	0.38 (0.015)	-	1.53 (0.060)
b	0.35 (0.014)	-	0.59 (0.023)
c	0.20 (0.008)	-	0.36 (0.014)
D	-	-	30.79 (1.212)
e	-	2.54(0.100) typ.	-
e_1	-	15.24(0.600) typ.	-
H	4.71 (0.185)	-	5.38 (0.212)
M_E	-	-	15.90 (0.626)
Z	-	-	1.27 (0.050)
W	-	-	1.53 (0.060)
Dimensions in mm (inches)			

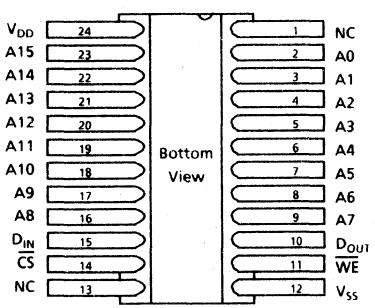
MEDL XG403

Figure 5: 24-Lead Ceramic DIL (solder seal) - package style C

MA9287

Radiation Hard
65536 x 1 Bit Static RAM
(Preliminary Data)





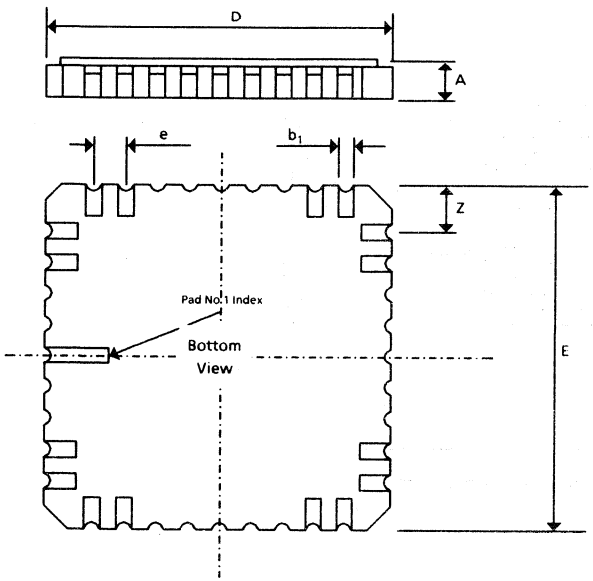
Ref.	Min.	Nom.	Max.
A			2.67 (0.105)
A_1	0.25 (0.010)		1.02 (0.040)
b	0.38 (0.015)		0.48 (0.019)
c	0.10 (0.004)		0.18 (0.007)
D	14.86 (0.585)		15.62 (0.615)
e		2.54 (0.050)	
L	6.73 (0.265)		7.75 (0.305)
M	9.91 (0.390)		10.41 (0.410)
M_E	7.6 (0.30)		
Z	0.13 (0.005)		1.14 (0.045)

Dimensions in mm (inches)

MEDL XG472

Figure 6: 24-lead Ceramic Flatpack (solder seal) - Package style F

Radiation Hard 65536 x 1 Bit Static RAM
(Preliminary Data)



Ref.	Min.	Nom.	Max.
A			2.29 (0.090)
b_1		0.64 (0.025)	
D	16.33 (0.643)		16.81 (0.662)
E	16.33 (0.643)		16.81 (0.662)
e		1.27 (0.050)	
Z		1.91 (0.075) typ.	

Dimensions in mm (inches)

MEDL XG446

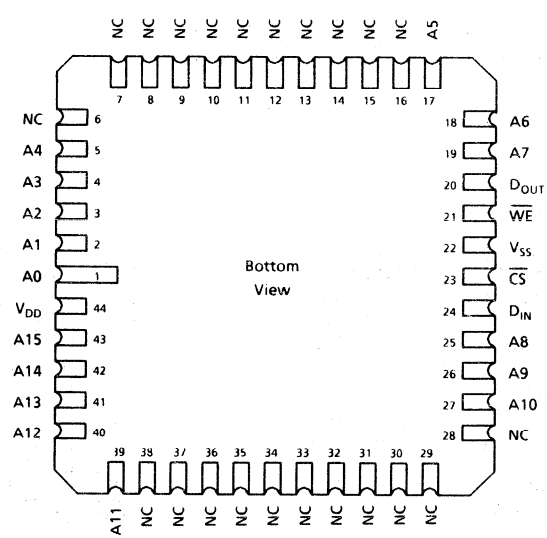


Figure 7: 44-pad Leadless Chip Carrier (Package style L)

MA9287

Radiation Hard 65536 x 1 Bit Static RAM
(Preliminary Data)

RadiationTolerance

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

Total Dose (Function to specification)	$1x10^{6}$ Rad(Si)
Transient Upset (survivability)	$>10^{11}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>10^{15}$ neutrons/cm^2
Single Event Upset (GSO 10% worst case)	$4.3x10^{-11}$ errors/bitday
Latch-up	Not possible

Table 8: Radiation Hardness Parameters

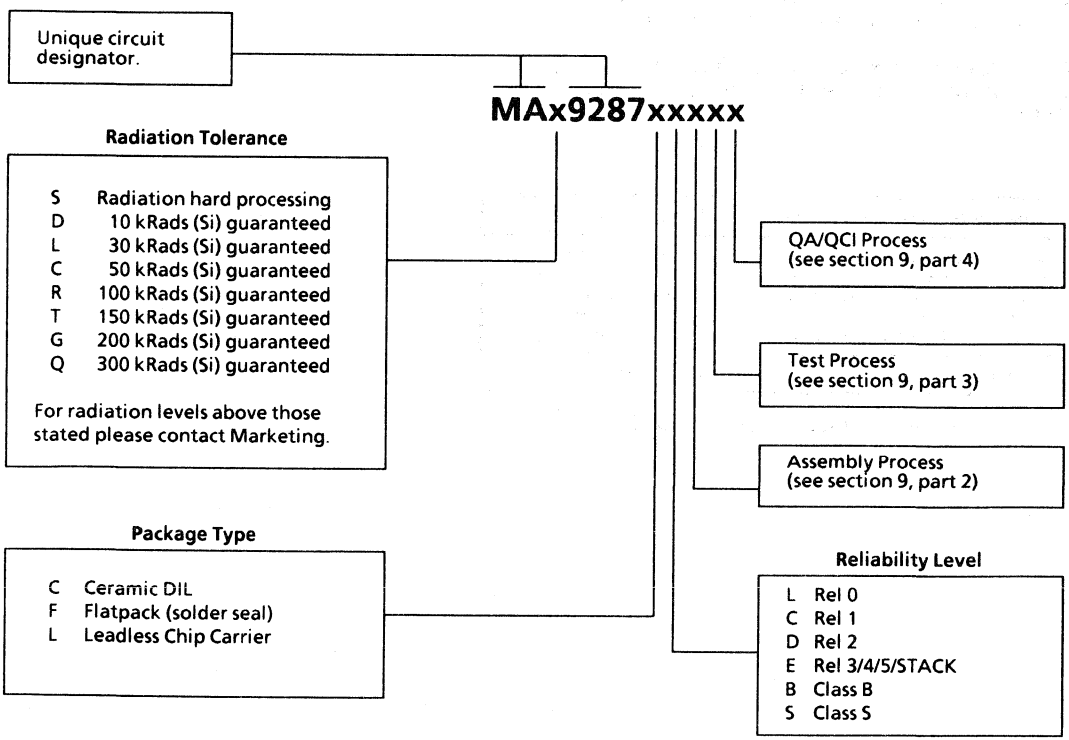
MA9287

GEC PLESSEY
SEMICONDUCTORS

Radiation Hard
65536 x 1 Bit Static RAM
(Preliminary Data)

Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



GEC PLESSEY

SEMICONDUCTORS

MA7001

Radiation Hard 512 x 9 Bit FIFO

S11000FDS/2 Issue 2.4 December 1990

Features

- **Radiation hard CMOS-SOS technology**
- **Fast access time 60ns typical**
- **Single 5V supply**
- **Inputs fully TTL and CMOS compatible**
- **-55°C to + 125°C operation**

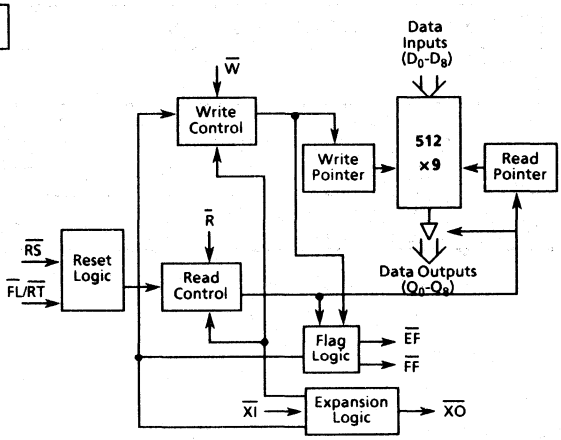


Figure 1: Block Diagarm

General Description

The MA7001 512 x 9 FIFO is manufactured using MEDL's CMOS-SOS high performance, radiation hard, 3µm technology.

The MEDL Silicon-on-Sapphire process provides significant advantages over bulk silicon substrate technologies. In addition to very good total dose hardness and neutron hardness $>10^{15}$n/cm^2, the MEDL technology provides very high transient gamma and single event upset performance without compromising speed of operation. The Sapphire substrate also eliminates latch-up giving greater flexibility of use in electrically severe environments.

The MA7001 implements a First-In First-Out algorithm that reads and writes data on a first-in first-out basis. The dual-port static RAM memory is organised as 512 words of 9 bits (8 bit data and 1 bit for parity or control purposes).

Sequential read and write accesses are achieved using a ring pointer architecture that requires no external addressing information. Data is toggled in and out of the device by using the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins.

Full and Empty status flags prevent data overflow and underflow. Expansion logic on the device allows for unlimited expansion capability in both word size and depth. A RETRANSMIT ($\overline{RT}$) feature allows for reset of the read pointer to its initial position to allow retransmission of data.

The device is designed for applications requiring asynchronous and simultaneous read/write in multi-processing and rate buffering (sourcing and sinking data at different rates e.g. interfacing fast processors and slow peripherals).

5

DC Characteristics and Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0.5	7.0	V
V_{IN}	Input voltage	-0.3	V_{DD} + 0.3	V
T_A	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 2: Absolute Maximum Ratings

The following D.C. and A.C. electrical characteristics apply to pre-radiation at T_A = -55°C to + 125°C, V_{DD} = 5V ± 10% and post 100kRad(Si) total dose radiation at T_A = 25°C, V_{DD} = 5V ± 10%.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input logic '1' voltage	-	2.0	-	-	V
V_{IL}	Input logic '0' voltage	-	-	-	0.8	V
I_{IL}	Input leakage current (any input) (Note 1)	Note 4	-10	-	10	µA
I_{OL}	Output leakage current (Note 2)	Note 4	-50	-	50	µA
V_{OH}	Output logic '1' voltage	I_{OUT} = -1mA	2.4	-	-	V
V_{OL}	Output logic '0' voltage	I_{OUT} = 2mA	-	-	0.4	V
I_{DD1}	Average V_{DD} power supply current (Note 3)	Freq = 10MHz	-	70	100	mA
I_{DD2}	Average standby current (Note 3)	$\overline{R} = \overline{W} = \overline{RS} = \overline{FL/RT} = V_{IH}$	-	8	15	mA
$I_{DD3(L)}$	Power down current (Note 3)	All inputs = V_{DD}-0.2V	-	-	3.0	mA

NOTES:
1. Measurements with $V_{SS} \leq V_{IN} \leq V_{DD}$.
2. $\overline{R} > V_{IH}$, $V_{SS} \leq V_{OUT} \leq V_{DD}$.
3. I_{DD} measurements are made with outputs open, V_{DD} = 5.5V.
4. Guaranteed but not measured at -55°C.

Figure 3: DC Electrical Characteristics

AC Characteristics

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Read Cycle Time	100	-	ns
t_A	Access Time	-	90	ns
t_{RR}	Read Recovery Time	20	-	ns
t_{RPW}	Read Pulse Width (Note 2)	80	-	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z (Note 3)	10	-	ns
t_{DV}	Data Valid from Read Pulse High	20	-	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z (Note 3)	-	30	ns
t_{WC}	Write Cycle Time	100	-	ns
t_{WPW}	Write Pulse Width (Note 2)	80	-	ns
t_{WR}	Write Recovery Time	20	-	ns
t_{DS}	Data Setup Time	0	-	ns
t_{DH}	Data Hold Time	10	-	ns
t_{RSC}	Reset Cycle Time	100	-	ns
t_{RS}	Reset Pulse Width (Note 2)	80	-	ns
t_{RSR}	Reset Recovery Time	20	-	ns
t_{RTC}	Retransmit Cycle Time	100	-	ns
t_{RT}	Retransmit Pulse Width (Note 2)	80	-	ns
t_{RTR}	Retransmit Recovery Time	20	-	ns
t_{EFL}	Reset to Empty Flag Low	-	100	ns
t_{REF}	Read Low to Empty Flag Low	-	90	ns
t_{RFF}	Read High to Full Flag High	-	70	ns
t_{WEF}	Write High to Empty Flag High	-	70	ns
t_{WFF}	Write Low to Full Flag Low	-	90	ns
t_{EFR}	EF High to Valid Read	10	-	ns
t_{RPI}	Read Protect Indeterminant	-	35	ns
t_{FHW}	FF High to Valid Write	10	-	ns
t_{WPI}	Write Protect Indeterminant	-	35	ns

NOTES:
1. Timings referenced as in A.C. Test Conditions, figure 5.
2. Pulse widths less than minimum values are not allowed.
3. Values guaranteed by design, not currently tested.

Figure 4: AC Characteristics

5

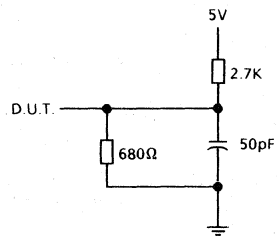
Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 7

Figure 5: AC Test Conditions

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance (Note 1)	$V_{IN} = 0V$	7	pF
C_{OUT}	Output Capacitance (Notes 1 and 2)	$V_{OUT} = 0V$	12	pF

NOTES:
1. Characterized values, not currently tested.
2. With output deselected.

Figure 6: Capacitance



* Includes jig and scope capacitances.

Figure 7: Output Load.

Truth Tables

Operation	Input					Output			Pointer	
	$\overline{R}$	$\overline{W}$	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	$\overline{EF}$	$\overline{FF}$	Data	Read	Write
Reset	1	1	0	x	0	0	1	Z	Zero	Zero
Retransmit*	1	1	1	0	0	1	1	Z	Zero	N/C
Read	1→0	x	1	1	0	1	1	valid	Increment	N/C
Read	x	x	1	1	0	0	1	Z	N/C	N/C
Write	x	1→0	1	1	0	x	1	x	N/C	Increment
Write	x	x	1	1	0	1	0	x	N/C	N/C

* Only available if less than 512 writes since last reset.

Figure 8: Single Device or Width Expansion: Read, Write, Reset and Retransmit

Operation	Input					Output			Pointer	
	$\overline{R}$	$\overline{W}$	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	$\overline{EF}$	$\overline{FF}$	Data	Read	Write
Reset First	1	1	0	0	1	0	1	Z	Zero	Zero
Reset Rest	1	1	0	1	1	0	1	Z	Zero	Zero

NOTES:
1. D_1-D_n are the number of devices in a depth expansion.
2. See Modes of Operation for connections of $\overline{XI}$ and $\overline{XO}$ in depth expansion mode.
3. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. (Fig. 12)

Figure 9: Depth Expansion: Reset and First Load

MA7001

Radiation Hard 512 x 9 Bit FIFO

Signal Descriptions

Reset ($\overline{RS}$)
Reset occurs when $\overline{RS}$ is in a low state, setting both read and write pointers to the first location in memory. Reset is required prior to the first write. Both READ ($\overline{R}$) and WRITE ($\overline{W}$) signals must be in high states during reset.

Read Enable ($\overline{R}$):
Providing the EMPTY FLAG ($\overline{EF}$) is not set, i.e. there is still data to be read, a read cycle commences on the falling edge of R, (see Fig. 16). Data is read in a First-In First-Out manner independent of write operations. When reads are disabled data outputs (Q0 - Q8) are in a high impedance state. Reading the last available memory location sets the EMPTY FLAG ($\overline{EF}$), which is cleared following a write cycle.

Write Enable ($\overline{W}$):
Providing the FULL FLAG ($\overline{FF}$) is not set, i.e. there exists at least one memory location for writing, a write cycle commences on the falling edge of ($\overline{W}$), (see Fig. 17). Data is written into consecutive memory locations independent of read operations on the rising edge of W. Data set up and hold times are with respect to the rising edge of W.

Expansion In ($\overline{XI}$):
There are two possible modes of operation for the FIFO. One with $\overline{XI}$ grounded in which the device is in single-device mode, the other is a depth expension mode or daisy chain configuration. In the latter mode $\overline{XI}$ inputs come from EXPANSION OUT ($\overline{XO}$) outputs of the device preceding it in the chain.

Expansion Out ($\overline{XO}$):
In depth expansion mode $\overline{XO}$ from one device signals the next device in the chain that the last location in its memory has been accessed.

Full Flag ($\overline{FF}$):
$\overline{FF}$ becomes active when the last available memory location has been written to, (see Fig. 18). In general, this occurs whenever the write pointer coincides with the read pointer following a write cycle. Writes are inhibited while $\overline{FF}$ is active, and may only proceed after a read cycle has occured.

$\overline{FF}$ will go high t_{RFF} after completion of a valid READ operation. $\overline{FF}$ will go low t_{WFF} from the beginning of a subsequent WRITE operation, provided that a second READ has not been completed. Writes beginning t_{FFW} after $\overline{FF}$ goes high, are valid. Writes beginning after $\overline{FF}$ goes low and ending more than t_{WPI} before $\overline{FF}$ goes high, are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{FF}$ goes high and less than t_{FFW} later, may or may not occur (be valid) depending on the internal flag status (see figure 19).

Empty Flag ($\overline{EF}$):
Following an initial RESET $\overline{EF}$ is active, becoming inactive after the first write cycle, (see Fig. 20). $\overline{EF}$ becomes active once the read and write pointers are coincident following a read cycle. Reading will not take place whilst $\overline{EF}$ is active, and may only proceed once a write cycle has occured.

$\overline{EF}$ will go high t_{WEF} after completion of a valid WRITE operation. $\overline{EF}$ will again go low t_{REF} from the beginning of a subsequent READ operation, provided that a second WRITE has not been completed. Reads beginning t_{EFR} after $\overline{EF}$ goes high, are valid. Reads begun after $\overline{EF}$ goes low and ending more than t_{RPI} before $\overline{EF}$ goes high, are invalid (ignored). Reads beginning less than t_{RIP} before $\overline{EF}$ goes high and less than t_{EFR} later, may or may not occur (be valid) depending on the internal flag status (see figure 21).

First Load/Retransmit ($\overline{FL}/\overline{RT}$):
This is a dual purpose input depending on the mode of operation of the device. In single device mode $\overline{XI} = 0$ data may be retransmitted, i.e. it may be re-read. In depth expansion mode $\overline{FL}$ signifies the first device in the chain. When $\overline{RT}$ is pulsed low the read pointer is set to the first memory location. The write pointer is unaffected. This feature is disabled in depth expansion mode, and can only be applied when $\overline{R}$ and $\overline{W}$ are inactive (see figure 22).

Data Inputs (D0 - D8):
Data inputs, 9 bit word, for write operations.

Data Outputs (Q0 - Q8):
Data outputs, 9 bit word, for read operations. When $\overline{R}$ is inactive these outputs are in a high impedance state.

5

Modes of Operation

Single Device Mode:
The single device mode is used with $\overline{XI}$ grounded.
(See Fig. 10). In this mode the retransmit facility may be used to re-read the data when less than 512 have been performed between resets.

Width Expansion Mode:
In this mode two or more devices are used, depending on the word length required, with the same control inputs applied to each. The same operations are applied to all devices, thus warning flags $\overline{EF}$ and $\overline{FF}$ are available from any or all of the devices. Output Signals from devices in this mode should not be merged. Fig. 11 illustrates two devices configured in width expansion mode to give an 18 bit word. (512 x 18).

Depth Expansion Mode:
This has applications where more than 512 words are required. The RETRANSMIT facility is not available in this mode.
Two or more devices are organised in a daisy chain. The first device in the chain has $\overline{FL}$ grounded, all others have $\overline{FL}$ in high states. $\overline{XO}$ of each device is connected to $\overline{XI}$ of the next device in the chain.
The same read, write and reset signals are applied to each device. External logic is required to form new empty and full flags, i.e. all $\overline{EF}$'s are ORed together and all $\overline{FF}$'s are ORed together to form new empty and full flags respectively.
Fig. 12 illustrates depth expansion of 2 devices (1024 x 9).

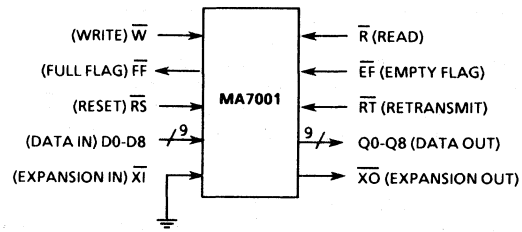


Figure 10: Single Device mode (512 x 9 bits)

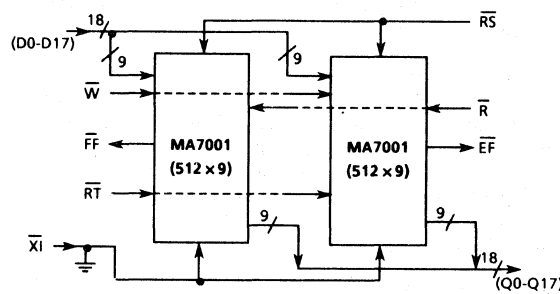


Figure 11: Width Expansion mode (512 x 18 bits)

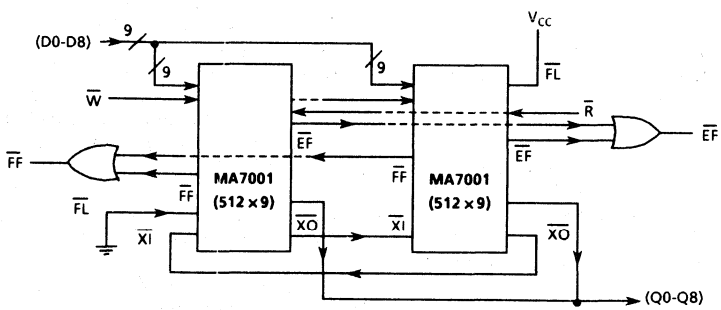


Figure 12: Depth Expansion mode (1024 x 9 bits)

Compound Expansion Mode:
Both width and depth expansion can be implemented into the same expansion block. Note that no control signals are in conflict in either of the two expansion modes, i.e. width or depth expansion modes. Utilising compound expansion large FIFO arrays are possible. Fig. 13 illustrates the use of compound expansion.

Bidirectional Mode:
The FIFO is a unidirectional device, i.e. one system reads, another writes. In cases where full communication is required between two or more systems, two or more groups of devices can be used. These groups can utilise any or all of the expansion modes already mentioned. Fig. 14 illustrates 2 systems connected so that each can transmit data to and recieve data from each other, (see Modes of Operation for connection of control and data signals).

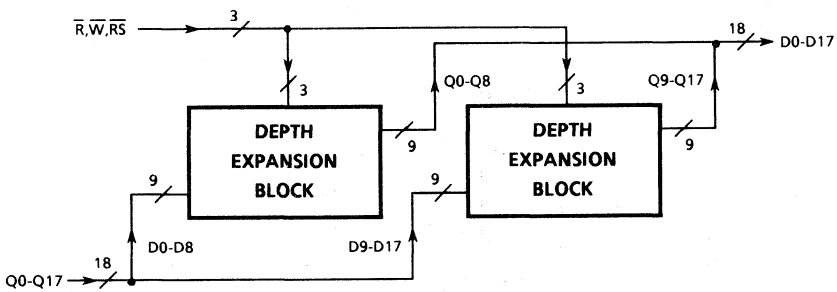


Figure 13: Compound Expansion

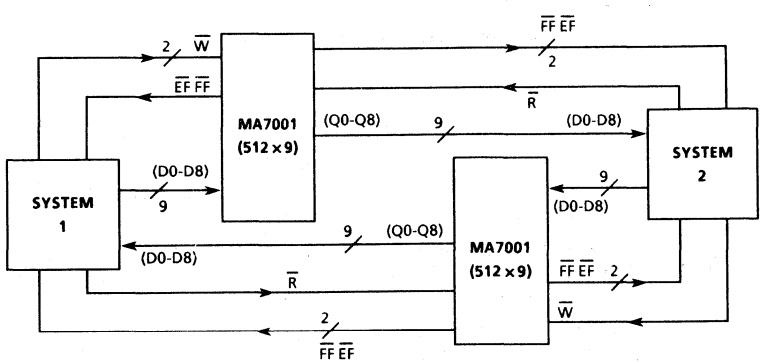


Figure 14: Bidirectional mode (512 x 9 bits each way)

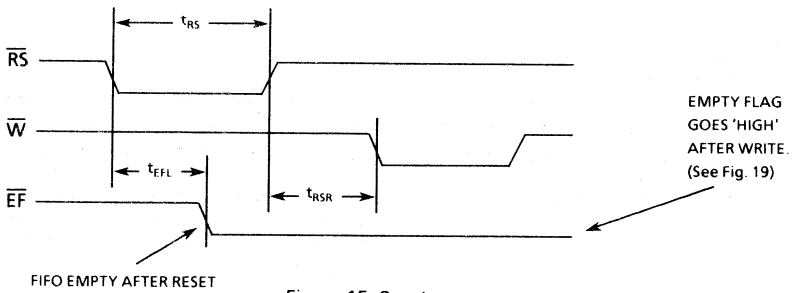


Figure 15: Reset

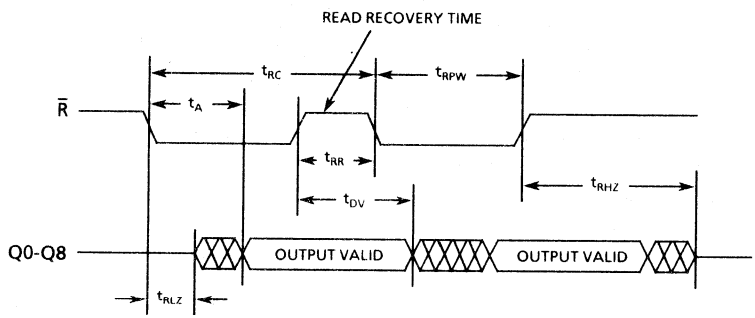


Figure 16: Asynchronous Read

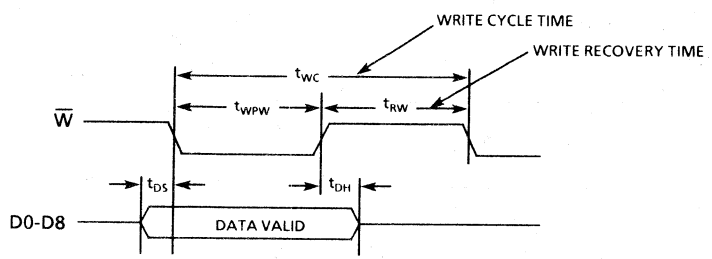


Figure 17: Asynchronous Write

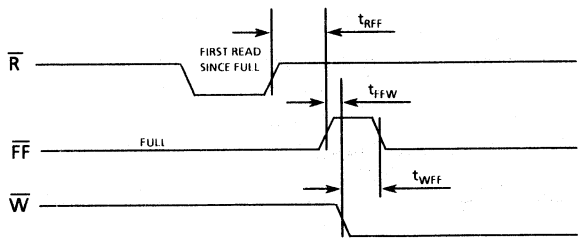


Figure 18: Read/Write to Full Flag

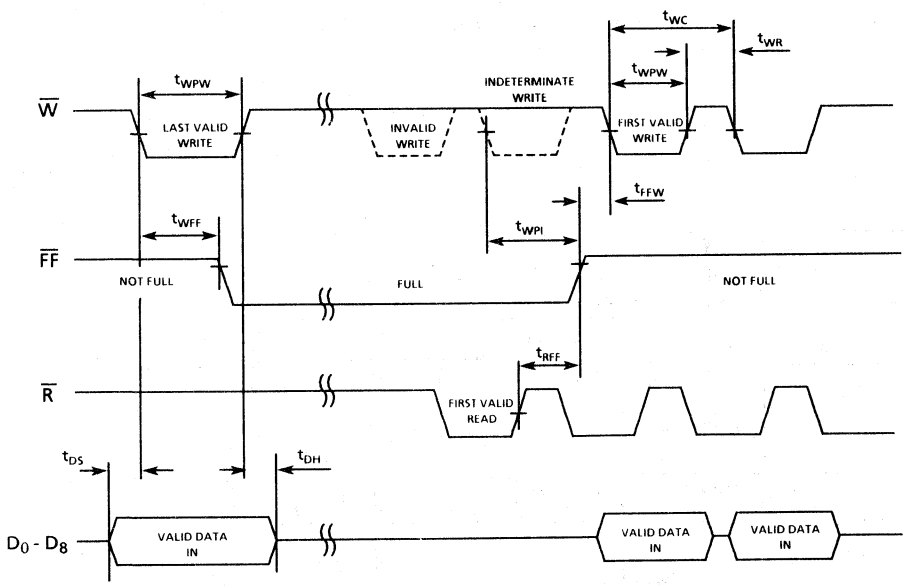


Figure 19: Write and Full Flag

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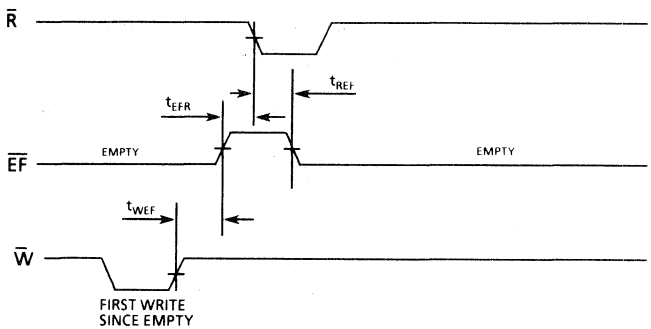


Figure 20: Write/Read to Empty Flag

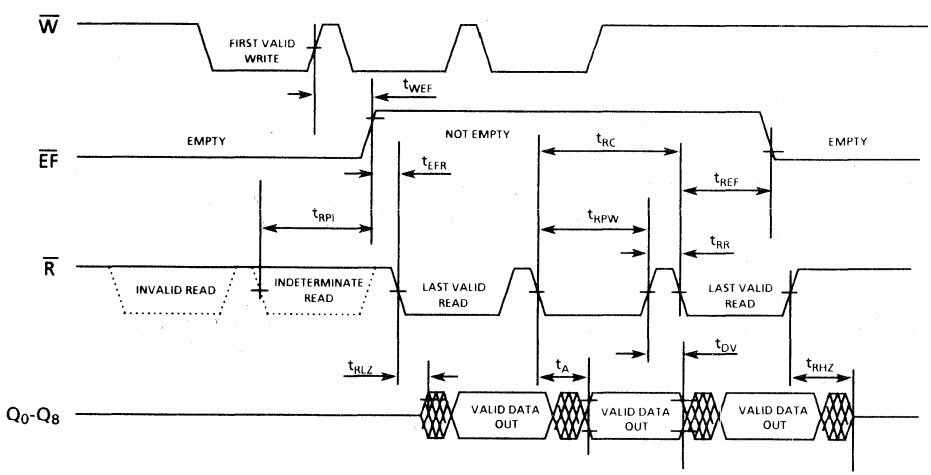
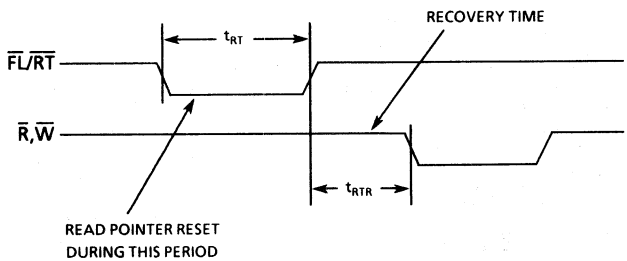


Figure 21: Read and Empty Flag



NOTE: RETRANSMIT AVAILABLE ONLY IN SINGLE DEVICE MODE.

Figure 22: Retransmit Timing

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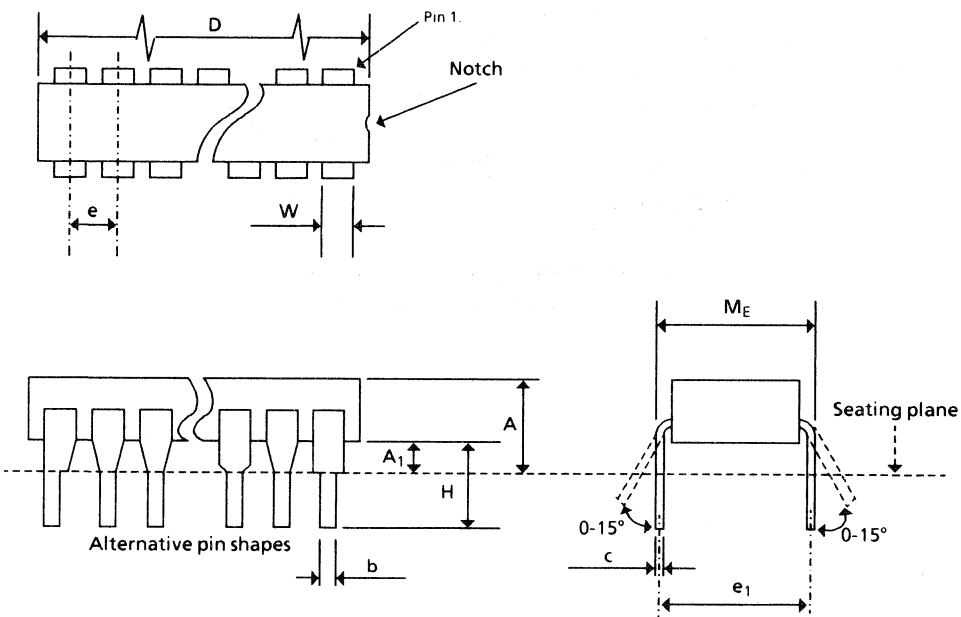
Out lines and Pin Assignments



Ref.	Min.	Nom.	Max.
A	-	-	5.60 (0.220)
A_1	0.38 (0.015)	-	1.53 (0.060)
b	0.35 (0.014)	-	0.59 (0.023)
c	0.20 (0.008)	-	0.36 (0.014)
D	-	-	36.02 (1.418)
e	-	2.54(0.100) typ.	-
e_1	-	15.24(0.600) typ.	-
H	4.71 (0.185)	-	5.38 (0.212)
M_E	-	-	15.90 (0.626)
W	-	-	1.53 (0.060)

Dimensions in mm (inches)

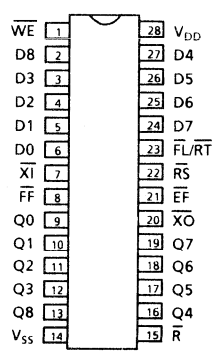
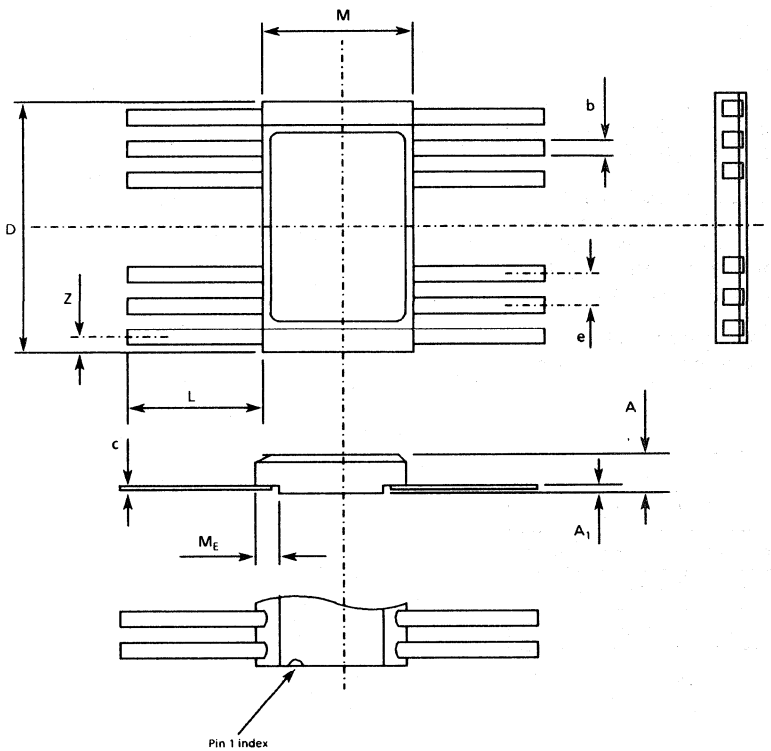


Figure 23: 28-Lead Ceramic DIL (solder seal) - package style C



Ref.	Min.	Nom.	Max.
A			2.36 (0.093)
A_1	(0.013)		(0.017)
b	0.38 (0.015)		0.48 (0.019)
c	0.10 (0.004)		0.18 (0.007)
D	18.08 (0.712)		18.49 (0.728)
e		1.27 (0.050)	
L	7.62 (0.300)		9.91 (0.390)
M	12.50 (0.492)		12.09 (0.508)

Dimensions in mm (inches)

MEDL XG530

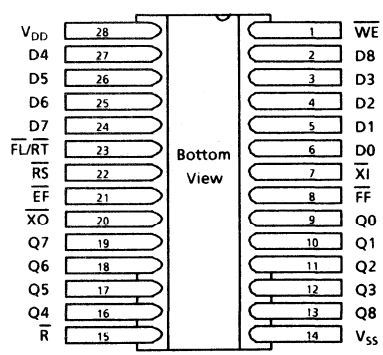


Figure 24: 28-Lead Ceramic Flatpack (solder seal) - package style F

RadiationTolerance

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

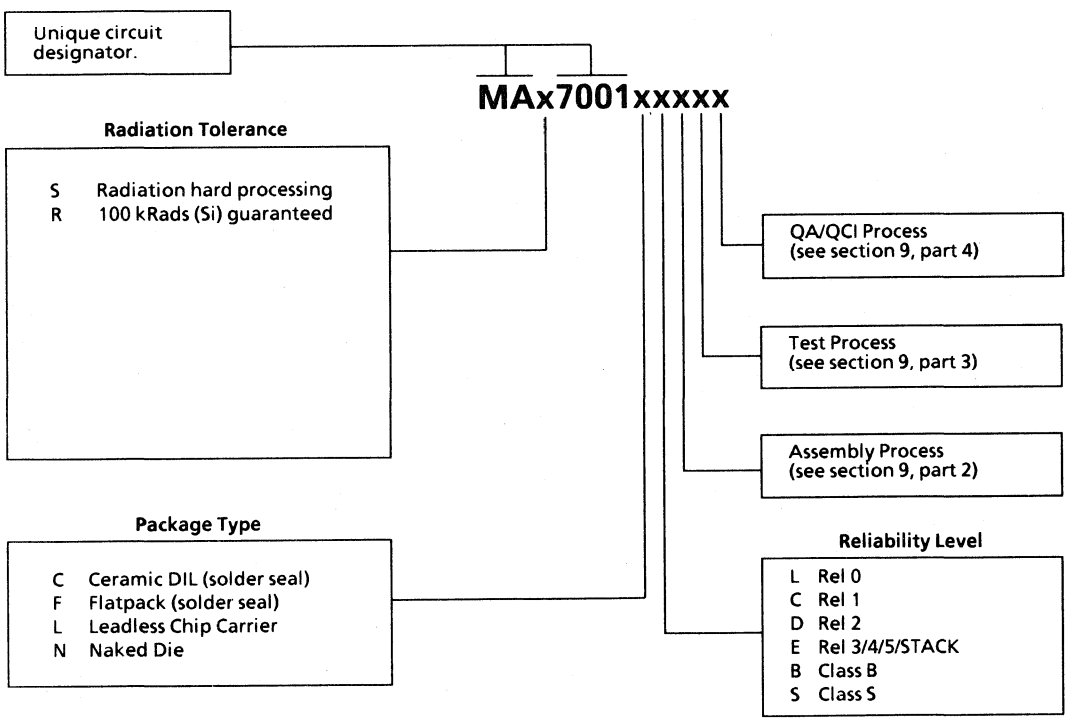
Total Dose (Function to specification)	1.0×10^5 Rad(Si)
Transient Upset (survivability)	5×10^{10} Rad(Si)/sec
Neutron Hardness (Function to specification)	$>10^{15}$ Neutrons/cm^2
Single Event Upset (GSO 10% worst case)	10^{-10} errors/bitday
Latch-up	Not possible

Figure 25: Radiation Hardness Parameters

MA7001
Radiation Hard 512 x 9 Bit FIFO

Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



section 6
DATA BUS

GEC PLESSEY

SEMICONDUCTORS

S10401FDS Issue 1.6 December 1990

MA3690/1

Radiation Hard 1553B Bus Controller/ Remote Terminal

Features

- **Radiation Hard to 1MRads (Si)**
- **High SEU immunity, latch-up free**
- **CMOS-SOS Technology**
- **All inputs & outputs fully TTL or CMOS compatible**
- **Military temperature range -55 to + 125°C**
- **Dual bus capability**
- **Minimal subsystem interface**
- **Powerful bus control facility**
- **Complete remote terminal protocol**
- **SEAFAC approved**

General Description

The MA3690/1 chip set has three modes of operation: remote terminal, bus controller, and passive monitor. It has a dual bus capability, requires minimum support hardware / software and is implemented on a radiation hard, CMOS/SOS process. For applications requiring access to Terminal Flag, an MA3693 is available as an alternative to the MA3690 in a 48-Pin DIL.

As a remote terminal, the MA3690/1 is fully compatible with Mil Std 1553B. The chip set obtained SEAFAC approval in December 1987. All options and mode commands specified by the Mil Std are implemented. Full and meaningful use is made of status word bits and a comprehensive bit word is provided.

A unique mechanism has been incorporated that allows the subsystem to declare illegal commands legal, and vice versa, before the chip set services the command.

It should be noted that use of this mechanism is optional and that the system defaults to normal operation if the option is not required. The chip set is easily interfaced to subsystem memory and is sufficiently flexible to ensure compatibility with a wide range of microprocessors.

As a bus controller the MA3690/1 has the ability to initiate all types of 1553B transfer on either of the two buses. An instruction word is set up by the subsystem, prior to transmission, which contains details of transfer type and bus selection. Four bits of the instruction word have been used to specify the conditions under which the chip set will generate a subsystem interrupt. The most significant bits of the instruction word have been used to specify the conditions under which the chip set will perform an automatic retry and the number of retries to be carried out (max. 3). At the end of each instruction execution cycle, the chip set writes a report word into the subsystem memory; the contents of which give the subsystem an indication of the degree of success of the transfer.

The bus controller may be used in either of two configurations, i.e. single shot or table driven.

In the single shot configuration, the controller is under direct control from the subsystem (processor). In table driven configuration, the controller is given greater autonomy to execute a table of instructions held in either ROM or RAM.

As a passive monitor, the chip set will monitor all bus activity and pass any associated information to the subsystem. As the name implies, in this mode of operation, the chip set is truly passive and will not reply to command instructions.

Signal Descriptions

All signals are TTL compatible unless stated otherwise. An 'N' at the end of the signal name denotes an active low signal.

Supplies

VDD 5 volts positive supply
VSS Ground

Clock inputs

CK12 12MHz clock

Bus Interface Lines

PDIN0 Positive threshold exceeded on bus 0

NDIN0 Negative threshold exceeded on bus 0

TXEN0N Transmit enable for driver on bus 0

PDOUT0N Positive Manchester data for driver on bus 0
NDOUT0N Negative Manchester data for driver on bus 0
PDIN1 Positive threshold exceeded on bus 1

NDIN1 Negative threshold exceeded on bus 1

TXEN1N Transmit enable for driver on bus 1

PDOUT1N Positive Manchester data for driver on bus 1
NDOUT1N Negative Manchester data for driver on bus 1

Subsystem Interface Lines

STROBEN Output
STROBE - Information transfer strobe pulse for words being transferred on the data highway.

BUFENN Output
BUFFER ENABLE - This line goes low to enable the data highway buffer between the terminal and the subsystem.

R/WN Output
READ/WRITE - This line indicates the direction of information transfer between the terminal and the subsystem. When low, information is being written from the terminal to the subsystem.

DTRQN Output
DATA TRANSFER REQUEST - This line goes low to request permission to transfer a non mode data word to or from the subsystem.

DTAKN Input
DATA TRANSFER ACKNOWLEDGE - This line should be driven low to grant permission to perform the requested data word transfer.

MDTN Output
MODE DATA TRANSFER -
RT: This line goes low to indicate that the data word being transferred is assosiated with a mode command.
BC: When operating as a passive monitor this line goes low to indicate that a valid data word is on the data highway and should be written into the received data latch.

GBRN Output
GOOD BLOCK RECEIVED - When in RT mode this line will pulse low to inform the subsystem that the received non mode data words are valid and may be used.

ADENN Output
ADDRESS ENABLE - When in RT mode this line will go low as part of the reset routine to enable the terminal address on to the data highway.

SYNCN Output
SYNCHRONISE - This line will pulse low if a valid synchronise mode command without data is received and passes all validity checks.

STATENN Output
STATUS ENABLE -
RT: When low this line enables the contents of the subsystem status latch on to the data highway.
BC: When low this line enables the BC report word on to the data highway.

MDRN Output
MODE DATA RECEIVED - This line will pulse low to inform the subsystem that the received mode data is valid and may be used.

RXCMDN Output
RECEIVED COMMAND -
RT: This line goes low to indicate that a valid command word for this RT is on the highway and should be written into the command word latch.

BC: When operating as a passive monitor this line goes low to indicate that a valid command / status word is on the data highway and should be written into the received status latch.

BUSYREQN / HALTREQN Input
BUSY REQUEST / HALT REQUEST -
RT: This line should be driven low as a request for the terminal to set the busy bit and inhibit non mode data transfers to or from the subsystem.
BC: This line should be driven low as a request for the terminal to halt table execution and all subsystem access.

BUSYACKN / HALTEDN Output
BUSY ACKNOWLEDGE / HALTED -
RT: This line will go low to indicate that the subsystem has free access to the shared store.
BC: This line will go low to indicate that all terminal operation has been halted and hence the subsystem has free access to the shared store.

CODENN Output
CODE ENABLE - This line when low indicates that a word transfer between the terminal and either the Instruction Store or the Report Store is taking place.

C0 Output
CODE 0 - This line is the least significant address line from the terminal to the Instruction and Report Stores.

C1 Output
CODE 1 - This line is the least significant but one address line from the terminal to the Instruction and Report Stores.

INCADRN Output
INCREMENT ADDRESS - This line pulses low to increment the external instruction addressing counter.

HSFN/IRQN Output
HANDSHAKE FAIL -
RT: This line pulses low to inform the subsystem that it has not responded to a data transfer request to take place.

INTERRUPT REQUEST -
BC: This line pulses low to generate an interrupt to the BC subsystem processor.

INCMDN Output
IN COMMAND - When low this line indicates that the terminal is currently servicing a command word.

EOTN Output
END OF TRANSMISSION - When low this line indicates that the selected bus is quiet and hence available for use.

ABORTN Output (CMOS)
This line will pulse low to abort execution of the current command if an error is detected.

B0-B15 Input / Output
HIGHWAY LINES - 16 line bidirectional Output data highway. (B0 = LSB).

CLDN Output (CMOS)
COMMAND LOAD - When low this line indicates that the word on the data highway should be loaded into the transmitter for transmission with a command sync.

DLDN Output (CMOS)
DATA LOAD - When low this line indicates that the word on the data highway should be loaded into the transmitter for transmission with a data sync.

OBFN Output (CMOS)
OUTPUT BUFFER FULL - When low this line indicates that the transmitter output buffer is full and cannot be overwritten.

VALDRN Output (CMOS)
VALID DATA RECEIVED - When low this line indicates that a valid data word has been received and is on the data highway.

VALCRN Output (CMOS)
VALID COMMAND RECEIVED -
RT: When low this line indicates that a valid command word for this RT has been received.
BC: When low this line indicates that a valid word with a command sync has been received.

RT/BCN Input
REMOTE TERMINAL/BUS CONTROLLER - When high the terminal will function as an RT.When low the terminal will function as a bus controller.

CK4 Output
4MHz system clock.

PUCN Input
POWER UP CLEAR - This line should be pulsed low following power-up.

RESETN Input / Output
RESET - This line when low, forces the internal circuitry to reset to the quiescent initialised state. This is a 'TTL' level input on both devices and an open-drain output on the MA3690. The subsystem should drive this line via an open drain/collector device with external pull up fitted.

RT0 / RT1 See Note 2 Inputs
REPLY TIMEOUT DECODE - These lines on the MA3690 allow four different timeout values to be used.

RT1	RT0	Timeout (us)
0	0	16
0	1	22
1	0	44
1	1	108

Note: Under normal operation, option 00 should be used, (i.e 16uS)

The measurement is taken between mid parity and mid sync - measured at PDIN/NDIN terminals.

Note 1: TEST and SOT are used for test purposes only and for normal chip set operationboth lines should be tied low.

Note 2: The MA3693 may be specified as an alternative to the MA3690. On the MA3693 RT1 input is pulled low internally and replaced with terminal flag (TFN) output. This signal can be inhibited by the mode code Inhibit Terminal Flag. This is an active LOW signal.

Operation in Bus Control Mode

For this mode of operation the RT/BC pin must be held in the logic zero state. On power up the PUC or RESET line must be pulsed low for a minimum of 500ns causing the chip set to initialise and assume the halted state with the HALTED output low. To release the terminal from the halted state, the subsystem must drive the HALTREQ line through a low to high transition, at which time the HALTED line will go inactive.
When the HALTED line goes inactive,the terminal will address a four word deep Instruction Store as shown below, using the C0 and C1 outputs.

Instruction Store

C1	C0	Word
0	0	Instruction
0	1	Receive Command
1	0	Transmit Command
1	1	Data Pointer

The instruction word specifies the operation which the terminal is to carry out, and is formatted in the following way:

Instruction word

Bit 15.14.	13.12.11.	10.9.8.7.	6.5	4.3.	2.1.0.
Retry Count	Retry Condition	Interrupt Condition	Bus Select	Function Code	Message Code

The significance of the instruction word bits are as follows:

Message Code

Code	Transfer Type
000	RT to BC
001	BC to RT
010	RT to RT, data to BC subsystem
011	RT to RT, no data to BC subsystem
100	Broadcast RT to BC, non data mode commands only
101	Broadcast BC to RT
110	Broadcast RT to RT, data to BC subsystem
111	Broadcast RT to RT, no data to BC subsystem

Function Code

Code	Terminal Function
00	Execute message code
01	Perform self test
10	Monitor bus
11	No operation

Bus Select

Code	Definition
00	Transmit on bus 0
01	Transmit on bus 1

Note: Bit 6 of the instruction word is tied low internally.

Interrupt Condition

Code	Definition
0001	Interrupt if no response
0010	Interrupt if status bit set
0100	Interrupt always
1000	Interrupt if word error

If the terminal detects one of the above conditions and the appropriate flag is set, the the IRQ line will pulse low for 250ns.

Retry Condition

Code	Definition
001	Retry if error
010	Retry if status bit set
100	Retry if busy set

Function Code

The Function Code (bits 4 and 3 of the Instruction Word) specifies the required terminal mode of operation.

Execute - Code 00

With the Function code bits set to 00, the terminal will execute the message as defined in the Message code bits.

Self Test - Code 01

If the terminal has been selected to perform a Self Test then the terminal transmitter output stages will be disabled and the self test sequence entered. At the end of the Self Test the transmitter stages will be re-enabled and a Report sequence will be activated, in order to report on the success, or failure, of the Self Test.

Passive Monitor - Code 10

If the Function code of the Instruction word is 10 the terminal will disable the transmitter output stages, suspend table execution and merely monitor the specified bus for valid words.

No Operation - Code 11

The No Operation code provides a means of introducing delay or a wait sequence into the table operation. In selecting this code the terminal will be forced into the Report sequence and provide either an increment signal (INCADRN) or an interrupt (IRQN) if the Interrupt Always flag in the Instruction word has been selected.

Bus Select

The required data bus on which transactions take place is defined by bit 5. In addition to this, this bit defines the bus on which the Transmitter Self Test operation will be conducted and the choice of the bus for monitor purposes in Passive Monitor mode.

Interrupt Request

Four bits of the Instruction word (bits 10-7) define conditions under which the terminal will generate an interrupt to the subsystem (IRQN). Note that the generation of IRQN will only take place after any selected retry conditions have been exhausted.

The interrupt conditions which may be selected can be categorised as follows.

1. Interrupt if no response - the terminal will generate an interrupt if the RT does not respond.
2. Interrupt if Status bit set - the terminal will generate an interrupt if a received status word has a bit set other than in the RT address field or if the wrong RT responds.
3. Interrupt Always - the terminal will generate an interrupt regardless of whether the message was successful or not.
4. Interrupt if word error - the terminal will generate an interrupt if a word encoding or word count error occurs.

In all of the above cases, the terminal will generate a 250ns pulse on IRQN and enter the halted state. This will occur after the Report sequence has been executed.

Note the INCADRN will not be produced.

Retry Request

Three bits of the Instruction word (bits 13-11) are used as flags to specify conditions under which the terminal will execute automatic message retries until the retry number count is zero. The retry flags are involved with the following conditions:

1. Retry if error - this includes a no-status response, a word encoding error, or a wrong word count from a responding RT.
2. Retry if Status bit set - an automatic retry will take place if a received status word has a bit set, other than in the RT address field, or if the wrong RT responds.
3. Retry if Busy - this is a specific check for the setting of the Busy bit in a responding RT's status word.

The remaining two bits of the Instruction word specify the number of message retries which the Bus Controller will attempt automatically. A code of 00 specifies no retries, a code of 11 specifies the maximum of three retries. The retries are in addition to the initial message transmitted, hence a message may be transmitted four times in total, if not successful. Note that if the condition which is being tested becomes invalid, the retry sequence will discontinue on the next message with the Bus Controller completing execution of the message in the relevant manner.

Bit 6 of the Instruction word is permanently tied low.

Retry Count

The two most significant bits of the instruction word specify the number of retries to be carried out when a retry condition has been detected. (Maximun 3 given by code 11)

Receive Command Word

The receive command word is addressed when CODENN and C1 are both low and R/WN and C0 are both high. This word is the command word which will be transmitted for a BC to RT transfer or as the first command word of an RT to RT transfer.

Note: This word should be set to 1111 HEX if the message code is 000 or 100, or if the Function Code is not 00.

Transmit Command Word

The transmit command word is addressed when CODENN and C0 are both low and R/WN and C1 are both high. This word is the command word which will be transmitted for an RT to BC transfer or as the first command word of an RT to RT transfer.

Note: This word should be set to 1111 HEX if the message code is 001 or 101, or if the Function Code is not 00.

Data Pointer Word

The data pointer word is addressed when CODENN is low and C0, C1 and R/WN are all high. This word is intended as a base address pointer to the subsystem data store thus specifying where any data words associated with the current instruction should be stored or retrieved from. As such, this word is not read into the terminal itself but is merely transferred from the Instruction Store to a suitable external address latch. (The BUFENN signal is therefore inactive during this transfer).

Report Store

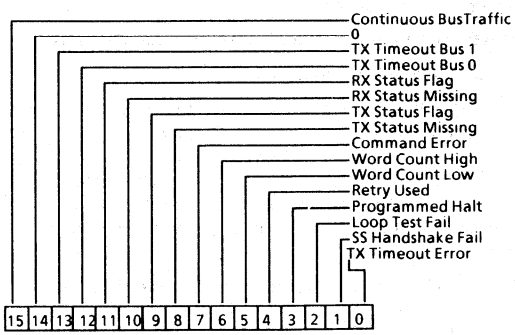
The report store holds information concerning the success or failure of the execution of the last instruction, and is addressed by means of the CODENN, C0 and C1 lines as for the instruction store. The report store is addressed when the R/WN line is low, the instruction store when the R/WN line is high.

The report store comprises a Report word, a receive status word (if applicable) and a transmit status word (if applicable). The fourth location has no meaning and is not at anytime addressed.

C1	C0	Word
0	0	Report word
0	1	RX status word
1	0	TX status word
1	1	Not used

Report Word

The report word gives the subsystem information as to the type of error associated with the last transfer (the word will be clear if no error occurred).
The report word is formatted as follows :



Receive Status Word

The receive status word location is addressed when CODENN, C1 and R/WN are low and C0 is high. This location is used by the terminal to store the status word, if any, received from a receiving RT. In self test mode this location is updated with the contents of the receive command word during the instruction fetch cycle.

Transmit Status Word

The transmit status word location is addressed when CODENN, C0 and R/WN are low and C1 is high. This location is used by the terminal to store the status word, if any, received from a transmitting RT. In self test mode this location is updated with the contents of the transmit command word during the instruction fetch cycle.

Report Word

The Report word is written at the end of message execution, after all retries have been exhausted and prior to the IRQN line being set active. This word indicates the health of the terminal as well as information relating to the message execution.

Transmitter Timeout Error

This bit will be set if a transmitter timeout error occurs while the terminal is transmittting or if a self test on the transmitter timeout mechanism fails. This will come into effect 800us after the commencement of the Self Test. The setting of this bit will also cause a subsystem interrupt to be generated.

This bit will be reset to logic zero if the terminal is reset.

Subsystem Handshake Failure

This bit will be set if the subsystem fails to acknowledge a terminal request to transfer a data word in 0.75us for a received data word or 13.5us for a transmit data word. If this condition takes place while the terminal is transmitting the transmission will be aborted. The setting of this bit will also cause a subsystem interrupt to be generated..

This bit will be reset to logic zero if the terminal is reset.

Loop Test Failure

This bit will be set if the receiver circuitry detects an absence of terminal transmission or a waveform encoding error occurs while the terminal is transmitting. The seting of this bit while the terminal is transmitting will cause the transmission to be aborted and a subsystem interrupt to be generated.

This bit will be reset to logic zero if the terminal is reset.

Programmed Halt

This bit will be set if the Interrupt Always flag of the Instruction word has been selected.

This bit will be reset at the start of each new instruction execution cycle.

Retry Used

This bit will be set if one or more message retries has been attempted.

This bit will be reset at the start of each new instruction execution cycle.

Word Count Low

This bit will be set if the terminal detects fewer valid data words than specified by the Transmit Command word of the Instruction set.

This bit will be set low at the start of each instruction execution cycle or message retry.

Word County High

This bit will be set if the terminal detects more valid data words than specified by the Transmit Command word of the Instruction set.

This bit will be set low at the start of each instruction execution cycle or message retry.

Command Error

This bit will be set if an error occurs in the Instruction set. The setting of this bit will cause instruction execution to be aborted and a subsystem interrupt to be generated.

This bit will be reset at the start of each new instruction execution cycle.

TX Status Missing

This bit will be set if a no-response is detected from an RT which has been commanded to transmit and the relevant RT address was not the Broadcast address.

This bit will be reset at the start of each new instruction cycle or message retry.

TX Status Flag

This big will be set if the status word received from a transmitting RT has a bit set or has the wrong terminal address.

This bit will be reset at the start of each new instruction execution cycle or message retry.

RX Status Missing

This bit will be set if a no-response is detected from an RT which has been commanded to receive and the relevant RT address was not the Broadcast address.

This bit will be reset at the start of each new instruction cycle or message retry.

RX Status Flag

This bit will be set if the status word received from a receiving RT has a bit set or has the wrong terminal address.

This bit will be reset at the start of each new instruction execution cycle or message retry.

Transmitter Timeout On Bus 0

This bit will be set if the transmitter timeout mechanism operates on Bus 0. This will be set under Selt Test execution with Bus 0 selected in the Instruction word.

This bit will be reset to logic zero if the terminal is reset.

Transmitter Timeout On Bus 1

This bit will be set if the transmitter timeout mechanism operates on Bus 1. This will be set under Selt Test execution with Bus 1 selected in the Instruction word.

This big will be reset to logic zero if the terminal is reset.

Continuous Bus Traffic.

This bit will be set if the terminal detected that the data bus is already active when the BC is instructed to execute a message on that a data bus. An active data bus is defined as a data stream of one command word or status word and greater than 32 continguous data words being received by the terminal. The setting of this bit will cause transmission to be suppressed and a subsystem interrupt to be generated.

It should be noted that:

1. This condiction is only likely to be caused by a runaway RT which transmits continuously.
2. If this condition is present the subsystem is able to specify the use of the alternative bus for its transmissions.

This bit will be reset to logic zero when the terminal is reset or when the terminal detected a quiet bus.

Modes of Operation

The Bus Controller may be controlled in either a single shot mode or ina table driven mode. In the former, the execution of the message table would be under direct control of the subsystem, on a message by message basis.

The table driven mode would provide a subsystem capable of more autonomous operation, leading to a greatly reduced level of processor intervention in the message execution level, at least. In either case the procedure of Instruction fetch, message execute and reporting would be the same. The difference arises from the value of the HALTREQN line when it is re-sampled at the end of message execution. This is further described below.

Single Shot Operation

To commence a message execution the subsystem must take the HALTREQN line low to high for a minimum of 1us. This will be followed by the terminal acknowledging this action by the HALTEDN line being set inactive (high). The HALTEDN line will remain high until the message has been completed, at which time the HALTREQN line is further sampled. If it is low then the terminal will halt and wait until the request line is taken high again, in effect a single instruction execution.

It is important to the integrity of the system that the HALTREQN line is strictly glitch free, otherwise problems will arise with the terminal attempting to execute commands at a time when no terminal access to the variou s stores can be guaranteed.

Continuous Operation

The continuous message table operation mode can be achieved by ensuring that the end of a message the HALTREQN line is high. Thus, assuming that the message has executed correctly, the terminal will generate a signal to increment the external address counter (INCADRN) and continue to the next instruction. If, however there has been an interrupt generated (IRQN active) the terminal will halt in the HALTEDN state until specifically requested to continue. Note that no address increment will take place. To continue execution the HALTREQN line should be taken low to high for the appropriate time.

Continuous table driven operation results in an intermessage gap of 20us.

Passive Monitor

The terminal may be configured into a Passive Monitor (or Bus Monitor) merely by selecting the appropriate Function Code of the Instruction word. By doing this the terminal will not take part in any further Instruction execution but instead will monitor the selected bus for data transmissions.

Interrupt/Retry Capability

The terminal has certain in-built functions which permit the terminal to retrieve situations which would normally cause a greater degree of subsystem intervention. This is achieved by having an automatic retry facility in-built to the terminal which is selectable from the Instruction word. In this case both the condition and number of attempts for which the terminal must try may be specified. After completion of the required number of attempts, terminal operation may be halted with the possibility of aninterrupt generated also.

The interrupt facility provides a means of more direct subsystem interaction in the event of a failure. Similar flags are required to be set in the Instruction word before a selectable interrupt may be generated. This form of interrupt also includes an Interrupt Always flag whose application may be used to determine subsystem/system timing requirements.

It should be noted that an interrupt may also be generated by the error checking procedures of the terminal which verify aspects of the Instruction word and associated Receive/Transmit command words.

Standby Bus Controller

The terminal provides a number of signals to the subsystem for message addressing and execution. Two address lines are provided (C0, C1) plus a signal to increment an external counter (INCADRN). This, together with the on-chip sequencing, error checking, etc., enables a standby bus controller, using a fixed table of messages, to be realised in few devices as shown in Figure 3. It is therefore possible to attain a standby BC on a single 6 x 4 PCB card.

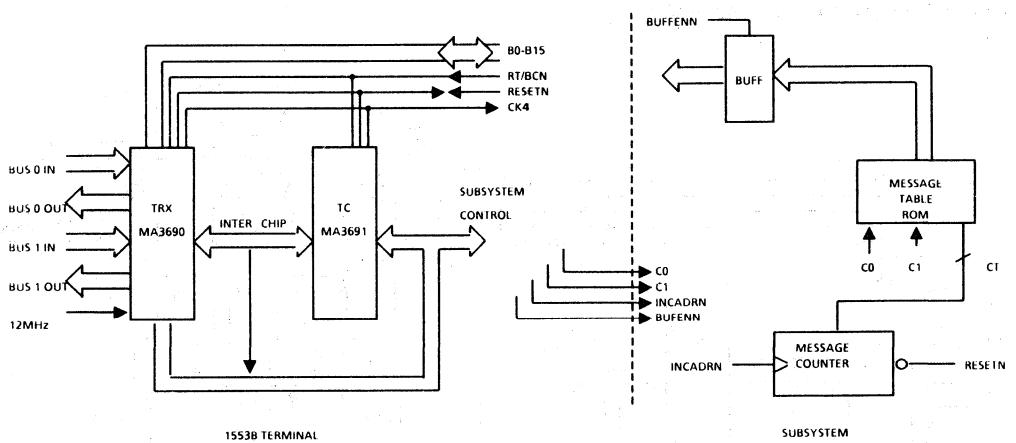


Figure 3: Standby Bus Controller

6

Full Bus Controller

To make use of the SOS chipset's capabilities a processor-based system would be more applicable. A block diagram of such a system, using shared store technique is shown in Figure 4. In this, the instruction word store would be alterable by the processor for use in various system conditions, i.e. a basic message table would initialy be set up with the processor monitoring the results of execution from the report word store and / or the interrupt request (IRQN) line. On detection of an erroneous condition, the processor could write a new message table to test the RT in error by, for example, a self test mode command. The inclusion of automatic retry, with a maximum of 3 retries, in the instruction word, removes the requirement from the processor to retry under simple RT faults, e.g., status bit set.

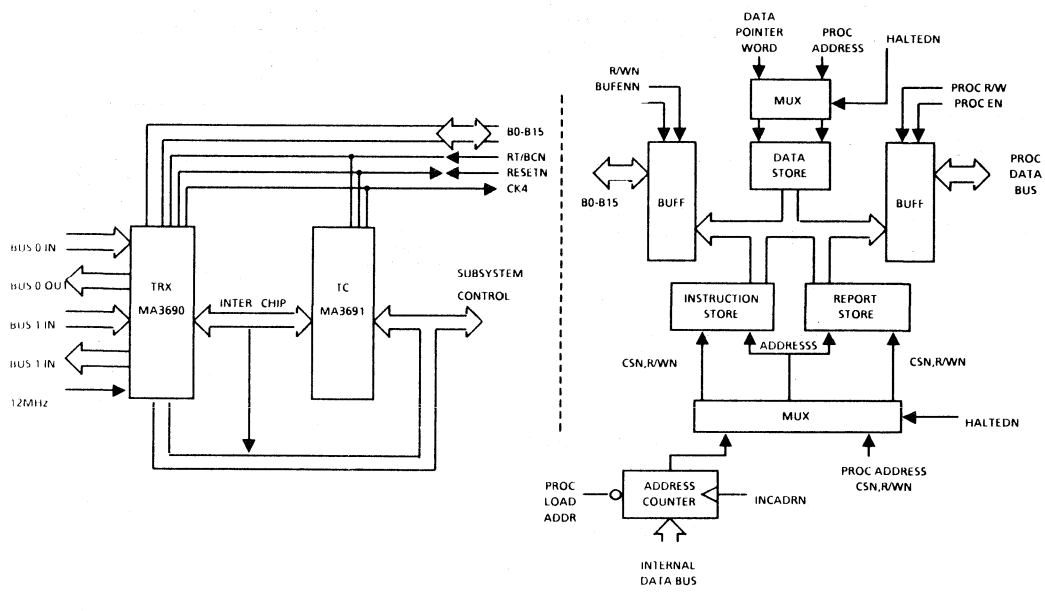


Figure 4: Full Bus Controller

Subsystem Interface

The terminal / subsystem interface consists of a 16 bit bi-directional data highway and a number of control lines, many of which are of optional use. The subsystem lines have been arranged such as to allow a simple shared store technique to be readily implemented but sufficient flexibility has been designed to allow optimisation of the interface for a particular subsystem design.

Remote Terminal Mode

On initialisation, the RT address, address parity and broadcast enables are loaded from latches contained within the subsystem via the data highway. The subsystem status bits are also loaded in a similar manner when required.

This terminal uses two distinct methods for dealing with non mode data and mode data. In the first, a busy request / acknowledge handshake is used to ensure no data transfer takes place when the subsystem is busy thus ensuring no addressing / data conflict of the main data store. Mode data, however, may be transferred even if the subsystem has declared itself busy. This represents a departure from previous chipset philosophy.

The validation of a data transfer also depends on data type. For non mode data, a data transfer request / acknowledge handshake is used to transfer each data word to or from the subsystem (both RT and BC) with a good block received (GBRN) denoting a correct transfer. For mode data, a mode data transfer (MDTN) is used to signal a mode data word with correct transfer being denoted by mode data received (MDRN). Thus, dependant on application, the I/O signals may be significantly reduced.

An RT subsystem interface signal transfer is shown in Figure 5.

Bus Controller Mode

For data transfers generally, 750ns enable signals (BUFENN,R/WN etc.) are produced by the terminal with a 250ns strobe signal upon which the data will be valid.

The bus controller terminal provides signals to fetch the message and write out a report and any associated data. The HALTREQN and HALTEDN handshake lines operate in a similar fasion to the BUSYREQN / BUSYACKN RT lines in that if HALTREQN is taken low the terminal will complete the current instruction and then halt, taking HALTEDN low to indicate that it has done so.

A BC subsystem may be operated in either a single shot or table driven mode. In either case, the two least significant address lines (C0,C1) to the instruction and report word stores are provided by the terminal. On taking HALTREQN high (for a minimum of 1us) the subsystem initiates an instruction fetch cycle which consists of the terminal reading the instruction word, receive command word and transmit command word from the instruction store and transferring the data pointer word from the instruction store to an external data address latch. Further operation is dependent on the instruction word.

On executing a message sequence the terminal will write out the report word and either:

(a) Increment the instruction address and proceed to the next instruction,

(b) Increment the instruction address and halt,

(c) Do not increment the instruction address, interrupt subsystem and halt.

Any data associated with the command will be transferred to or from the data store in a similar manner as used by the RT.

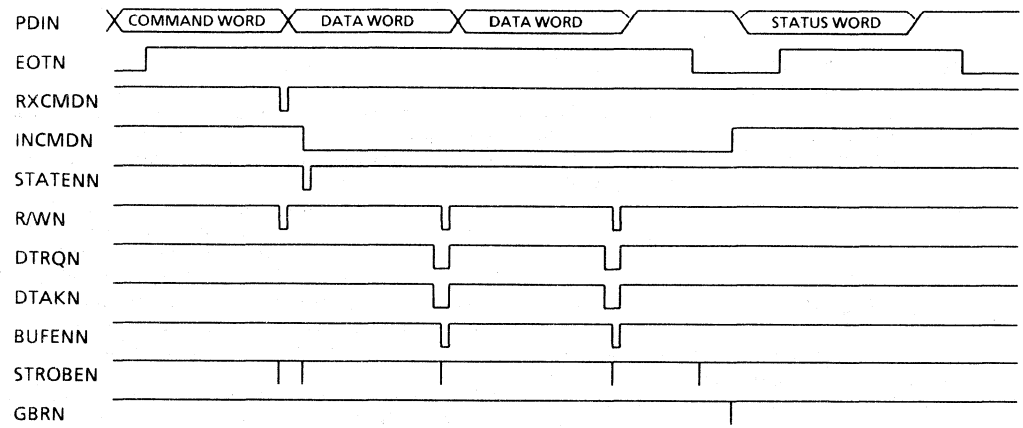


Figure 5: Remote Terminal subsystem interface signal transfer

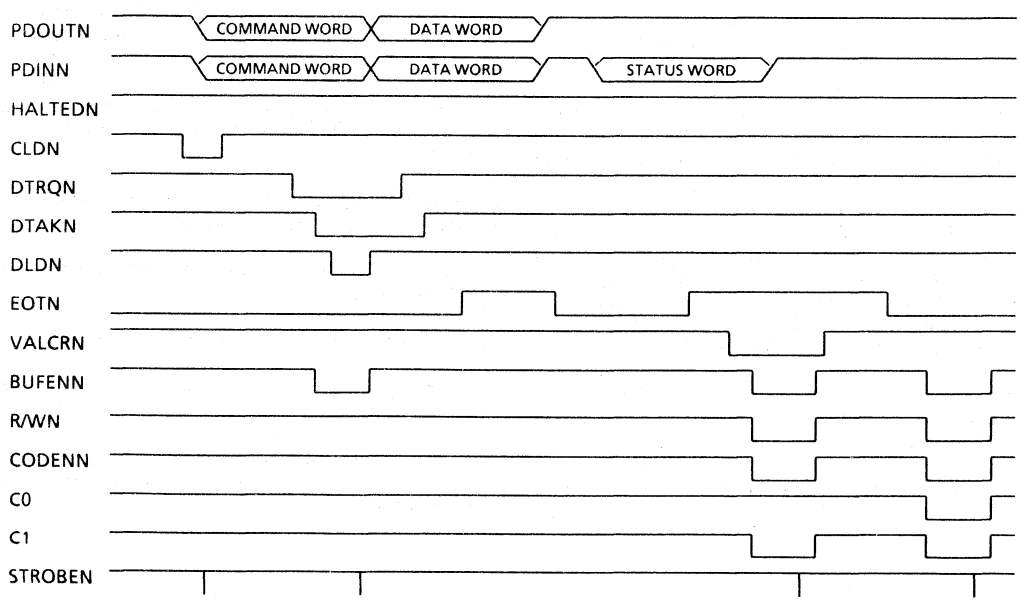


Figure 6: Bus Controller subsystem interface signal transfer

Chip Set Interconnection Diagram

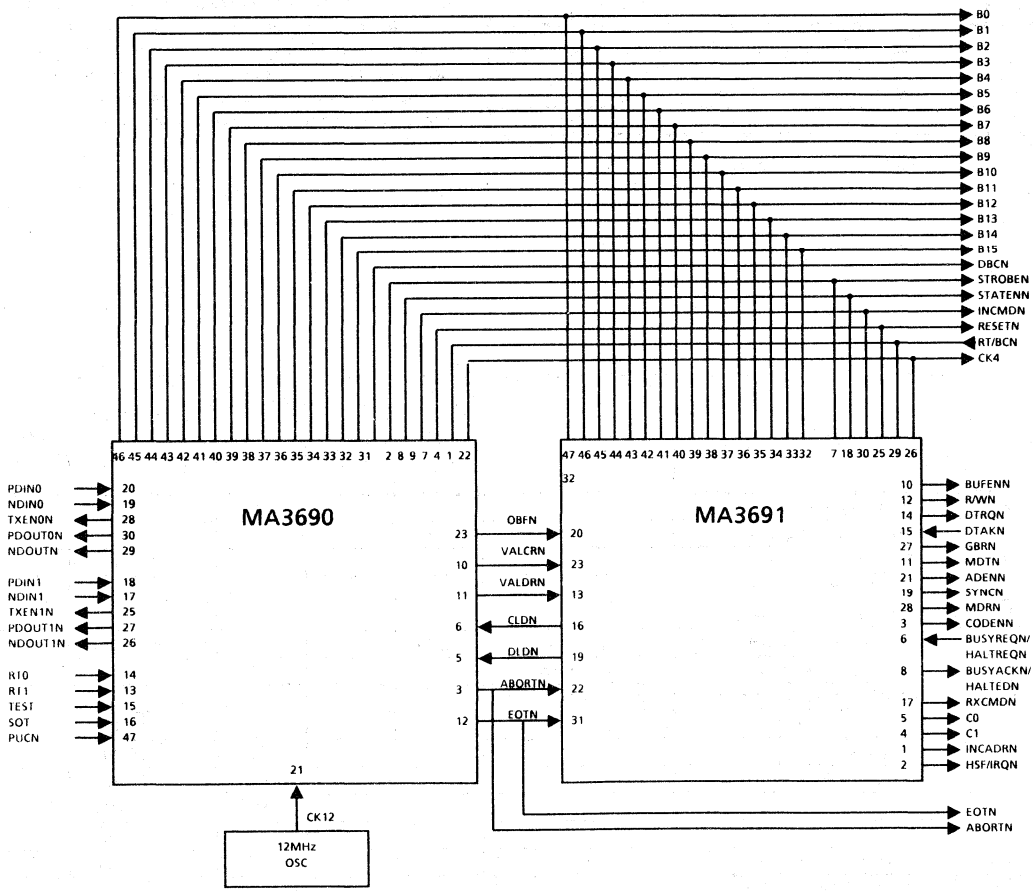


Figure 7: Chip Set Interconnection Diagram

DC Characteristics and Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0.5	7	V
V_I	Input voltage	-0.3	V_{DD} + 0.3	V
T_A	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Figure 8: Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Conditions	Total dose radiation not exceeding $3x10^5$ Rad (Si)			Total dose ≤1 MRad (Si)		Units
			Min.	Typ.	Max.	Min.	Max.	
V_{DD}	Supply voltage		4.5	5.0	5.5	4.5	5.5	V
V_{IH1}	TTL Input High Voltage		2.0			2.0		V
V_{IL1}	TTL Input Low Voltage				0.8		0.3	V
V_{IH2}	CMOS Input High Voltage		3.5			3.5		V
V_{IL2}	CMOS Input Low Voltage				1.5		1.0	V
V_{OH1}	TTL Output High Voltage	I_{OH} = -1mA	V_{DD}-0.4			V_{DD}-0.4		V
V_{OL1}	TTL Output low Voltage	I_{OL} = 2.0mA			0.4		0.4	V
V_{OH2}	CMOS Output High Voltage	I_{OH} = -1mA	V_{DD}-0.4			V_{DD}-0.4		V
V_{OL2}	CMOS Output low Voltage	I_{OL} = 2.0mA			0.4		0.4	V
I_{IL}	Input Low Current				-10		100	uA
I_{IH}	Input High Current				10		100	uA
I_{OZL}	IO Low Current				-50		-100	uA
I_{OZH}	IO High Current				50		100	uA
I_{DD}	Power Supply Current				25		25	mA

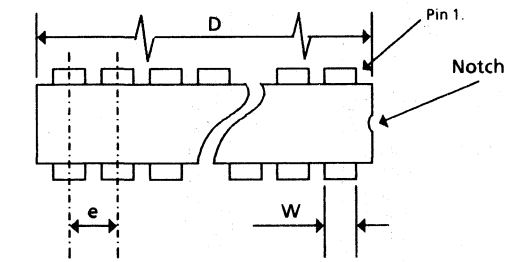
V_{DD} = 5V ± 10%, over full operating temperature range.

Figure 9: Electrical Characteristics

MA3690/1

Radiation Hard 1553B Bus Controller/ Remote Terminal

Outlines



Ref.	Min.	Nom.	Max.
A			5.60 (0.220)
A_1	0.38 (0.015)		1.53 (0.060)
b	0.35 (0.014)		0.59 (0.023)
c	0.20 (0.008)		0.36 (0.014)
D			51.57 (2.424)
e		2.54 (0.100) typ	
e_1		15.24 (0.600) typ	
H	4.71 (0.185)		5.38 (0.212)
M_E			15.90 (0.626)
W			1.53 (0.060)
Dimensions in mm (inches)			

MEDL XG426

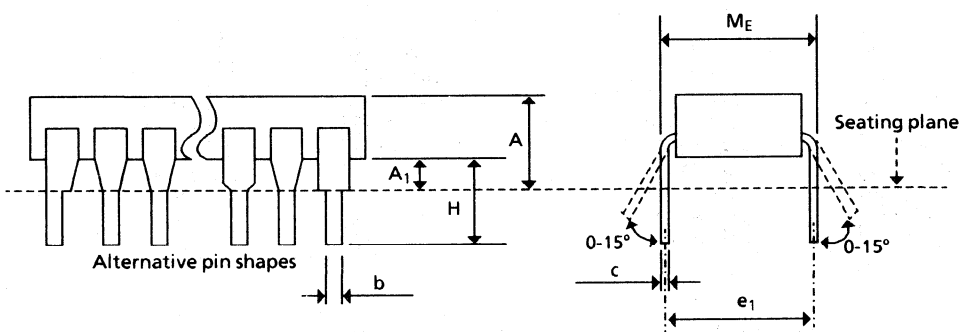
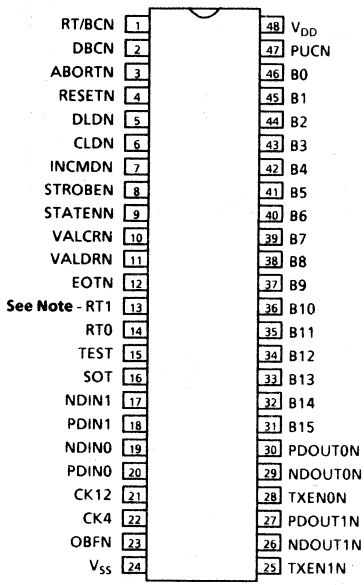


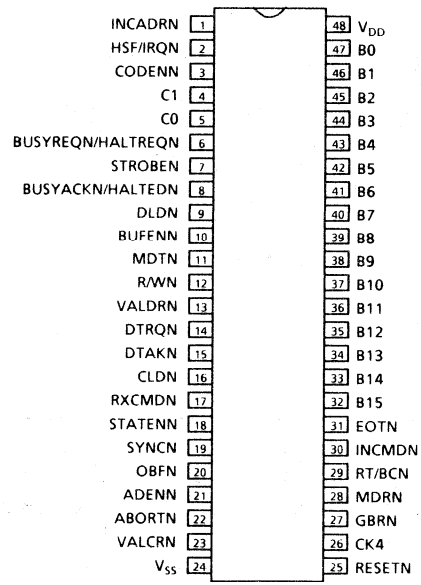
Figure 10a. 48-Lead Ceramic DIL (solder seal) - package style C

6

TRANSCEIVER CHIP (MA3690)



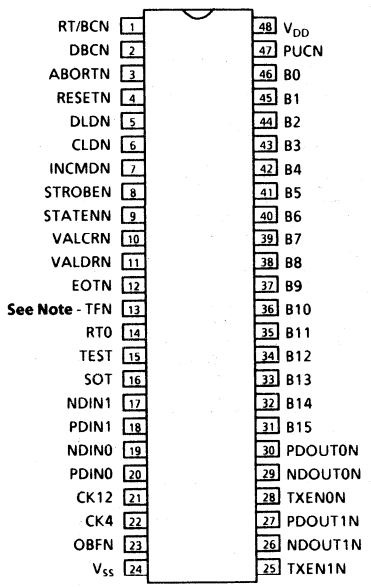
TERMINAL CONTROLLER CHIP (MA3691)



Note: On the MA3693 RT1 is replaced by Terminal flag TFN (TTL output)

Figure 10b: 48-Lead Ceramic DIL (solder seal) - package style C

TRANSCEIVER CHIP (MA3693)
(For applications that require access to Terminal flag)



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Note: The MA3693 has terminal flag (TFN) latched signal OUTPUT on pin 13 (TTL)
This replaces the RT1 signal INPUT that is used on the MA3690 standard version.

Figure 10c: 48-Lead Ceramic DIL (solder seal) - package style C

List of Timings

1	CLOCK TIMING
2	POWER UP CLEAR (PUC)
3	SUBSYSTEM RESET
4	Minimum no response timeout
5	ABORT
6	START of transmission/End of transmission
7	RT_ COMMAND reception and SUBSYSTEM STATUS read
8	RT_ BC-RT DATA transfer (non-mode) + STATUS
9	RT_ STATUS + RT-BC DATA (non-mode)
10	RT_ Received MODE DATA + STATUS
11	RT_ STATUS + transmit MODE DATA transfer
12	RT_ BROADCAST BC-RT DATA transfer (non-mode)
13	RT_ BROADCAST received MODE DATA transfer
14	RT_ MODE COMMAND no data (T/R = 1)
15	RT_ Terminal response time
16	RT_ RT-RT Validation timeout
17	RT_ Busy Handshake
18	RT_ STATUS LOAD
19	BC_ Message FETCH
20	BC_ REPORT cycle. RT-RT no data to subsystem
21	BC_ REPORT cycle. RT-BC
22	BC_ Intermessage gap
23	BC_ NO OPERATION
24	BC_ SELF TEST
25	BC_ PASSIVE MONITOR
26	BC_ DATA TRANSFER HANDSHAKE
27	BC_ RETRY

Figure 11

Symbol	Description	Min.	Typ.	Max.	Units
t1	CK4 to BUS [B0:B15] VALID			235	nS
t2	CK4 to BUS [B0:B15] High Impedance			220	nS
t3	B0:B15 set up wrt STROBEN ↑	15			nS
t4	B0:B15 hold wrt STROBEN ↑	20			
t5	VALCRN ↓ to RXCMDN ↓		3t		
t6	Pulse width RXCMDN, R/WN, STATENN, BUFENN, CLDN, DLDN, MDTN, CODENN		3t		
t7	Pulse width STROBEN, GBRN, MDRN, SYNCN, IRQN		1t		
t7a	RXCMDN/R/WN/STATENN/BUFENN/CLDN/DLDN /MDTN, CODENN ↓ to STROBEN		1t		
t7b	As 7a from STROBEN ↑		1t		
t8	RXCMDN ↑ to INCMD ↓		4t		
t9	INCMDN ↓ to STATENN ↓		3t		
t10	VALCRN pulse width		5t		
t11	VALDRN ↓ to DTRQN ↓			1t	
t12	DTRQN ↓ to DTAKN ↓ (RXDATA)	0		3t	
t13	DTAKN ↓ to BUFENN ↓	1t		2t	
t14	DTRQN ↑ to CLDN ↓		24t		
t15	CLDN ↑ to GBRN ↓	15t		16t	
t16	CLDN ↓ to STATUS valid BUS B0:B15			85	nS
t17	CLDN ↑ to STATUS invalid on B0:B15	35			nS
t18	DTRQN ↑ to DTAKN ↑	0			
t19	STATENN to CLDN ↓ Non mode data	11t		12t	
t20	CLDN ↑ to DTRQN ↓		15t		
t21	DTRQN ↓ to DTAKN ↓ (TX data)	0		54t	
t22	VALDRN ↓ to R/WN ↓	2t		3t	
t23	MDTN ↓ to CLDN ↓		24t		
t24	CLDN ↑ to MDRN ↓		14t		
t25	STATENN to CLDN ↓ mode data	11t		12t	
t26	CLDN ↑ to MDTN ↓	15t		16t	
t27	MDTN ↑ to INCMDN ↑	77t		78t	
t28	DTRQN ↑ to INCMDN ↑ (non broadcast)	77t		78t	
t29	DTRQN ↑ to INCMDN ↑ (broadcast)		25t		
t30	MDTN ↑ to INCMDN ↑ (broadcast)		25t		
t31	CLDN ↑ to INCMDN ↑ (mode)	11t		12t	
t32	CLDN ↑ to TXENN ↓	1t		2t	
t33	TXENN/PDOUTN/NDOUTN/prop delay difference		6		nS
t34	Start of transmission to EOTN ↑		$76t_{12}$		
t34a	End of transmission to EOTN ↓		$82t_{12}$		
t35	End of transmission to ABORTN ↓ 1) RT1 = 0 RT0 = 0 2) RT1 = 0 RT0 = 1 3) RT1 = 1 RT0 = 0 4) RT1 = 1 RT0 = 1		 20 26 48 112		uS
t36	Minimum no response timeout 1) RT1 = 0 RT0 = 0 2) RT1 = 0 RT0 = 1 3) RT1 = 1 RT0 = 0 4) RT1 = 1 RT0 = 1	 15.75 21.75 43.75 107.75		 16.25 22.25 44.25 108.25	uS

Figure 12a

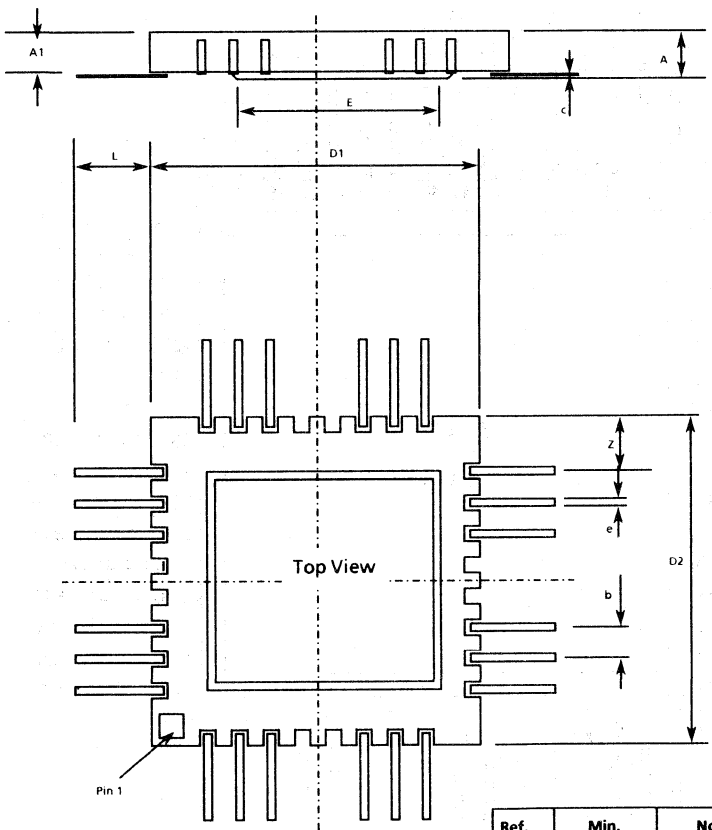
Symbol	Description	Min.	Typ.	Max.	Units
t37	Remote terminal response time	10.3		11.25	uS
t38	Minimum PUCN pulse width	20			nS
t39	PUCN ↓ to RESET ↓			75	nS
t40	RESETN ↓ to ADEN ↓			80	nS
t41	PUCN ↑ to RESETN ↑		2t		
t42	RESETN ↑ to ADENN ↑		2t	2t + 80	nS
t43	Initialisation word set-up wrt RESETN ↑	15			nS
t44	Initialisation word HOLD wrt RESETN ↑	20			nS
t45	Minimum RESETN pulse width	75			nS
t46	Minimum CK12 high	30			nS
t47	Minimum CK12 low	15			nS
t48	CK12 ↑ to CK4 ↑			90	nS
t49	CK12 ↓ to CK4 ↓			90	nS
t50	HALTREQN pulse width	1t			
t51	HALTREQN ↑ to HALTEDN ↑			55	nS
t52	HALTREQN ↑ to CODENN ↓	1t		2t	
t53	CODENN ↑ to CODENN ↓		2t		
t54	RT-RT minimum validation time 1) RT1 = 0 RT0 = 0 2) RT1 = 0 RT0 = 1 3) RT1 = 1 RT0 = 0 4) RT1 = 1 RT0 = 1	 55.75 61.75 83.75 147.75		 56.25 62.25 84.25 148.25	uS
t55	HALTREQN setup for next message wrt to INCMDN ↑		150		nS
t56	R/WN ↓ to R/WN ↓ RT-BC Report cycle		80t		
t57	BUFENN ↑ to BUFENN ↓ Data word to report word		29t		
t58	BC intermessage gap 1) without a No Operation instruction 2) with a No Operation instruction		 20 28		uS
t59	CODENN interval high between received status and report word during report cycle		24t		
t60	CODENN interval between report word and next message fetch for continuous operation		6t		
t61	CODEN interval between BC Noop data pointer fetch and report word		5t		
t62	INCMDN ↑ to INCADDRN ↓		1t		
t63	BUSYREQN ↓ to BUSYACKN ↓			60	nS
t64	BUSYREQN ↑ to BUSYACKN ↑			60	nS
t65	INCMDN ↑ to BUSYACKN ↓		60		nS
t66	INCMDN ↑ to BUSYACKN ↑		100		nS
t67	CK4 ↑ to R/WN/BUFENN/CO/C1/CODENN/MDTN			115	nS

Notes: 1. t = CK4 period, t_{12} = CK12 period

2. Times quoted as typical means a fixed number of CK4 clock cycles but excludes slight variations due to propagation delays.

Conditions: V_{dd} = 4.5 to 5.5V, T_{amb} = -55°C to + 125°C, V_{IL} = 0V, V_{IH} = 4V, V_{OUT} Threshold = 1.5V except t_2 where measured by a 1.0V change in output voltage. Load = 50pf except t_2 where additional 1K load to 0V or V_{DD}.

Figure 12b (continued)

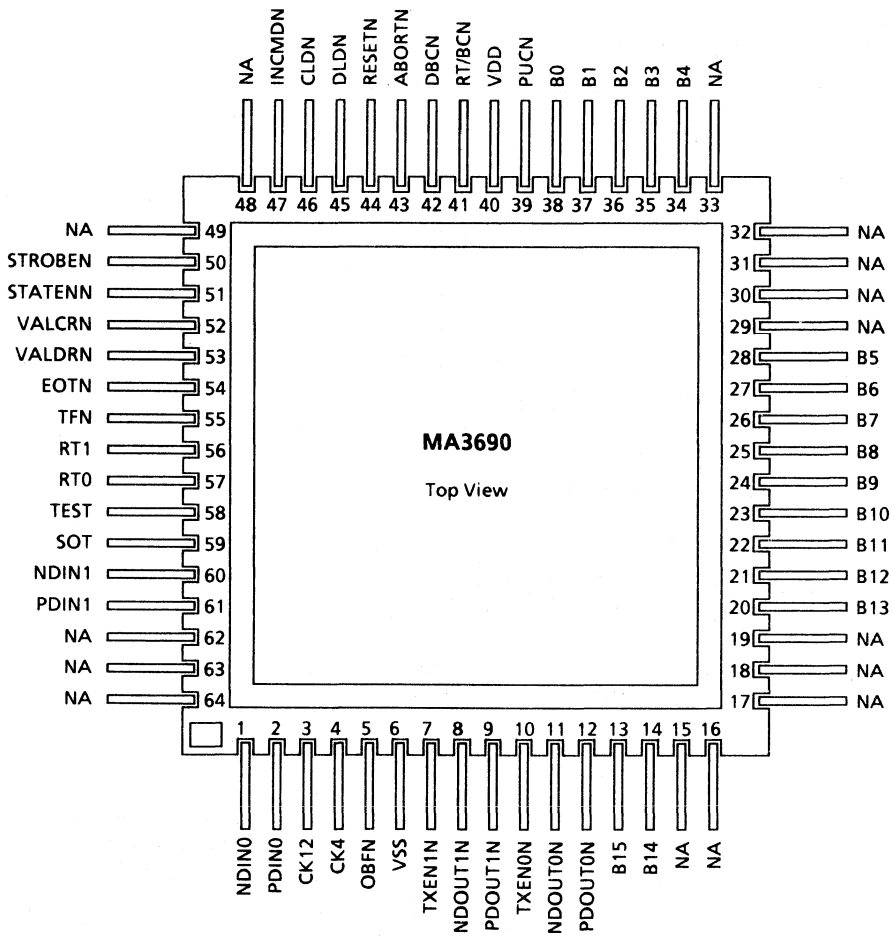


Ref.	Min.	Nom.	Max.
A			0.085
A_1	0.038		0.042
b	0.016		0.020
c	0.009		0.012
D1 D2			0.910
E		0.605 sq	0.490 sq
e		0.050	
L	0.350		0.445
Z	0.065		0.085

Dimensions in mm (inches)

MEDL XG487

Figure 13a: 64-Lead Topbraze Flatpack (Package style F)



MA3690A

The MA3690A is packaged in a 48-pin DIL, with Pin No. 13 being TF (Terminal Flag) instead of RT1 (Reply Timeout 1), the RT1 signal being pulled down internally.

Figure 13b: 64-Lead Topbraze Flatpack (Package style F)

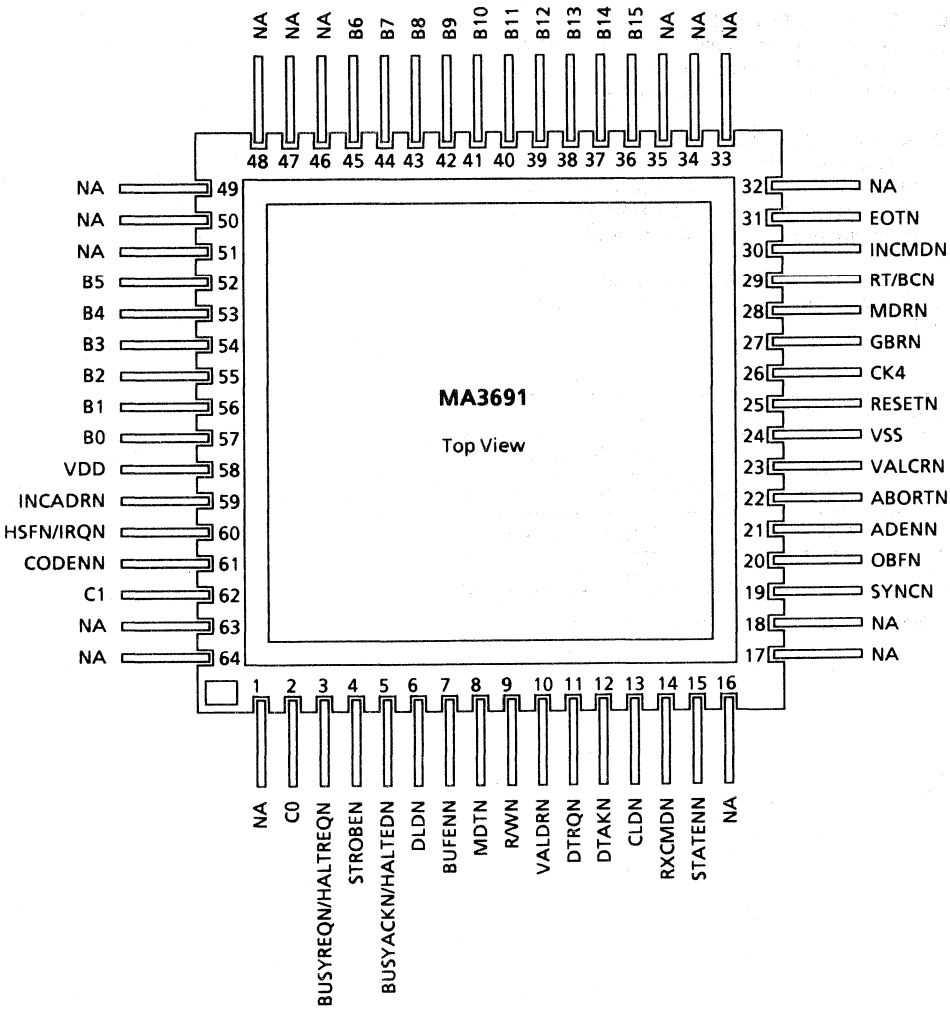


Figure 13c: 64-Lead Topbraze Flatpack (Package style F)

Radiation Hard 1553B Bus Controller/ Remote Terminal

RadiationTolerance

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

Total Dose (Function to specification)	$3x10^5$ Rad(Si)
Transient Upset (survivability)	$>10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$1x10^{15}$ neutrons/cm^2
Single Event Upset (GSO 10% worst case)	$<10^{-10}$ errors/bitday
Latch-up	Not possible

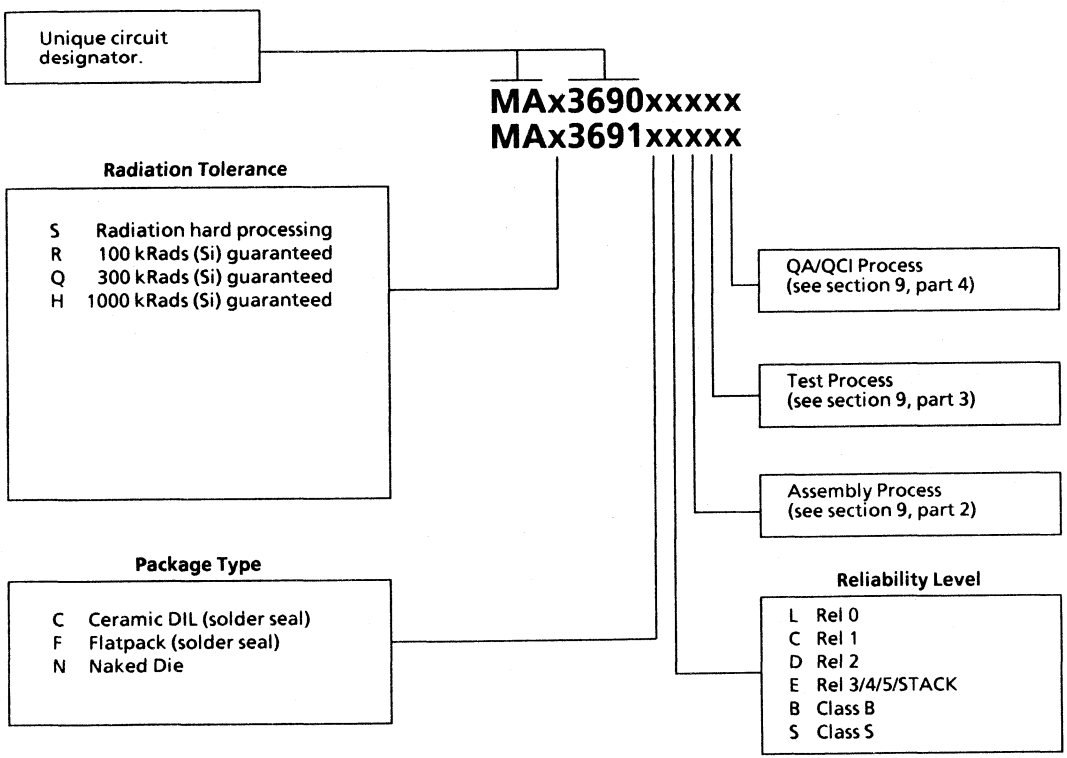
Figure 14: Radiation Hardness Parameters

MA3690/1

Radiation Hard 1553B Bus Controller/ Remote Terminal

Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



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GEC PLESSEY

SEMICONDUCTORS

S10402ADS/1 Issue 1.4 December 1990

MA3692

Radiation Hard MIL-STD-1553B to 16-Bit Processor Interface

(Advance Data)

Features

- **Radiation Hard to 1MRad(Si)**
- **High SEU immunity, latch-up free**
- **CMOS-SOS technology**
- **All inputs & outputs are fully TTL & CMOS compatible**
- **High speed, Low power**
- **Compatible with MA3690/1 Mil Std 1553B Remote Terminal / Bus Controller / Passive Monitor**

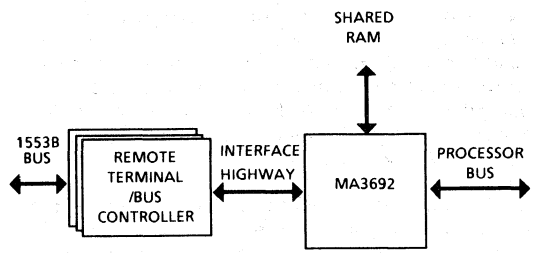

Figure 1: Block Diagram

General Description

The MA3692 is a multi-function device for interfacing between Mil. Std. 1553B Data Bus controller/remote terminals and a range of 16-bit processors.

The device uses low power Silicon-on-Sapphire technology for radiation hardness up to 1MRad (Si) with high speed, latch-up free operation.

To obtain a degree of flexibility this interface permits the use of 1750A (MAS281), Z800X, 68000 and 8086 processors. The interface between the RT/BC terminal and microprocessor uses shared store technique. This shared store allows the information to be utilised by either the processor or the terminal in such a manner as to provide data consistency in all forms of data transfer. Hence no data corruption or unusable data will result.

Furthermore all subsystem processor I/O accessed with the I/F and shared RAM does not result in data, status or flags being corrupted or lost.

The algorithm and method is implemented in the interface device with minimal external device requirements. Remote Terminal, active Bus Controller and Passive Monitor mode are supported allowing the full facilities of the MA3690/1 chip set to be exploited. In Passive Monitor Mode command, status and data information is also stored in the shared memory.

Radiation Hard MIL-STD-1553B to 16-Bit Processor Interface
(Advance Data)

Operation

General
The MA3690/1 1553B terminal provides all of the required signals for control of data flow from the main 1553B buses and the subsystem. In this system these control signals are utilised by the MA3692 to provide appropriate control of the shared RAM. The addressing capability of the MA3692 is set at 32kx16 words (expandable to 64kx16 words).

Transferrable data is mapped into this RAM with the MA3692 providing the address, data strobe and chip select. The range of data stored in the RAM consists of:

1. RT Mode:
   Command.
   Data (non-mode and mode).
2. BC Mode:
   Instruction sequences with appropriate 1553B command words.
   Report words with relevent 1553B status information.
   Data.
3. Passive Monitor:
   Command
   Status
   Data

Memory Access
Latched addressing takes place within the MA3692 and therefore SRAMs without internal latched addressing must be used. Maximum access time for the SRAM's are as follows:

1. Achitecture 1 ≤150ns
2. Achitecture 2 ≤70ns

The MA3692 does not incorporate byte addressing.

Processor Interface
The range of processors to which this device interfaces are the Mil Std 1750A (MAS281), Z800X, 8086, and 68000. The choice of the correct interface will be selected by two external pins on the device giving the results:

P0	P1	PROCESSOR
0	0	Z800X
0	1	8086
1	0	68000
1	1	1750A

MA3690/1 Timing
This documentation describes the chip set signals used in subsystem transfers.

MA3692

Radiation Hard MIL-STD-1553B to 16-Bit Processor Interface

(Advance Data)

System Operation

Architecture 1 (Figure 2)

In all modes of operation the MA3692 utilises a shared store composed of two identical RAMs, one addressed by the processor and one by the 1553B terminal. Both RAMs are available to both the processor and the 1553B terminal though not at the same time. The internal memory mapping of the RAMs is identical, such that they constitute two versions of the shared stores. In order to swap between the two RAMs the processor makes a request via an XIO command.

Architecture 2 (Figure 3)

This architecture uses one RAM as the shared store. To maintain data consistency in RT mode the shared store features double-buffering of the data stores. The MA3692 incorporates a low level contention and arbitration scheme to handle the possible contentions of access to the shared stores given by this architecture.

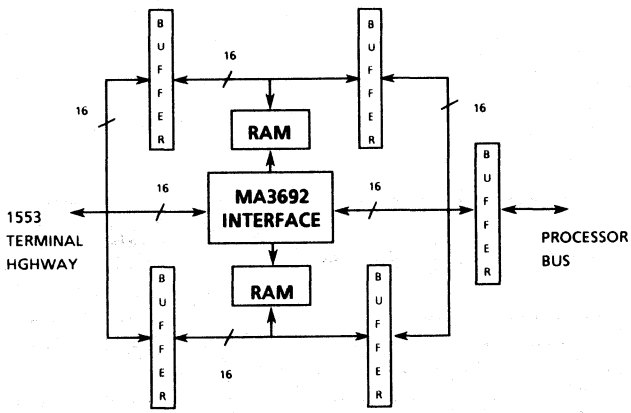

Figure 2: Architecture 1

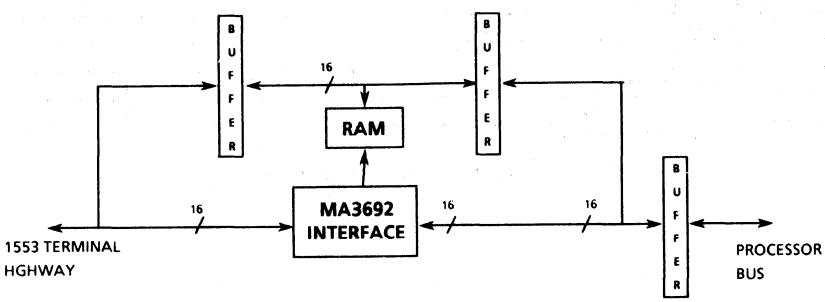

Figure 3: Architecture 2

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DC Characteristics and Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0.5	10	V
V_I	Input voltage	-0.3	V_{DD} + 0.3	V
T_A	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Figure 4: Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Conditions	Total dose radiation not exceeding $3x10^5$ Rad (Si)			Total dose ≤1 MRad (Si)		Units
			Min.	Typ.	Max.	Min.	Max.	
V_{DD}	Supply voltage		4.5	5.0	5.5	4.5	5.5	V
V_{IH1}	Input High Voltage		2.0			2.0		V
V_{IL1}	Input Low Voltage				0.8		0.3	V
V_{OH1}	Output High Voltage	I_{OH} = -1mA	V_{DD}-0.4			V_{DD}-0.4		V
V_{OL1}	Output low Voltage	I_{OL} = 2.0mA			0.4		0.4	V
I_{IL}	Input Low Ccurrent				-10		-100	uA
I_{IH}	Input High Current				10		100	uA
I_{OZL}	IO Low Current				-50		-100	uA
I_{OZH}	IO High Current				50		100	uA
I_{DD}	Power Supply Current				10		10	mA
I_{DDYN}	Dynamic Power Supply Current				20		20	mA

V_{DD} = 5V ± 10%, over full operating temperature range.

Figure 5: Electrical Characteristics

MA3692

Radiation Hard MIL-STD-1553B to 16-Bit Processor Interface
(Advance Data)

Pin Descriptions

$\overline{\text{ADENI}}$ Address Enable
In RT mode, is activated as part of the reset routine to enable the terminal address, address parity and broadcast enable lines.

$\overline{\text{STROBEI}}$ Strobe
Used as an information transfer strobe pulse for words being transferred on the terminal data highway. Data is valid when transferred at this time.

$\overline{\text{STATENI}}$ Status Enable
In RT mode, used to enable the contents of the subsystem status latch onto the terminal data highway (THIGHO[0:7]). In Bus Control mode this line indicates that the BC Report Word is active on the highway.

CK4I 4 MHz System Clock

THIGHO[0:15] Terminal Highway
16 bit bidirectional data highway, THIGHO[0] being the least significant bit.

$\overline{\text{RXCMDI}}$ Recieve Command
In RT mode, indicates that a valid command is present on the terminal data highway. In BC mode with the terminal configured as a Passive Monitor this line indicates that the data on the terminal highway is a valid command/status word.

$\overline{\text{GBRI}}$ Good block received
Indicates that the non-mode data received by the terminal forms a valid message and may be used. This signal is used in both RT and BC modes.

$\overline{\text{INCMDI}}$ In command
When low this line indicates that the terminal is currently servicing a command word.

$\overline{\text{MDTI}}$ Mode Data Transfer
In RT mode, indicates that the data word being transferred is associated with a mode command. In BC mode with the terminal operating as a Passive Monitor, indicates that a valid data word is on the terminal highway.

$\overline{\text{MDRI}}$ Mode Data Received
Indicates that the mode data received by the terminal forms a valid message and may be used.

$\overline{\text{TRWI}}$ Terminal Read/Write
Indicates the direction of data transfer between the terminal and the subsystem. When low, data is being written to the subsystem RAM.

$\overline{\text{DTRQI}}$ Data Transfer Request
Goes low to request permission to transfer a non-mode data word to or from the subsystem.

$\overline{\text{SYNCI}}$ Synchronise
Pulses low if a vaild Synchronise without data mode command has been received.

$\overline{\text{DBCI}}$ Dynamic Bus Control
Pulses low if a valid Dynamic Bus Control command has been received by the terminal and that the control has been accepted.

$\overline{\text{CODENI}}$ Code Enable
Indicates that a word transfer between the terminal and either the instruction store or the Report store is in effect.

C0I,C1I Instruction/ Report Code Bits
Used to address the instruction and report stores for the transfer of information.

$\overline{\text{INCADDRI}}$ Increment Address
Pulses low to increment the Instruction/Report word addressing counter

$\overline{\text{RTBCI}}$ Remote Terminal/ Bus Control Select
Driven by the subsystem; high for RT mode, low for BC mode

$\overline{\text{HALTEDI}}$ Halted/Busy Acknow-ledge
In BC mode, indicates that all terminal operation has been halted and the terminal is waiting for the next instruction to be executed.

$\overline{\text{IRQI}}$ Interrupt Request
Pulses low to indicate that a BC interrupt has been generated.

RTADI[0:4] RT Address Lines
Output to the terminal on the data highway on a terminal reset, using THIGHO[0:4].

RTADPARI RT Address Parity
Output to the terminal on the data highway on a terminal reset, using THIGHO[5].

$\overline{\text{BCSTENI}}$[0:1] Broadcast Enable Lines
Output to the terminal on the data highway on a terminal reset, using THIGHO[6:7]. Used to select the broadcast address detect function of the terminal.

$\overline{\text{BBRI}}$ Bad Block Received
Indicates that the data received forms an invalid message. This input is part of the interrupt request system to the susbsytem processor. Used in conjunction with $\overline{\text{BBRO}}$.

$\overline{\text{BTXI}}$ Block Transmit
The terminal has attempted to read a subaddress for data to be transmitted. This input is part of the interrupt request system to the subsystem. Used in conjunction with $\overline{\text{BTXO}}$.

$\overline{\text{SSWRII}}$ Subsystem Write Reset
When low, a valid reset mode command does not alter the contents of the RT subsystem status word. When set high, a reset mode command initialises the staus as normal.

ICSELI Illegal Command Select
When low, allows the subsystem processor to set the value of the terminal Illegal Command line in the subsystem status latch. When high, the Illegal Command line may be controlled by the MSB of the subaddress field of the received command word.

$\overline{\text{RESET1I}}$ Reset 1
In RT mode only, causes the RT subsystem status word in the device to be initialised, provided SSWRII is high. Is generated by either a valid reset mode command or a subsystem-driven reset.

$\overline{\text{RESET2I}}$ Reset 2
In active BC mode and RT mode, causes the internal circuitry of the device to initialise. In Passive Monitor mode this reset also causes the device to enter the quiescent BC state.

$\overline{\text{HALTREQO}}$ Halt Request/Busy Request
Taken high to request the terminal to commence execution of the next instruction, if in Single Step mode. If in Table Driven mode, keeping this line high causes the terminal to automatically continue at the end of the instruction cycle.

$\overline{\text{BBRO}}$ Bad Block Received
Indicates that the data received by the terminal forms an invalid message and should not be used.

$\overline{\text{BTXO}}$ Block Transmit
Indicates that the terminal has attempted to read a subaddress for data to be transmitted.

$\overline{\text{PMMO}}$ Passive Monitor Mode
Indicates that the terminal is in Passive Monitor mode. Remains active until a RESET2I is received.

$\overline{\text{PMIRQO}}$ Passive Monitor Interrupt
Pulses low to indicate to the subsystem processor that PM mode has been selected. Also pulses low to indicate that the maximum count of the PM counter has been reached.

$\overline{\text{CS0MTC0}}$ Command Stack Zero/ Message Carry
In RT mode, indicates that the RT Command Stack is low. In BC mode, used to provide a Message Carry signal for the Instruction/Report word counter for external expansion purposes.

$\overline{\text{IWCRO}}$ Instruction count compare equal
Generated when the value of the Instruction word count and the value held in the Instruction address compare register are equal. The state remains until the processor updates the Instruction counter or the Instruction address compare register.

P0I,P1I Processor type select
Define the type of processor being used, according to the table shown earlier.

PCLKI Processor Clock

PRWI Processor Read/Write
Indicates the direction of data transfer between the processor and the subsystem. When low, data is being written to the subsystem RAM.

ZDSI Data Strobe
Used as an information transfer strobe pulse for words being transferred on the processor data highway.

VIAKENI Vectored Interrupt Enable
Driven low by the controlling processor when ZDSI is low, during an interrupt acknowledge cycle. Used to enable the interrupt vector onto the processor's bus from the highest priority interrupting device in the daisy chain.

VIAKI Vectored Interrupt Acknow-ledge
Driven low by the controlling processor when acknowledging a vectored interrupt.

IEII Interrupt Enable Input
An interrupt priority control signal which when taken low may be used to prevent the device, and all other lower priority devices from causing an interrupt.

CS1I Chip Select 1 (MA3692)
Used to select the appropriate function within the device for which the data (valid on ZDSI) will be used.

CS2I Chip Select 2 (MA3692)
This chip select is accompanied by any data which is required to be loaded into the registers of the device.

PHIGHO[0:15] Processor Highway
16-bit bidirectional processor data highway. PHIGHO[0] being the **least** significant bit.

WAITO Wait
Used as the input to the processor WAIT line for holding off the processor should the device require an arbitration between a terminal and processor access.

IEOO Interrupt Enable Output
An interrupt priority control signal which should be connected to the next lower priority device's IEII input. This signal is driven low by a device whose IEII input is low or whose interrupt is being serviced.

VIRQO Vectored Interrupt Request
Indicates that either one or both of the interrupt devices within the Interface wishes to interrupt the controlling processor.

VIRQ1O Vectored Interrupt Request
Indicates that the higher priority interrupt device wishes to interrupt the controlling processor.

VIENO Vector Enable
Generated when ZDSI is low and IEII is high and is used to enable the interrupt vector onto the processor's bus during the vectored interrupt acknowledge cycle.

TBUFEN1O Terminal Buffer Enable 1
Used to control the enable to the data buffers on the terminal side of the shared RAMs.

TBUFRW1O Terminal Buffer R/W 1
Used to control the direction of the data transfer between the terminal and the shared RAMs.

TBUFEN2O Terminal Buffer Enable 2
Used to control the enable to the data buffers on the terminal side of the shared RAMs.

TBUFRW2O Terminal Buffer R/W 2
Used to control the direction of the data transfer between the terminal and the shared RAMs.

CS1BO Chip Select 1B (RAM)
Used to provide the chip select to the shared RAMs and is used to address data between 0000 and 7FFF. (Associated with RAM Highway 1)

CS2BO Chip Select 2B (RAM)
As CS1BO, but used to address data between 8000 and FFFF. (Associated with RAM Highway 1)

OE1O Output Enable 1
Used to control the output enable line of the RAMs directly. (Associated with RAM Highway 1)

WE1O Write Enable 1
Used to provide write enable access to the RAM. (Associated with RAM Highway 1)

RAMHIGH1O [0:14] RAM Highway 1
15-bit RAM 1 data highway.

$\overline{\text{PBUFEN1O}}$ Processor Buffer Enable 1
Used to control the enable to the data buffers on the processor side of the shared RAMs.

PBUFR$\overline{\text{W}}$1O Processor Buffer R/W 1
Used to control the direction of the data transfer between the processor and the shared RAMs.

$\overline{\text{PBUFEN2O}}$ Processor Buffer Enable 2
Used to control the enable to the data buffers on the processor side of the shared RAMs.

PBUFR$\overline{\text{W}}$2O Processor Buffer R/W 2
Used to control the direction of the data transfer between the processor and the shared RAMs.

$\overline{\text{CS1AO}}$ Chip Select 1 (RAM)
Used to provide the chip select to the shared RAMs and is used to address data between 0000 and 7FFF. (Associated with RAM High 2)

$\overline{\text{CS2AO}}$ Chip Select 2 (RAM)
As CS1AO, but used to address data between 8000 and FFFF. (Associated with RAM High 2)

$\overline{\text{OE2O}}$ Output Enable 2
Used to control output enable of the RAMs directly. (Associated with RAM Highway 2)

$\overline{\text{WE2O}}$ Write Enable 2
Used to provide write enable access to the RAM. (Associated with RAM High 2)

RAMHIGH2O [0:14] RAM Highway 2
15-bit RAM 2 data highway.

TNBI Test Use Only
For normal operation connect to logic '1'.

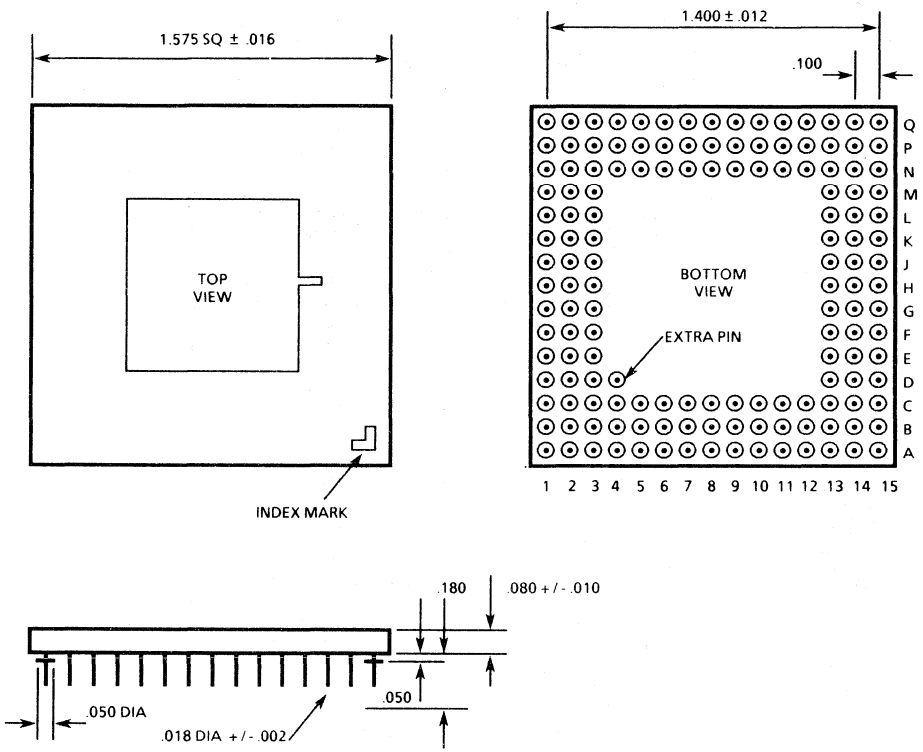
ARCHI Architecture Select
'1' = ARCH 1 (2 RAM Architecture).
'0' = ARCH 2 (Single RAM).

C7	V_{DD}	N2	$\overline{BBRO}$	L14	$\overline{WE2O}$
A7	$\overline{ADENI}$	P1	$\overline{BBRI}$	M15	RAMHIGH2O[0]
A6	$\overline{STROBEI}$	M3	$\overline{BTXO}$	K13	RAMHIGH2O[1]
B7	$\overline{STATENI}$	N3	$\overline{BTXI}$	K14	RAMHIGH2O[2]
B6	CK4I	P2	$\overline{PMMO}$	L15	RAMHIGH2O[3]
C6	THIGHO[0]	Q1	$\overline{PMIQO}$	J14	RAMHIGH2O[4]
A5	THIGHO[1]	N4	$\overline{SSWRII}$	J13	RAMHIGH2O[5]
B5	THIGHO[2]	P3	$\overline{CS0MTCO}$	K15	RAMHIGH2O[6]
A4	THIGHO[3]	Q2	$\overline{IWCRO}$	J15	RAMHIGH2O[7]
A3	THIGHO[4]	P4	$\overline{ICSELI}$	H14	RAMHIGH2O[8]
B4	THIGHO[5]	N5	$\overline{RESET1I}$	H15	RAMHIGH2O[9]
C5	THIGHO[6]	Q3	$\overline{RESET2I}$	H13	Not Connected
B3	THIGHO[7]	P5	$\overline{WAITO}$	G13	Not Connected
A2	THIGHO[8]	Q4	$\overline{TBUFEN1O}$	G15	RAMHIGH2O[10]
C4	THIGHO[9]	N6	$\overline{TBUFRW1O}$	F15	RAMHIGH2O[11]
C3	THIGHO[10]	P6	$\overline{TBUFEN2O}$	G14	RAMHIGH2O[12]
B2	THIGHO[11]	Q5	$\overline{TBUFRW2O}$	F14	RAMHIGH2O[13]
A1	THIGHO[12]	P7	$\overline{CS2BO}$	F13	RAMHIGH2O[14]
D3	THIGHO[13]	N7	$\overline{CS1BO}$	E15	PCLKI
C2	THIGHO[14]	Q6	$\overline{OE1O}$	E14	$\overline{PRWI}$
B1	THIGHO[15]	Q7	$\overline{WE1O}$	D15	$\overline{ZDS}$
D2	$\overline{RXCMDI}$	P8	P0I	C15	VIRQO
E3	$\overline{GBRI}$	Q8	P1I	D14	VIRQ1O
C1	$\overline{INCMDI}$	N8	V_{SS}	E13	$\overline{VIENO}$
E2	$\overline{MDTI}$	N9	V_{DD}	C14	$\overline{VIAKI}$
D1	$\overline{MDRI}$	Q9	TNBI	B15	$\overline{VIAKENI}$
F3	$\overline{TRWI}$	Q10	RAMHIGH1O[0]	D13	$\overline{IEOO}$
F2	$\overline{DTRQI}$	P9	RAMHIGH1O[1]	C13	$\overline{IEII}$
E1	$\overline{SYNCI}$	P10	RAMHIGH1O[2]	B14	$\overline{CS1I}$
G2	$\overline{DBCI}$	N10	RAMHIGH1O[3]	A15	$\overline{CS2I}$
G3	$\overline{CODENI}$	Q11	RAMHIGH1O[4]	C12	PHIGHO[0]
F1	C0I	P11	RAMHIGH1O[5]	B13	PHIGHO[1]
G1	C1I	Q12	RAMHIGH1O[6]	A14	PHIGHO[2]
H2	$\overline{INCADRI}$	Q13	RAMHIGH1O[7]	B12	PHIGHO[3]
H1	$\overline{RTBCI}$	P12	RAMHIGH1O[8]	C11	PHIGHO[4]
H3	Not Connected	N11	RAMHIGH1O[9]	A13	PHIGHO[5]
J3	Not Connected	P13	RAMHIGH1O[10]	B11	PHIGHO[6]
J1	$\overline{HALTEDI}$	Q14	RAMHIGH1O[11]	A12	PHIGHO[7]
K1	$\overline{HALTREQO}$	N12	RAMHIGH1O[12]	C10	PHIGHO[8]
J2	$\overline{IRQI}$	N13	RAMHIGH1O[13]	B10	PHIGHO[9]
K2	RTADI[0]	P14	RAMHIGH1O[14]	A11	PHIGHO[10]
K3	RTADI[1]	Q15	$\overline{PBUFEN1O}$	B9	PHIGHO[11]
L1	RTADI[2]	M13	$\overline{PBUFRW1O}$	C9	PHIGHO[12]
L2	RTADI[3]	N14	$\overline{PBUFEN2O}$	A10	PHIGHO[13]
M1	RTADI[4]	P15	$\overline{PBUFRW2O}$	A9	PHIGHO[14]
N1	RTADPARI	M14	$\overline{CS2AO}$	B8	PHIGHO[15]
M2	$\overline{BCSTEN0I}$	L13	$\overline{CS1AO}$	A8	ARCHI
L3	$\overline{BCSTEN1I}$	N15	$\overline{OE2O}$	C8	V_{SS}

GEC PLESSEY
SEMICONDUCTORS

Outline and Pin Assignments

144-Pin Grid Array



MA3692

Radiation Hard MIL-STD-1553B to 16-Bit Processor Interface

(Advance Data)

RadiationTolerance

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

Total Dose (Function to specification)	$3x10^5$ Rad(Si)
Transient Upset (survivability)	$>10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$1x10^{15}$ neutrons/cm^2
Single Event Upset (GSO 10% worst case)	$<10^{-10}$ errors/bitday
Latch-up	Not possible

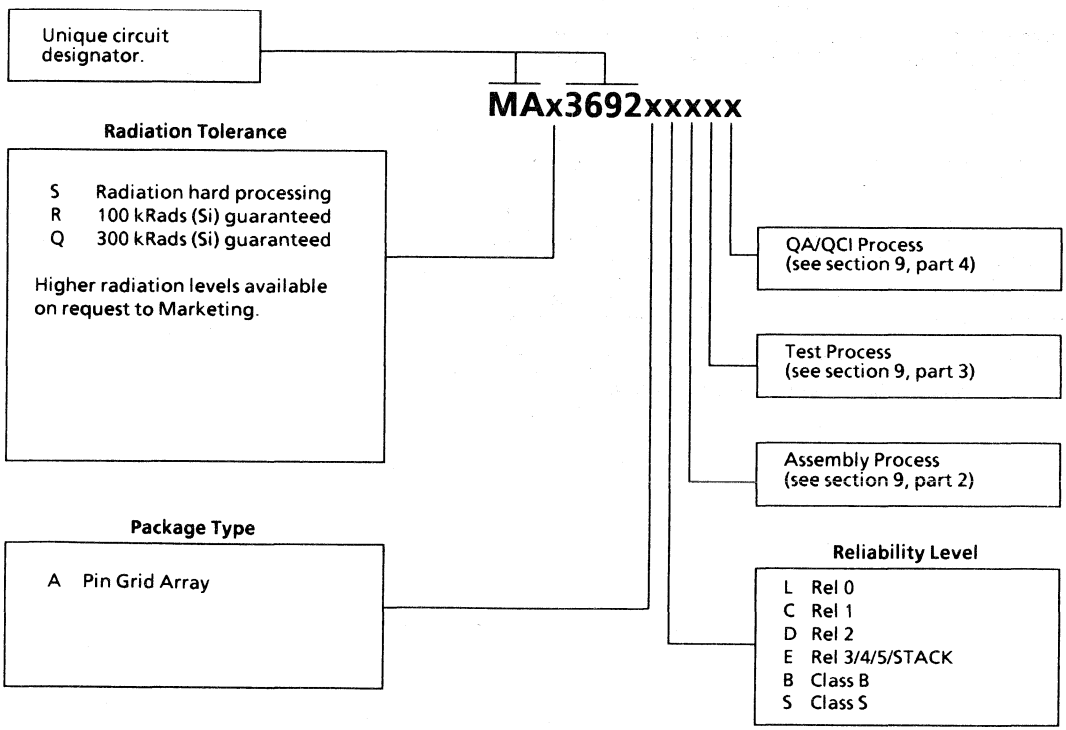
Figure 6: Radiation Hardness Parameters

Radiation Hard MIL-STD-1553B to 16-Bit Processor Interface
(Advance Data)

GEC PLESSEY
SEMICONDUCTORS

Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



GEC PLESSEY

SEMICONDUCTORS

MAS15530

Radiation Hard Manchester Encoder - Decoder

S10400FDS Issue 1.3 November 1990

Features

- MIL-STD-1553 compatible
- Radiation Hard
- 1.25 megabit/sec. Maximum Data Rate
- Sync Identification and Lock-in
- Clock Recovery
- Manchester II Encode/Decode
- Separate Encoder and Decoder Sections
- Low Operating Power
- Military Temperature Range - 55°C to 125°C
- Direct Replacement for Harris HD15530

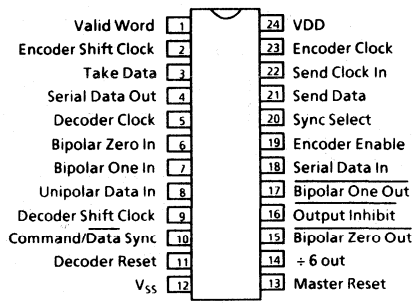


Figure 1: Pin Assignment

General Description

The MAS15530 is a high performance CMOS integrated circuit used to implement MIL-STD-1553 and similar Manchester II encoded, time division multiplexed, serial data protocols. The device is divided into two independent sections, encoder and decoder, with a common master reset. The function of the encoder section is to produce the sync pulse and parity bit, and encode the data bits. The decoder section recognises the sync pulse, decodes the data bits and checks for parity.

The MAS15530 is fully guaranteed to support the 1 MHz data rate of MIL-STD-1553 over the full temperature and supply voltage ranges. The device interfaces with CMOS, TTL or N-channel support circuitry and operates from a standard 5 volt supply. This circuit can also be used in many party line digital data communications applications.

6

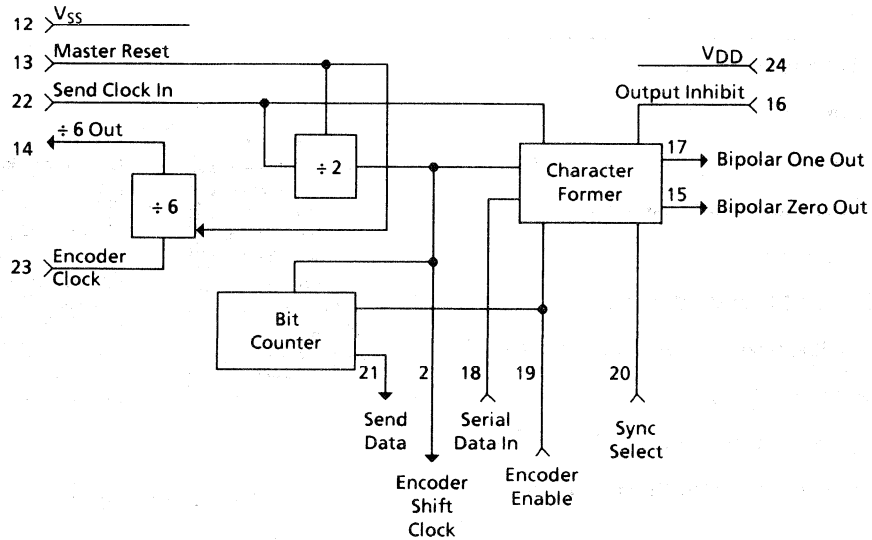


Figure 2. Encoder Block Diagram

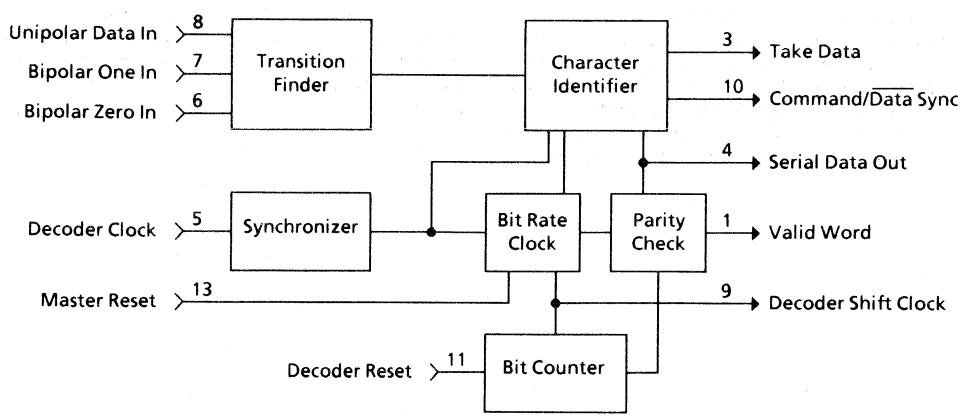


Figure 3. Decoder Block Diagram

MAS15530

Radiation Hard Manchester Encoder - Decoder

Pin Designations

Pin	Input	Output	Enc	Dec	Function	Comment
1		√		√	Valid word	A 'high' signals the receipt of a valid word
2		√	√		Encoder Shift Clock	Shifts data into the encoder on a 'low' to 'high' transition
3		√		√	Take Data	'high' during data reception after the sync pulse is identified
4		√		√	Serial Data Out	NRZ output of received data
5	√			√	Decoder Clock	Clock for the transition finder and synchronizer which generates the clock for the rest of the decoder
6	√			√	Bipolar Zero In	Should be 'high' when the bus is in a negative state. Must be tied 'high' when the unipolar input is used
7	√			√	Bipolar One In	Should be 'high' when the bus is in a positive state. Must be tied 'low' when the unipolar input is used
8	√			√	Unipolar Data In	Input for unipolar data to the transition finder. Must be tied 'low' when not used
9		√		√	Decoder Shift Clock	Provides the DECODER CLOCK divided by 12, synchronized by the recovered serial data
10		√		√	Command/$\overline{\text{Data}}$ Sync	This output indicates the type of synchronizing character received as follows: If a data synchronizing character was received, this pin is low while the data is decoded. If a command synchronizing character was received, this pin is high during data decoding
11	√			√	Decoder Reset	A 'high' during a DECODER SHIFT CLOCK rising edge resets the bit counter
12	–	–	√	√	V_{SS}	Ground
13	√		√	√	Master Reset	A 'high' clears the counters in both sections
14		√	√		÷ 6 Out	Provides the ENCODER CLOCK divided by 6
15		√	√		$\overline{\text{Bipolar Zero Out}}$	Provides an active 'low' output to the zero or negative sense of a bipolar line driver
16	√		√		$\overline{\text{Output Inhibit}}$	A 'low' inhibits the $\overline{\text{BIPOLAR ZERO OUT}}$ and $\overline{\text{BIPOLAR ONE OUT}}$ by forcing them to inactive, 'high', states
17		√	√		$\overline{\text{Bipolar One Out}}$	Provides an active 'low' output to the one or positive sense of a bipolar line driver
18	√		√		Serial Data In	Receives serial data at the rate of the ENCODER SHIFT CLOCK
19	√		√		Encoder Enable	A 'high' starts the encode cycle provided that the previous cycle is complete
20	√		√		Sync Select	A 'high' selects the command sync and a 'low' selects the data sync
21		√	√		Send Data	Provides an active 'high' to enable the external serial data source
22	√		√		Send Clock In	Clock input at 2 times the data rate
23	√		√		Encoder Clock	Input to the divide by 6 circuit
24	–	–	√	√	V_{DD}	Positive supply

Figure 4. Pin Designations

DC Characteristics and Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0.5	10	V
V_I	Input voltage	-0.3	V_{DD} + 0.3	V
T_A	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5: Absolute Maximum Ratings

Symbol	Parameter	Conditions	Total dose radiation not exceeding 3x105 Rad (Si)			Total dose ≤1 MRad (Si)		Units
			Min.	Typ.	Max.	Min.	Max.	
V_{DD}	Supply voltage		4.5	5.0	5.5	4.5	5.5	V
V_{IH2}	CMOS input high voltage		3.5			3.5		V
V_{IL2}	CMOS input low voltage				1.5		1.0	V
V_{OH2}	CMOS output high voltage	I_{OH} = -1mA	V_{DD}-0.4			V_{DD}-0.4		V
V_{OL2}	CMOS output low voltage	I_{OL} = 2.0mA			0.4		0.4	V
I_{IL}	Input low current				10		100	uA
I_{IH}	Input high current				-10		-100	uA
I_{DD}	Power supply current				2		10	mA
I_{DDYN}	Dynamic power supply current				10		20	mA

V_{DD} = 5V ± 10%, over full operating temperature range.

Figure 6: Electrical Characteristics

AC Characteristics

Symbol	Parameter	Min.	Max.	Units
f_{EC}	Encoder clock frequency	0	13	MHz
f_{ESC}	Send clock frequency	0	2.16	MHz
t_{ECR}	Encoder clock rise time	-	8	ns
t_{ECF}	Encoder clock fall time	-	8	ns
f_{ED}	Data rate	0	1.08	MHz
t_{MR}	Master reset pulse width	150	-	ns
t_{E1}	Shift clock delay	-	125	ns
t_{E2}	Serial data setup time	75	-	ns
t_{E3}	Serial data hold time	75	-	ns
t_{E4}	Enable setup time	90	-	ns
t_{E5}	Enable pulse width	80	-	ns
t_{E6}	Sync setup time	55	-	ns
t_{E7}	Sync pulse width	150	-	ns
t_{E8}	Send data delay	-	50	ns
t_{E9}	Bipolar output delay	-	130	ns

Notes:
1. V_{DD} = 5.0V ± 10%, over full operating temperature range.
2. C_L = 50pF

Figure 7. Encoder Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
f_{DC}	Decoder clock frequency	0	-	15	MHz
t_{DCR}	Decoder clock rise time	-	-	8	ns
t_{DCF}	Decoder clock fall time	-	-	8	ns
f_{DD}	Data rate	0	-	1.08	MHz
t_{DR}	Decoder reset pulse width	150	-	-	ns
t_{DRS}	Decoder reset setup time	75	-	-	ns
t_{MR}	Master reset pulse width	150	-	-	ns
t_{D1}	Bipolar data pulse width	t_{DC} + 10	-	-	ns
t_{D2}	Sync transition span	-	$18t_{DC}$	-	ns
t_{D3}	One-Zero overlap	-	-	t_{DC}-10	ns
t_{D4}	Short data transition span	-	$6t_{DC}$	-	ns
t_{D5}	Long data transition span	-	$12t_{DC}$	-	ns
t_{D6}	Sync delay (on)	-	-	110	ns
t_{D7}	Take data delay (on)	-	-	110	ns
t_{D8}	Serial data out delay	-	-	80	ns
t_{D9}	Sync delay (off)	-	-	110	ns
t_{D10}	Take data delay (off)	-	-	110	ns
t_{D11}	Valid word delay	-	-	110	ns

Notes:
1. V_{DD} = 5.0V ± 10%, over full operating temperature range.
2. C_L = 50pF
3. t_{DC} = Decoder clock period = $1/f_{DC}$

Figure 8. Decoder Electrical Characteristics

Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxiliary divide by six counter is provided on chip which can be utilised to produce the SEND CLOCK by dividing the DECODER CLOCK.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK ①. This cycle lasts for one word length or twenty ENCODER SHIFT CLOCK periods. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high at SYNC SELECT input actuates a command sync or a low will produce a data sync for that word ②. When the Encoder is ready to accept data, the SEND DATA output will go high and remain high for sixteen ENCODER SHIFT CLOCK periods ③. During these sixteen periods the data should be clocked into the SERIAL DATA input with every low-to-high transition of the ENCODER SHIFT CLOCK ③ - ④. After the sync and the Manchester II coded data are transmitted through the BIPOLAR ONE and BIPOLAR ZERO outputs, the Encoder adds on an additional bit which is the parity for that word ⑤. At any time a low in OUTPUT INHIBIT input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Anytime after or during this pulse, a low to high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.

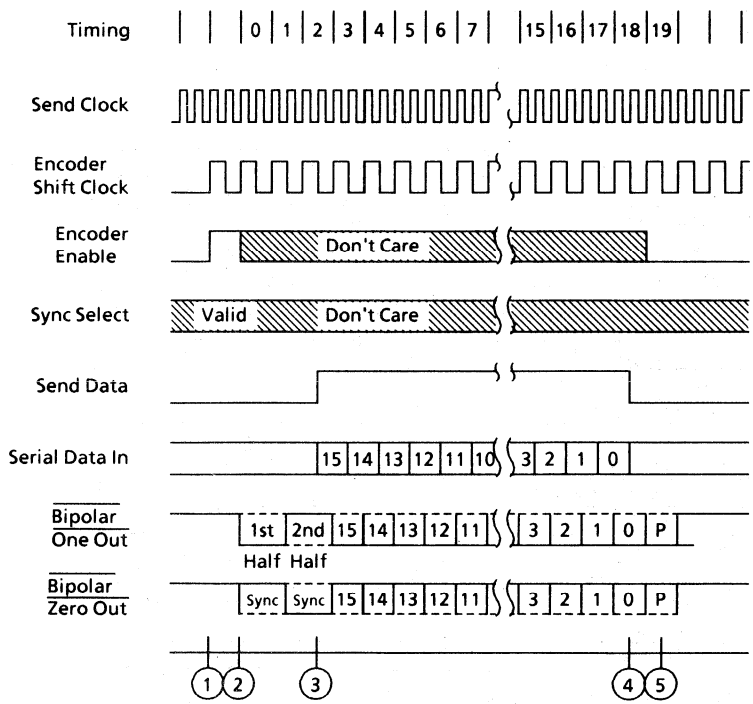


Figure 9. Encoder Operation

Decoder Operation

The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in MIL-STD-1553. The UNIPOLAR DATA input can only accept non-inverted Manchester II coded data (e.g. from $\overline{\text{BIPOLAR ZERO OUT}}$ of an Encoder).

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ①, the type of sync is indicated on COMMAND/$\overline{\text{DATA}}$ SYNC output. If the sync character was a command sync, this output will go high ② and remain high for sixteen DECODER SHIFT CLOCK periods ③, otherwise it will remain low. The TAKE DATA output will go high and remain high ② - ③ while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in a NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can get shifted into an external register on every low-to-high transition of this clock ② - ③.

After all sixteen decoded bits have been transmitted ③ the data is checked for odd parity. A high on VALID WORD output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence.

At any time in the above sequence, a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.

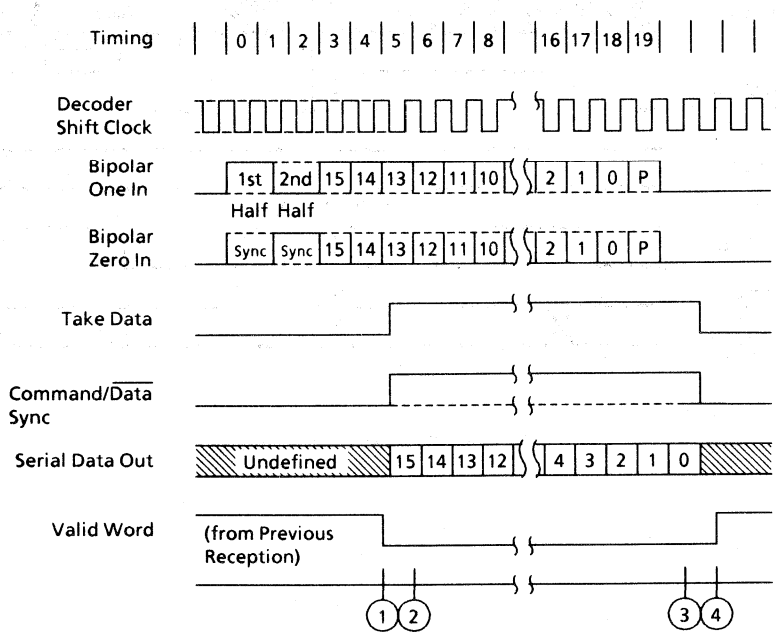


Figure 10. Decoder Operation

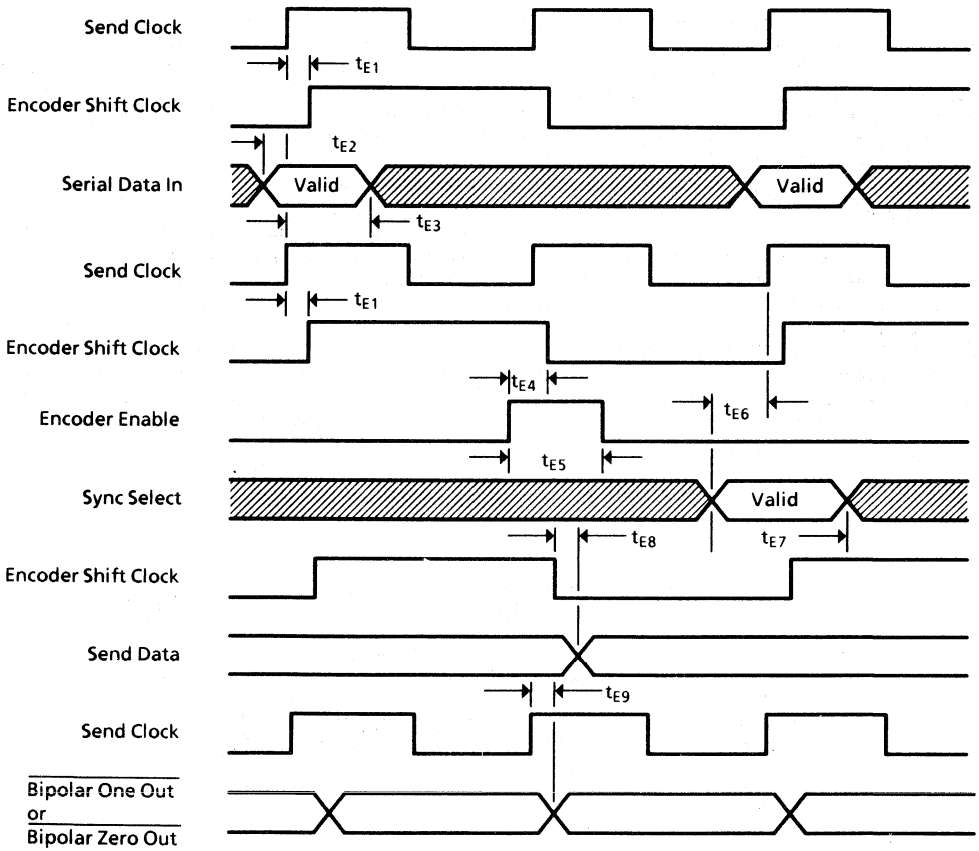
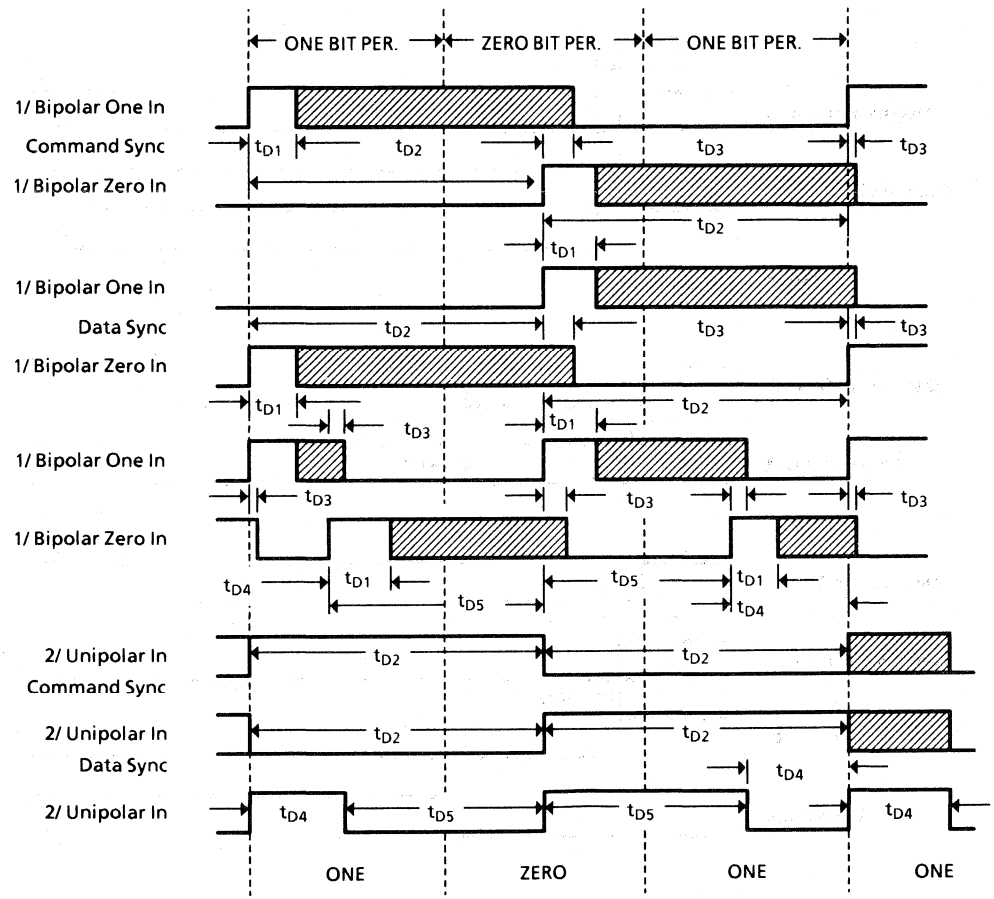


Figure 11. Encoder Timing Diagram



Notes:
1. Unipolar In = 0
2. Bipolar One In = 0
   Bipolar Zero In = 1

Figure 12. Decoder Timing Diagram

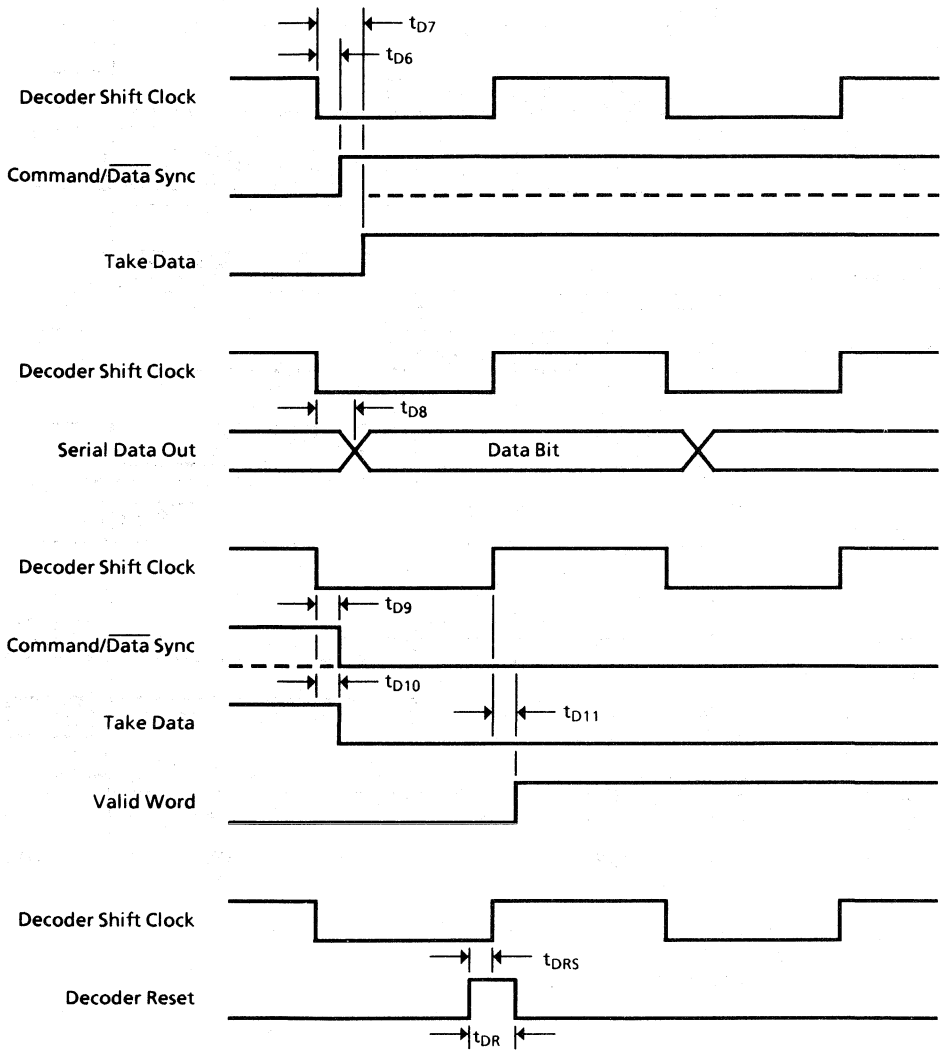


Figure 13. Decoder Timing Details

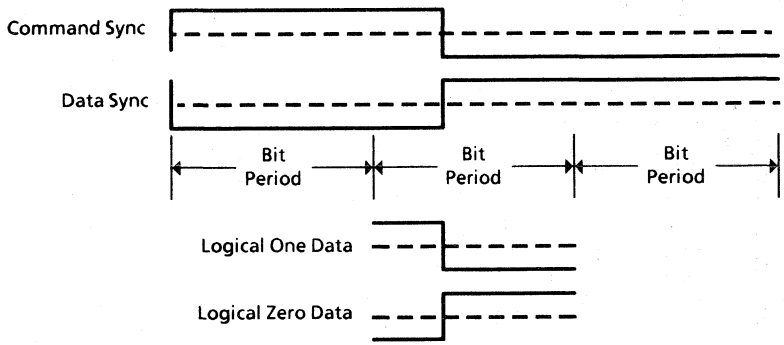


Figure 14. Character Formats

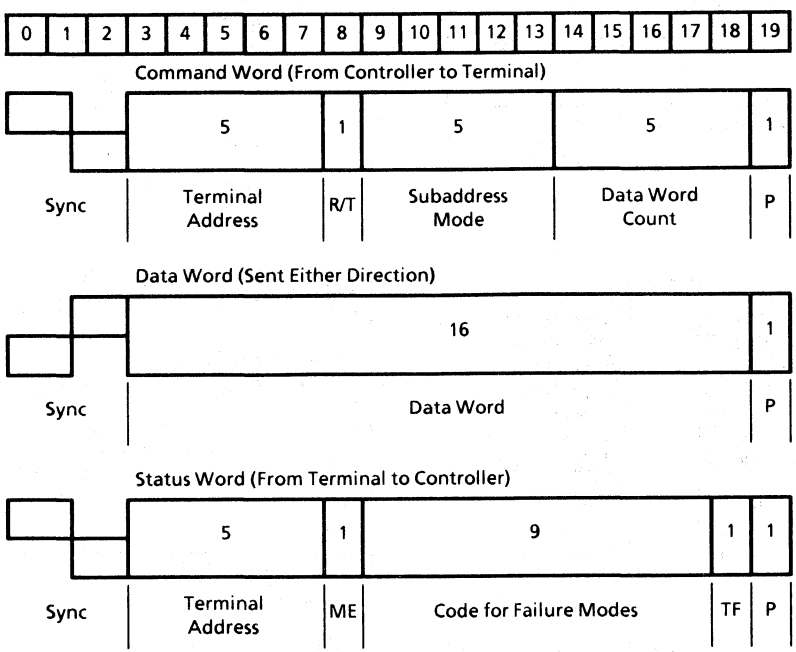
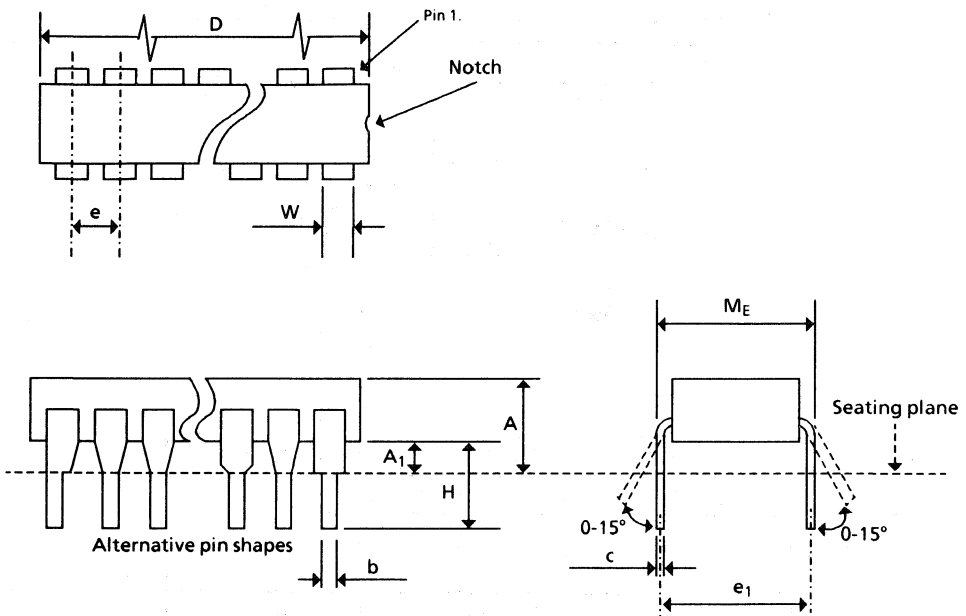
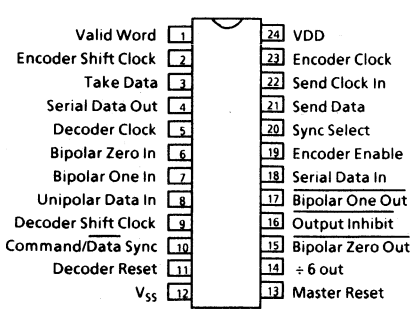


Figure 15. Word Formats

Outlines and Pin Assignments





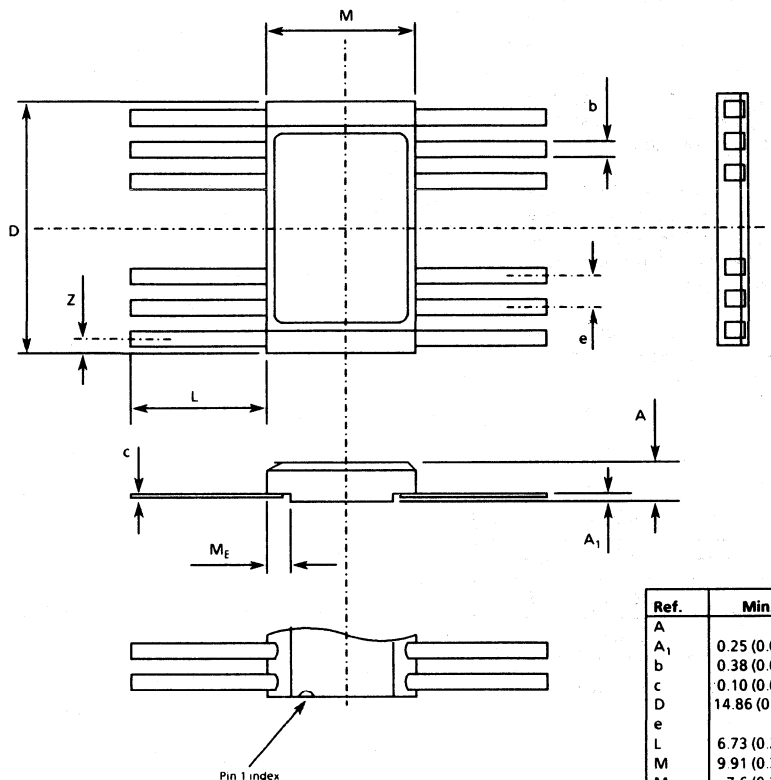
Ref.	Min.	Nom.	Max.
A	-	-	5.60 (0.220)
A_1	0.38 (0.015)	-	1.53 (0.060)
b	0.35 (0.014)	-	0.59 (0.023)
c	0.20 (0.008)	-	0.36 (0.014)
D	-	-	30.79 (1.212)
e	-	2.54(0.100) typ.	-
e_1	-	15.24(0.600) typ.	-
H	4.71 (0.185)	-	5.38 (0.212)
M_E	-	-	15.90 (0.626)
W	-	-	1.53 (0.060)

Dimensions in mm (inches)

MEDL XG403

Figure 16. 24-Lead Ceramic DIL (solder seal) - package style C

MAS15530
Radiation Hard Manchester Encoder - Decoder



Ref.	Min.	Nom.	Max.
A			2.67 (0.105)
A_1	0.25 (0.010)		1.02 (0.040)
b	0.38 (0.015)		0.48 (0.019)
c	0.10 (0.004)		0.18 (0.007)
D	14.86 (0.585)		15.62 (0.615)
e		2.54 (0.050)	
L	6.73 (0.265)		7.75 (0.305)
M	9.91 (0.390)		10.41 (0.410)
M_E	7.6 (0.30)		
Z	0.13 (0.005)		1.14 (0.045)
Dimensions in mm (inches)			

MEDL XG472

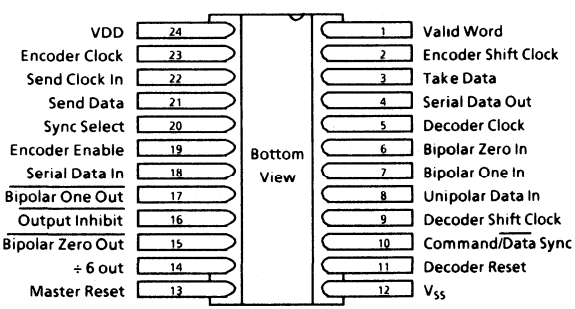


Figure 17. 24-lead Ceramic Flatpack (solder seal) - Package style F

RadiationTolerance

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

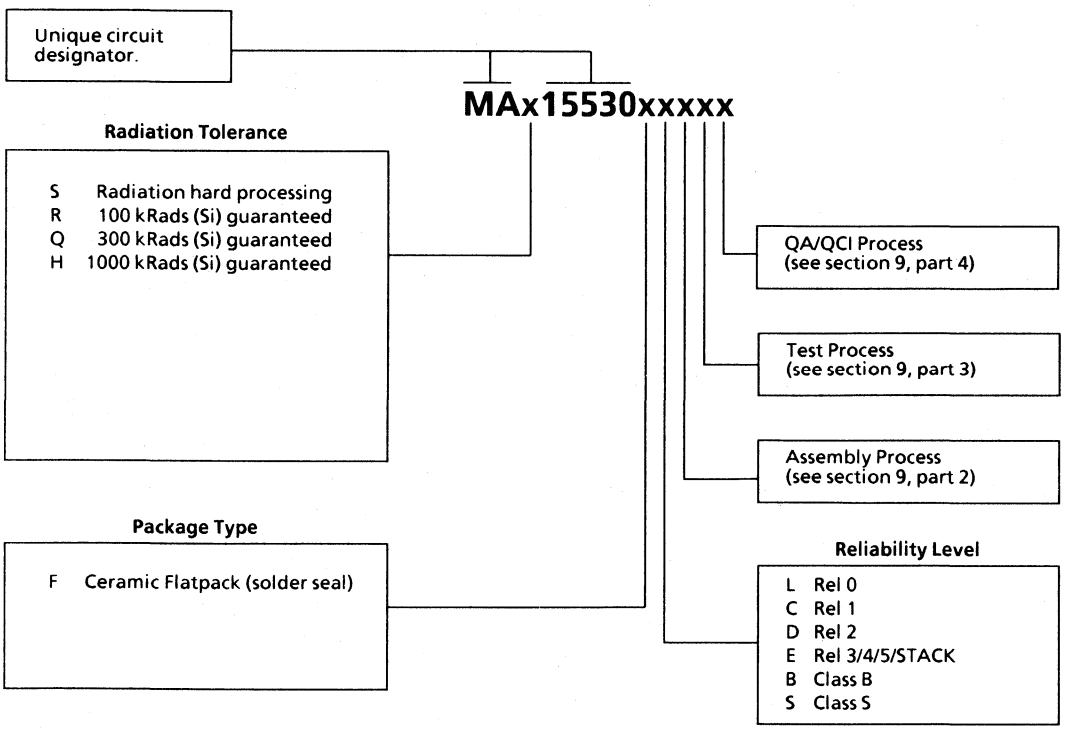
Total Dose (Function to specification)	$3x10^5$ Rad(Si)
Transient Upset (survivability)	$3x10^{10}$Rad(Si)/sec
Neutron Hardness (Function to specification)	$1x10^{15}$ neutrons/cm^2
Single Event Upset (GSO 10% worst case)	$<10^{-10}$ errors/bitday
Latch-up	Not possible

Figure 18. Radiation Hardness Parameters

MAS15530
Radiation Hard Manchester Encoder - Decoder

Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



section 7
LOGIC

GEC PLESSEY

SEMICONDUCTORS

S10505ASF Issue 1.2 November 1990

15HSC Series

Radiation Hard High Speed CMOS/SOS Logic

(Advanced Data)

Features

- **Radiation Hard to 1.5μm CMOS/SOS technology**
- **High SEU immunity**
- **Latch up free**
- **Low power CMOS/SOS technology**
- **Plug in replacement for 54/74LS, HC and HCT**
- **Dual in line, or flatpack packages**
- **High speed (toggle rate 100MHz)**

General Description

The 15HSC Series offer the conbined benefits of low power, high speed CMOS with the inherent latch up immunity, Single Event Upset (SEU) immunity and high level of radiation hardness of Marconis Silicon on Sapphire technology.

The 15HSC Series are pin compatible with the 54LS Series and the Marconi 54HSC Series CMOS/SOS devices with higher speed capability.

Further device types to those listed will be available shortly. Please contact Marconi for further information.

Device Types

15HSC138	3-Line to 8-Line Decoder/Multiplexer
15HSC163	Synchronous 4-Bit Counter

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Radiation Hard High Speed CMOS/SOS Logic
(Advanced Data)

DC Characteristics and Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0.5	10	V
V_I	Input voltage	-0.3	V_{DD} + 0.3	V
I	Current through any pin	-20	20	mA
T_A	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1: Absolute Maximum Ratings

Symbol	Parameter	Conditions	Total dose radiation not exceeding $3x10^5$ Rad (Si)			Total dose ≤1 MRad (Si)		Units
			Min.	Typ.	Max.	Min.	Max.	
V_{DD}	Supply voltage	-	4.5	5.0	5.5	4.5	5.5	V
V_{IH1}	HST input high voltage	-	2.0	-	-	2.0	-	V
V_{IL1}	HST input low voltage	-	-	-	0.8	-	0.3	V
V_{IH2}	HSC input high voltage	-	3.5	-	-	3.5	-	V
V_{IL2}	HSC input low voltage	-	-	-	1.5	-	1.0	V
V_{OH}	Output high voltage	$V_{IN} = V_{IH}$ or V_{IL} I_{OH} = -20uA I_{OH} = -6.0mA I_{OH} = -11.0mA	V_{DD} -0.1 3.7 2.5	-	-	V_{DD} -0.1 3.7 2.5	-	V V V
V_{OL}	Output low voltage	$V_{IN} = V_{IH}$ or V_{IL} I_{OL} = 20uA I_{OL} = 6.0mA I_{OL} = 9.0mA	-	-	0.1 0.2 0.4	-	0.1 0.2 0.4	V V V
I_{LI}	Input leakage current	$V_{IN} = V_{DD}$ or V_{SS} All inputs	-	-	± 10	-	± 10	µA
I_{LO}	Output leakage current	Outputs disabled $V_{OUT} = V_{DD}$ or V_{SS}	-	-	TBD	-	TBD	µA
I_{DD}	Quiescent current	$V_{IN} = V_{DD}$ Outputs unloaded	-	-	TBD	-	TBD	mA

V_{DD} = 5V ± 10%, over full operating temperature range.

Figure 2: Electrical Characteristics

15HSC138

3-Line to 8-Line Decoder/Multiplexer
(Advanced Data)

General Description

The 15HSC138 is a 3 to 8 line decoder/multiplexer.

Enable Inputs			Select Inputs			Outputs							
G_1	GN_{2A}	GN_{2B}	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = high level, L = low level, X = irrelevant

Figure 3: Function Table

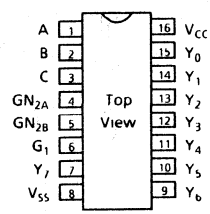

Figure 5: DIL Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		Units
		Spice Simulation	Max.	
t_{PLH}	Propagation delay. Address to Output.	7.6	15	ns
t_{PHL}	Propagation delay. Address to Output.	7.4	15	ns
t_{PLH}	Propagation delay. G to Output.	9.3	15	ns
t_{PHL}	Propagation delay. G to Output.	8.8	15	ns

V_{CC} = 5V, T_{MAX} = +125°C, C_L = 50pF

Figure 4: Switching Characteristics

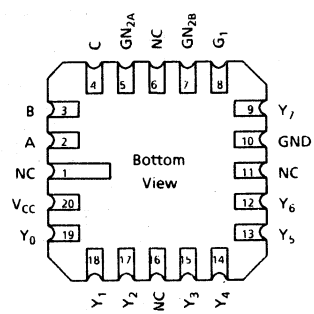

Figure 6: Flatpack Pin Out

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15HSC163

Synchronous 4-Bit Counter
(Advanced Data)

GEC PLESSEY
SEMICONDUCTORS

General Description

The 15HSC163 is a 4-bit counter with synchronous clear.

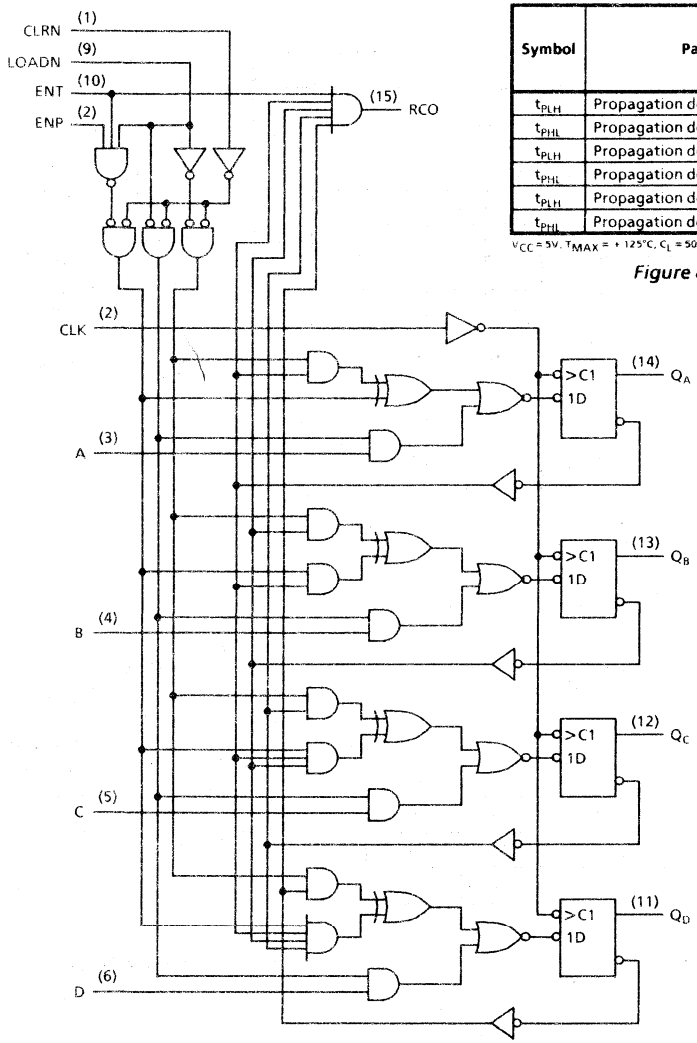


Figure 7: Logic Diagram

Symbol	Parameter	HSC (CMOS Comp.)		Units
		Spice Simulation	Max.	
t_{PLH}	Propagation delay Clock to RCO	11.5	15	ns
t_{PHL}	Propagation delay Clock to RCO	11.4	15	ns
t_{PLH}	Propagation delay Clock to any Q	9.4	15	ns
t_{PHL}	Propagation delay Clock to any Q	9.6	15	ns
t_{PLH}	Propagation delay ENT to RCO	8.5	15	ns
t_{PHL}	Propagation delay ENT to RCO	8.4	15	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 8: Switching Characteristics

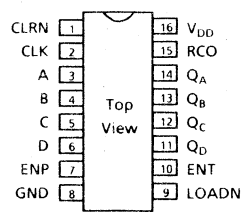


Figure 9: DIL Pin Out

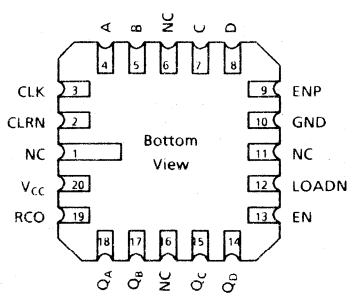
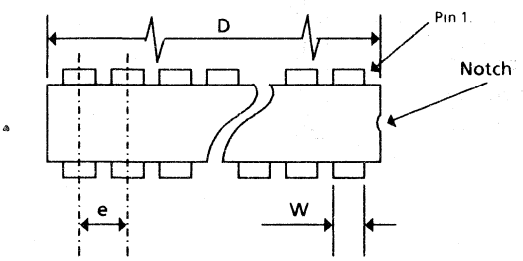


Figure 10: Flatpack Pin Out

15HSC Series

Radiation Hard
High Speed CMOS/SOS Logic
(Advanced Data)



Ref.	Min.	Nom.	Max.
A			5.60 (0.220)
A_1	0.38 (0.015)		1.53 (0.060)
b	0.35 (0.014)		0.59 (0.023)
c	0.20 (0.008)		0.36 (0.014)
D			20.58 (0.810)
e		2.54 (0.100) typ	
e_1		7.62 (0.300) typ	
H	4.45 (0.175)		5.38 (0.212)
M_E			8.30 (0.326)
W			1.53 (0.060)
Dimensions in mm (inches)			

MEDL XG402

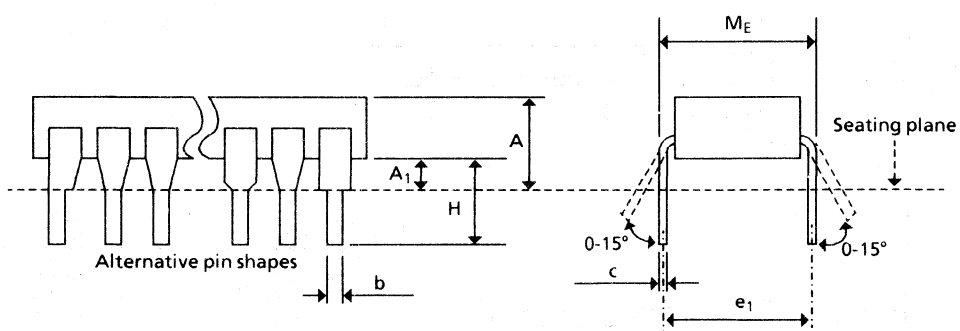
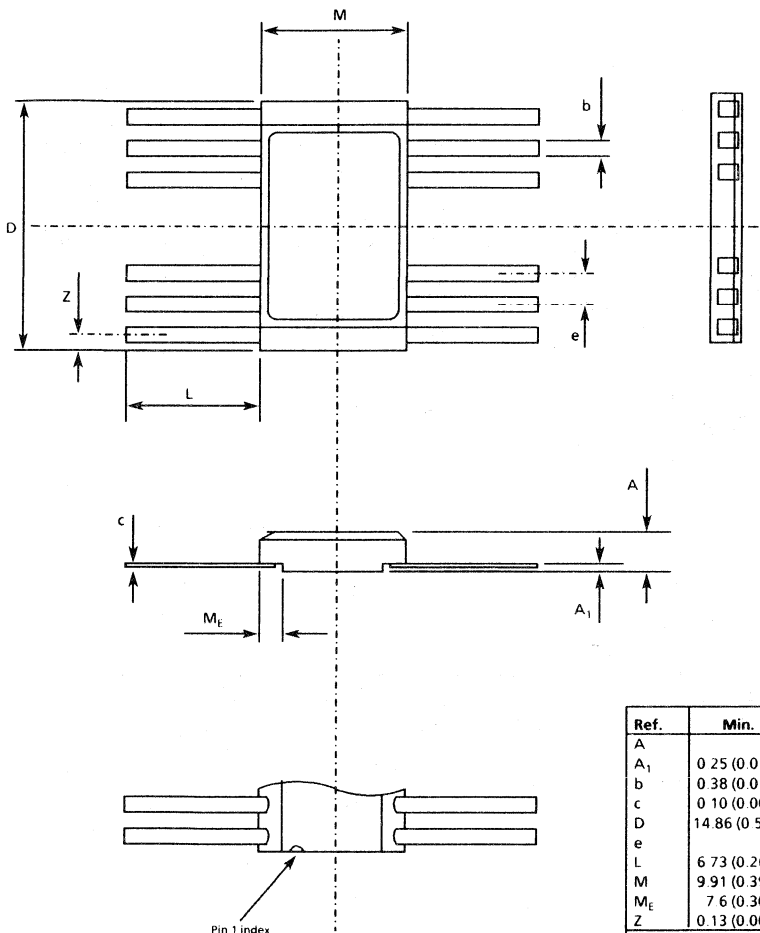


Figure 11: 16-Lead Ceramic DIL (solder seal) - package style C

7

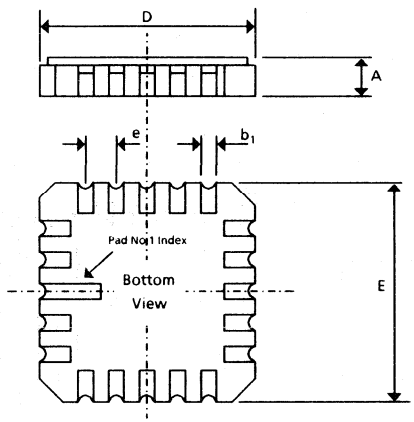


Ref.	Min.	Nom.	Max.
A			2.67 (0.105)
A_1	0.25 (0.010)		1.02 (0.040)
b	0.38 (0.015)		0.48 (0.019)
c	0.10 (0.004)		0.18 (0.007)
D	14.86 (0.585)		15.62 (0.615)
e		2.54 (0.050)	
L	6.73 (0.265)		7.75 (0.305)
M	9.91 (0.390)		10.41 (0.410)
M_E	7.6 (0.30)		
Z	0.13 (0.005)		1.14 (0.045)

Dimensions in mm (inches)

MEDL XG496

Figure 12: 16-lead Ceramic Flatpack (solder seal) - Package style F



Ref.	Min.	Nom.	Max.
A			1.96 (0.077)
b_1		0.64 (0.025)	
D			8.89 (0.350)
E			8.89 (0.350)
e		1.27 (0.050)	
Dimensions in mm (inches)			

MEDL XG431

Figure 13: 44-pad Leadless Chip Carrier (Package style L)

15HSC Series

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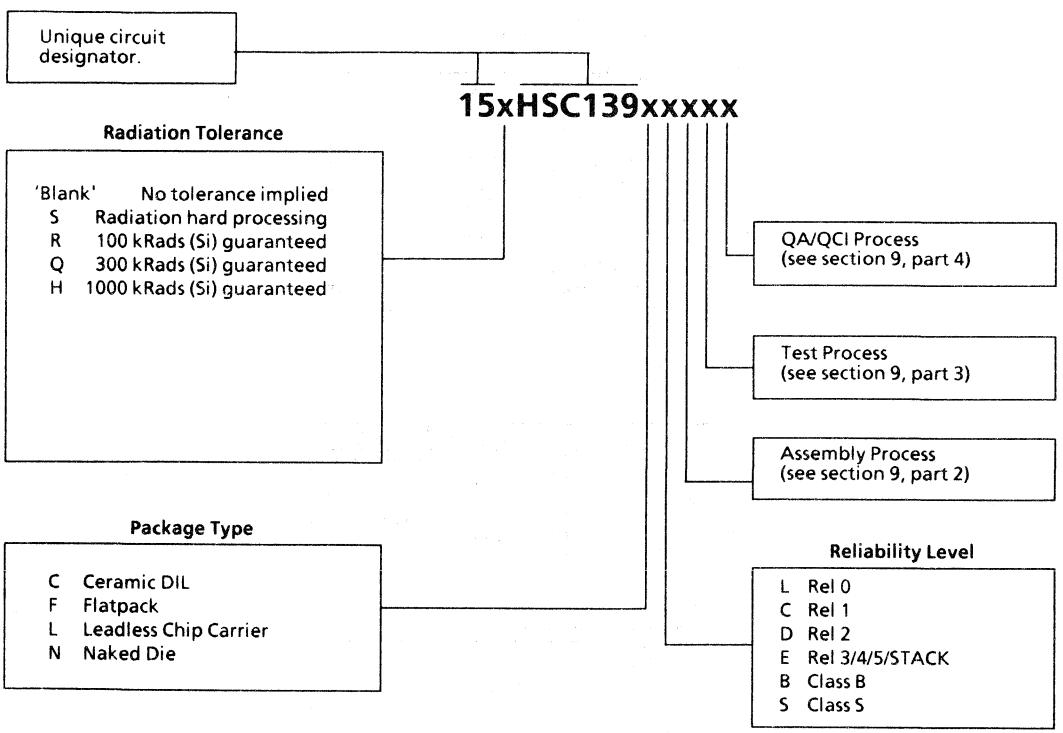
Radiation Hard
High Speed CMOS/SOS Logic
(Advanced Data)

Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



GEC PLESSEY

SEMICONDUCTORS

S10504FSF Issue 1.4 November 1990

54HSC/T Series

Radiation Hard High Speed CMOS/SOS Logic

Features

- **Radiation Hard to 1 MRad (Si)**
- **High SEU immunity, latch up free**
- **Low power CMOS/SOS technology**
- **Plug in replacement for 54/74LS, HC and HCT**
- **Dual in line or flatpack packages**

General Description

The CMOS/SOS HSC/T Series offer the combined benefits of low power, high speed CMOS with the inherent latch up immunity, Single Event Upset (SEU) immunity and the high level of radiation hardness of Silicon on Sapphire technology. The 54HSC/T series of circuits are pin for pin compatible with the 54LS series range.

HSC and HST devices have CMOS and TTL compatible inputs/outputs respectively.

Further variants to those listed will be available shortly.

Gates and Buffers

54HSC/T00	Quadruple 2-input positive NAND gates
54HSC/T02	Quadruple 2-input positive NOR gates
54HSC/T04	Hex inverters
54HSC/T08	Quadruple 2-input positive AND gates
54HSC/T10	Triple 3-input positive NAND gates
54HSC/T14	Hex schmitt-trigger inverters
54HSC/T21	Dual 4-input positive AND gates
54HSC/T27	Triple 3-input positive NOR gates
54HSC/T32	Quadruple 2-input positive OR gates
54HSC/T86	Quadruple 2-input EXCLUSIVE-OR gates
54HSC/T125	Quadruple bus buffer gates with tri-state outputs (Active low enable)
54HSC/T126	Quadruple bus buffer gates with tri-state outputs (Active high enable)

Flip-Flops

54HSC/T74	Dual D-type flip-flops with preset and clear
54HSC/T109	Dual J-KB flip-flop with preset and clear
54HSC/T273	Octal D-type flip-flops
54HSC/T374	Octal D-type edge triggered flip-flops
54HSC/T574	Octal D-type edge triggered flip-flops

Adders

54HSC/T283	4-bit binary full adders with fast carry

Counters

54HSC/T161	4-bit synchronous binary counter
54HSC/T163	Synchronous 4-bit counter

Decoders/Demultiplexers

54HSC/T138	3-line to 8-line decoder/multiplexer
54HSC/T139	Dual 2 to 4 decoders/multiplexers
54HSC/T148	8-line to 3-line octal priority encoders
54HSC/T151	1 of 8 data selectors/multiplexers
54HSC/T154	4 to 16 line decoders/demultiplexers
54HSC/T157	Quad 2-line to 1-line data selectors/multiplexers
54HSC/T238	3 to 8 decoder/demultiplexer
54HSC/T253	Dual 4 to 1 data selectors/multiplexers

Registers

54HSC/T164	8-bit parallel output serial shift register
54HSC/T165	Parallel load 8-bit shift register
54HSC/T166	8-bit shift register

Comparators

54HSC/T521	8-bit magnitude comparator

Line Drivers

54HSC/T240	Octal 3-state driver inverting
54HSC/T241	Octal 3-state driver complementary enable
54HSC/T244	Octal 3-state driver
54HSC/T540	Octal 3-state driver/buffer inverting
54HSC/T541	Octal 3-state driver/buffer

Transceivers

54HSC/T245	Octal bus transceiver

Latches

54HSC/T373	Octal transparent latch, 3-state outputs
54HSC/T573	Octal transparent latch, 3-state outputs

Miscellaneous

54HSC/T630*	EDAC (Error Detection And Correction)
54HSC/T670	4 x 4 register files with tri-state outputs

* Separate Data Sheet Available

7

DC Characteristics and Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0.5	10	V
V_I	Input voltage	-0.3	V_{DD} + 0.3	V
I	Current through any pin	-20	20	mA
T_A	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1: Absolute Maximum Ratings

Symbol	Parameter	Conditions	Total dose radiation not exceeding 3x10^5 Rad (Si)			Total dose ≤1 MRad (Si)		Units
			Min.	Typ.	Max.	Min.	Max.	
V_{DD}	Supply voltage		4.5	5.0	5.5	4.5	5.5	V
V_{IH1}	HST input high voltage		2.0			2.0		V
V_{IL1}	HST input low voltage				0.8		0.3	V
V_{IH2}	HSC input high voltage		3.5			3.5		V
V_{IL2}	HSC input low voltage				1.5		1.0	V
V_{OH}	Output high voltage	$V_{IN} = V_{IH}$ or V_{IL} I_{OH} = -20uA I_{OH} = -6.0mA I_{OH} = -11.0mA	V_{DD} -0.1 3.7 2.5			V_{DD} -0.1 3.7 2.5		V V V
V_{OL}	Output low voltage	$V_{IN} = V_{IH}$ or V_{IL} I_{OL} = 20uA I_{OL} = 6.0mA I_{OL} = 9.0mA			0.1 0.2 0.4		0.1 0.2 0.4	V V V
I_{LI}	Input leakage current	$V_{IN} = V_{DD}$ or V_{SS} All inputs			± 10		± 10	uA
I_{LO}	Output leakage current	Outputs disabled $V_{OUT} = V_{DD}$ or V_{SS}			± 90		± 90	uA
I_{DD}	Quiescent current	$V_{IN} = V_{DD}$ Outputs unloaded			600		4	uA

V_{DD} = 5V ± 10%, over full operating temperature range.

Figure 2: Electrical Characteristics

54HSC/T00

Quadruple 2-Input Positive-NAND Gates

General Description

The 54HSC/T00 is a quadruple 2-Input Positive-NAND gate.

Inputs		Outputs
A	B	
L	L	H
L	H	H
H	L	H
H	H	L

H = high level, L = low level

Figure 1: Function Table

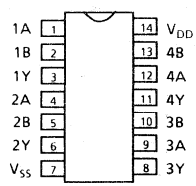


Figure 3: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	15	25	18	28	ns
t_{PHL}	Propagation delay time, high to low level output	14	25	17	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 4: Switching Characteristics

7

54HSC/T02

Quadruple 2-Input Positive-NOR Gates

GEC PLESSEY

SEMICONDUCTORS

General Description

The 54HSC/T02 is a quadruple 2-Input Positive-NOR gate.

Inputs		Outputs
A	B	
L	L	H
L	H	L
H	L	L
H	H	L

H = high level, L = low level

Figure 1: Function Table

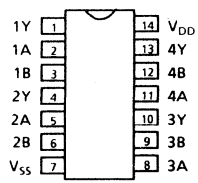


Figure 3: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	15	25	18	28	ns
t_{PHL}	Propagation delay time, high to low level output	14	25	17	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 4: Switching Characteristics

54HSC/T04
Hex Inverters

General Description

The 54HSC/T04 consists of six Hex Inverters.

Inputs	Outputs
A	
H	L
L	H

H = high level, L = low level

Figure 1: Function Table

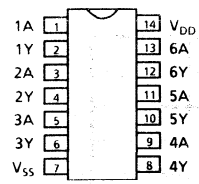


Figure 3: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	10	25	13	28	ns
t_{PHL}	Propagation delay time, high to low level output	11	25	14	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 4: Switching Characteristics

7

54HSC/T08

Quadruple 2-Input Positive-AND Gates

GEC PLESSEY
SEMICONDUCTORS

General Description

The 54HSC/T08 is a quadruple 2-Input Positive-AND gate.

Inputs		Outputs
A	B	
L	L	L
L	H	L
H	L	L
H	H	H

H = high level, L = low level

Figure 1: Function Table

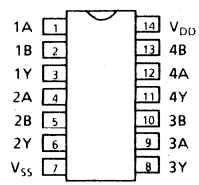


Figure 3: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	15	25	18	28	ns
t_{PHL}	Propagation delay time, high to low level output	16	25	19	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 4: Switching Characteristics

54HSC/T10

Triple 3-Input Positive-NAND Gates

General Description

The 54HSC/T10 is a Triple 3-Input Positive-NAND gate.

Inputs			Outputs
A	B	C	
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

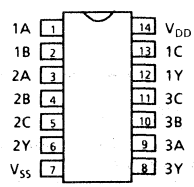


Figure 3: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	14	25	17	28	ns
t_{PHL}	Propagation delay time, high to low level output	15	25	18	28	ns

V_{CC} = 5V, T_{MAX} = +125°C, C_L = 50pF

Figure 4: Switching Characteristics

54HSC/T14

Hex Schmitt-Trigger Inverters

GEC PLESSEY
SEMICONDUCTORS

General Description

The 54HSC/T14 consists of six Schmitt-Trigger Inverters.

Inputs	Outputs
A	
L	H
H	L

H = high level, L = low level

Figure 1: Function Table

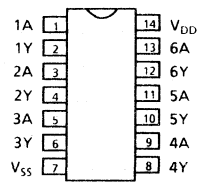


Figure 3: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	14	25	17	28	ns
t_{PHL}	Propagation delay time, high to low level output	15	25	18	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 4: Switching Characteristics

54HSC/T21

Dual 4-Input Positive-AND Gates

General Description

The 54HSC/T21 is a Dual 4-Input Positive-AND gate.

Inputs				Outputs
A	B	C	D	
L	L	L	L	L
L	L	L	H	L
L	L	H	L	L
L	L	H	H	L
L	H	L	L	L
L	H	L	H	L
L	H	H	L	L
L	H	H	H	L
H	L	L	L	L
H	L	L	H	L
H	L	H	L	L
H	L	H	H	L
H	H	L	L	L
H	H	L	H	L
H	H	H	L	L
H	H	H	H	H

H = high level, L = low level

Figure 1: Function Table

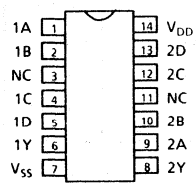


Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	12	25	15	28	ns
t_{PHL}	Propagation delay time, high to low level output	13	25	16	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 4: Switching Characteristics

7

54HSC/T27

Triple 3-Input Positive-NOR Gates

GEC PLESSEY
SEMICONDUCTORS

General Description

The 54HSC/T27 is a Triple 3-Input Positive-NOR gate.

Inputs			Outputs
A	B	C	
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	L

H = high level, L = low level

Figure 1: Function Table

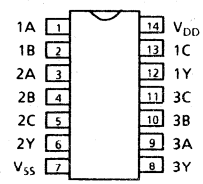


Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	10	25	12	28	ns
t_{PHL}	Propagation delay time, high to low level output	11	25	13	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 4: Switching Characteristics

54HSC/T32

Quadruple 2-Input Positive-OR Gates

General Description

The 54HSC/T32 is a Quadruple 2-Input Positive-OR gate.

Inputs		Outputs
A	B	
L	L	L
L	H	H
H	L	H
H	H	H

H = high level, L = low level

Figure 1: Function Table

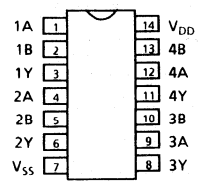


Figure 3: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	15	25	18	28	ns
t_{PHL}	Propagation delay time, high to low level output	16	25	19	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 4: Switching Characteristics

7

54HSC/T86

Quadruple 2-Input EXCLUSIVE-OR Gates

GEC PLESSEY
SEMICONDUCTORS

General Description

The 54HSC/T86 is a Quadruple 2-Input EXCLUSIVE-OR gate.

Inputs		Outputs
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

Figure 1: Function Table

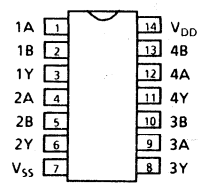


Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	14	25	17	28	ns
t_{PHL}	Propagation delay time, high to low level output	15	25	18	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

54HSC/T125

Quadruple Bus Buffer Gates with Tri-State Outputs (Active Low Enable)

General Description

The 54HSC/T125 is a Quadruple Bus Buffer Gate. When G is low the A-input is transferred to the Y-output. When G is high the output is in a high impedance state.

Inputs		Outputs
$\overline{G}$	A	Y
L	L	L
L	H	H
H	L	Z
H	H	Z

H = high level, L = low level, Z = high impedance

Figure 1: Function Table

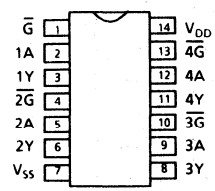


Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay A to Y	15	25	18	28	ns
t_{PHL}	Propagation delay A to Y	15	25	18	28	ns
t_{PZH}	Propagation delay G to Y	12	25	15	28	ns
t_{PZL}	Propagation delay G to Y	12	25	15	28	ns
t_{PHZ}	Propagation delay Y to Tri-State	12	25	15	28	ns
t_{PLZ}	Propagation delay Y to Tri-State	12	25	15	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

7

54HSC/T126

Quadruple Bus Buffer Gates with Tri-State Outputs (Active High Enable)

GEC PLESSEY
SEMICONDUCTORS

General Description

The 54HSC/T126 is a Quadruple Bus Buffer Gate. When G is high the A-input is transferred to the Y-output. When G is low the output is in a high impedance state.

Inputs		Outputs
G	A	Y
H	L	L
H	H	H
L	L	Z
L	H	Z

H = high level, L = low level, Z = high impedance

Figure 1: Function Table

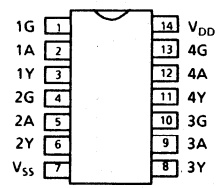


Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay A to Y	?	25	?	28	ns
t_{PHL}	Propagation delay A to Y	?	25	?	28	ns
t_{PZH}	Propagation delay G to Y	?	25	?	28	ns
t_{PZL}	Propagation delay G to Y	?	25	?	28	ns
t_{PHZ}	Propagation delay Y to Tri-State	?	25	?	28	ns
t_{PLZ}	Propagation delay Y to Tri-State	?	25	?	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

Typical timings not available at time of print, contact Marketing.

54HSC/T74

Dual D-Type Flip-Flops with Preset and Clear

General Description

The 54HSC/T74 is a Dual D-Type Flip-Flop. The D inputs are transferred to the Q outputs on the positive going edge of the clock pulse. The clear is active low.

Inputs				Outputs	
$\overline{\text{PRESET}}$	$\overline{\text{CLEAR}}$	CLOCK	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	L-H	H	H	L
H	H	L-H	L	L	H
H	H	L	X	Q_0	$\overline{Q_0}$

H = high level, L = low level, X = irrelevant, * = unknown return state

Figure 1: Function Table

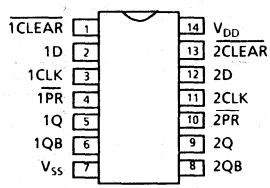


Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay. Preset to Q or QB.	15	25	18	28	ns
t_{PHL}	Propagation delay. Preset to Q or QB.	16	25	19	28	ns
t_{PLH}	Propagation delay. Clear to Q or QB.	18	25	21	28	ns
t_{PHL}	Propagation delay. Clear to Q or QB.	15	25	18	28	ns
t_{PLH}	Propagation delay. Clock to Q or QB.	17	25	20	28	ns
t_{PHL}	Propagation delay. Clock to Q or QB.	18	25	21	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

7

54HSC/T109

Dual J-KB Flip-Flops with Preset and Clear

GEC PLESSEY
SEMICONDUCTORS

General Description

The 54HSC/T109 is a Dual Positive-Edge-Triggered J-KB Flip-Flop with preset and clear.

Inputs					Outputs	
$\overline{PRESET}$	$\overline{CLEAR}$	CLOCK	J	KB	Q	QB
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	Toggle
H	H	↑	L	H	Q_0	QB_0
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	QB_0

H = high level, L = low level, X = irrelevant, * Unknown return state

Figure 1: Function Table

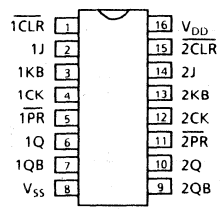


Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay. Preset to Q or QB.	15	25	18	28	ns
t_{PHL}	Propagation delay. Preset to Q or QB.	16	25	19	28	ns
t_{PLH}	Propagation delay. Clear to Q or QB.	17	25	20	28	ns
t_{PHL}	Propagation delay. Clear to Q or QB.	15	25	18	28	ns
t_{PLH}	Propagation delay. Clock to Q or QB.	18	25	21	28	ns
t_{PHL}	Propagation delay. Clock to Q or QB.	15	25	18	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

54HSC/T273
Octal D-Type Flip-Flops

General Description

The 54HSC/T273 is an Octal D-Type Flip-Flop with a direct active low clear. The D-Inputs are transferred to the Q-Outputs on the positive going edge of the clock pulse.

Inputs			Outputs
$\overline{\text{Clear}}$	Clock	D	Q
L	X	X	L
H	L-H	H	H
H	L-H	L	L
H	L	X	Q_0

Q_0 = level of Q before inputs were established
H = high level, L = low level, X = irrelevant

Figure 1: Function Table

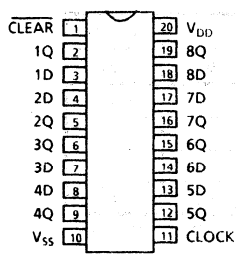


Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay Clock to Q or QB	15	25	18	28	ns
t_{PHL}	Propagation delay Clock to Q or QB	17	25	20	28	ns
t_{PLH}	Propagation delay Clear to Q or QB	14	25	17	28	ns
t_{PHL}	Propagation delay Clear to Q or QB	16	25	19	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

7

54HSC/T374

Octal D-Type Edge-Triggered Flip-Flops

GEC PLESSEY
SEMICONDUCTORS

General Description

The 54HSC/T374 consists of 8 Positive-Edge Triggered D-Type Flip-Flops with tri-state outputs.

Inputs			Outputs
$\overline{OC}$	Clock	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level, X = irrelevant, Z = high impedance

Figure 1: Function Table

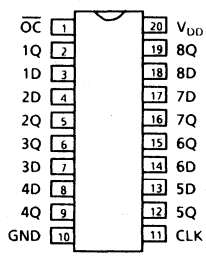


Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)			HST (TTL Comp.)			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH}	Propagation delay low to high output	-	16	25	-	19	28	ns
t_{PHL}	Propagation delay high to low output	-	19	27	-	22	30	ns
t_{PZL}	Propagation delay Enable to low	-	13	21	-	16	24	ns
t_{PZH}	Propagation delay Enable to high	-	16	24	-	19	27	ns
t_{PLZ}	Propagation delay Disable from low	-	14	22	-	17	25	ns
t_{PHZ}	Propagation delay Disable from high	-	13	21	-	16	24	ns
t_{SU}	Propagation delay Set Up Time	15	-	-	18	-	-	ns
t_U	Propagation delay Hold Time	0	-	-	0	-	-	ns
t_W	Propagation delay Min. Pulse Width	15	-	-	18	-	-	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

54HSC/T574

Octal D-Type Edge-Triggered Flip-Flops

General Description

The 54HSC/T574 consists of 8 Positive-Edge Triggered D-Type Flip-Flops with tri-state outputs.

Inputs			Outputs
$\overline{OC}$	Clock	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level, X = irrelevant, Z = high impedance

Figure 1: Function Table

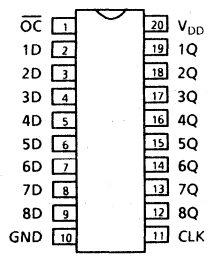


Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)			HST (TTL Comp.)			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH}	Propagation delay low to high output	-	16	25	-	19	28	ns
t_{PHL}	Propagation delay high to low output	-	19	27	-	22	30	ns
t_{PZL}	Propagation delay Enable to low	-	13	21	-	16	24	ns
t_{PZH}	Propagation delay Enable to high	-	16	24	-	19	27	ns
t_{PLZ}	Propagation delay Disable from low	-	14	22	-	17	25	ns
t_{PHZ}	Propagation delay Disable from high	-	13	21	-	16	24	ns
t_{SU}	Propagation delay Set Up Time	15	-	-	18	-	-	ns
t_U	Propagation delay Hold Time	0	-	-	0	-	-	ns
t_W	Propagation delay Min. Pulse Width	15	-	-	18	-	-	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

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54HSC/T283

4-Bit Binary Full Adders with Fast Carry

GEC PLESSEY
SEMICONDUCTORS

General Description

The 54HSC/T283 are 4-Bit Binary Full Adders with fast carry.

Inputs				Output					
				When C0 = L / When C2 = L			When C0 = H / When C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = high level, L = low level

Figure 1: Function Table

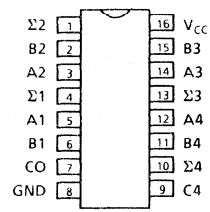

Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay C0 to any Σ	?	25	?	28	ns
t_{PHL}	Propagation delay C0 to any Σ	?	25	?	28	ns
t_{PLH}	Propagation delay Ai or Bi to Σi	?	25	?	28	ns
t_{PHL}	Propagation delay Ai or Bi to Σi	?	25	?	28	ns
t_{PLH}	Propagation delay C0 to C4	?	25	?	28	ns
t_{PHL}	Propagation delay C0 to C4	?	25	?	28	ns
t_{PLH}	Propagation delay Ai or Bi to C4	?	25	?	28	ns
t_{PHL}	Propagation delay Ai or Bi to C4	?	25	?	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

54HSC/T161

4-Bit Synchronous Binary Counter

General Description

The 54HSC/T161 is a Synchronous 4-Bit Binary Counter which features direct clear and an internal carry look-ahead.

Inputs						Output
$\overline{\text{Clear}}$	Enable P	Enable T	A→D	$\overline{\text{Load}}$	Clock	$Q_A \rightarrow Q_D$
L	X	X	X	X	X	0
H	L	X	X	H	X	Inhibit
H	X	L	X	H	X	Inhibit
H	X	X	Q_n	L	↑	Q_n
H	X	X	X	X	L	Q_0
H	X	X	X	X	H	Q_0
H	H	H	X	H	↑	Count

CARRY = H when $Q_A \rightarrow Q_D$ = H, Q_0 = Previous level of Q
H = high level, L = low level, X = irrelevant

Figure 1: Function Table

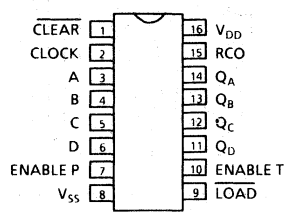

Figure 2: Pin Out

Symbol	From (Input)	To (Output)	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
			Typ.	Max.	Typ.	Max.	
t_{PLH}	CLOCK	RIPPLE CARRY	20	25	23	28	ns
t_{PHL}	CLOCK	RIPPLE CARRY	19	25	22	28	ns
t_{PLH}	CLOCK (Load Input HIGH)	Any Q Output	16	25	19	28	ns
t_{PHL}	CLOCK (Load Input HIGH)	Any Q Output	15	25	18	28	ns
t_{PLH}	CLOCK (Load Input LOW)	Any Q Output	15	25	18	28	ns
t_{PHL}	CLOCK (Load Input LOW)	Any Q Output	15	25	18	28	ns
t_{PLH}	ENABLE	RIPPLE CARRY	14	25	17	28	ns
t_{PHL}	ENABLE	RIPPLE CARRY	14	25	17	28	ns
t_{PHL}	CLEAR	Any Q Output	18	25	21	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

54HSC/T163
Synchronous 4-Bit Counter

GEC PLESSEY
SEMICONDUCTORS

General Description

The 54HSC/T163 is a 4-Bit Counter with synchronous clear.

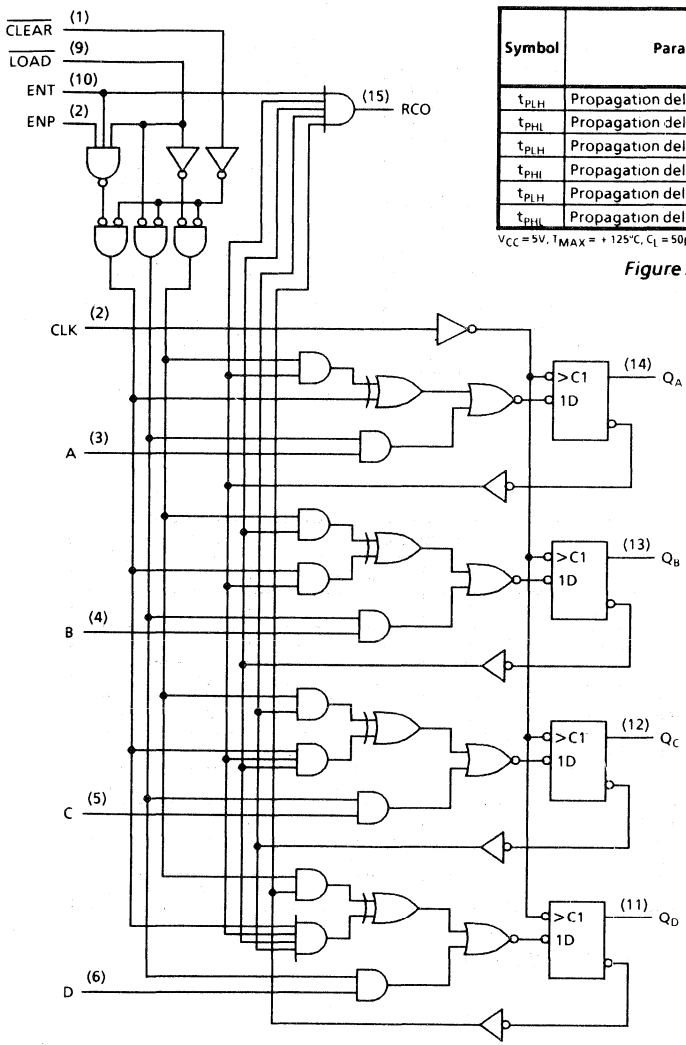

Figure 1: Logic Diagram

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay Clock to RCO	25	30	28	33	ns
t_{PHL}	Propagation delay Clock to RCO	18	25	21	28	ns
t_{PLH}	Propagation delay Clock to any Q	25	30	28	33	ns
t_{PHL}	Propagation delay Clock to any Q	18	25	21	28	ns
t_{PLH}	Propagation delay ENT to RCO	18	25	21	28	ns
t_{PHL}	Propagation delay ENT to RCO	15	25	18	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 2: Switching Characteristics

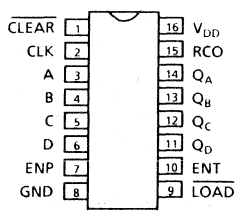

Figure 3: Pin Out

54HSC/T138

3-Line to 8-Line Decoder/Multiplexer

General Description

The 54HSC/T138 is a 3-Line to 8-Line Decoder/Multiplexer, with inverted outputs.

Enable Inputs			Select Inputs			Outputs							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

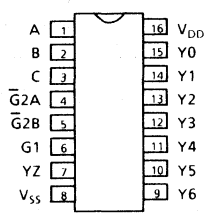

Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay Address to Output	17	25	20	28	ns
t_{PHL}	Propagation delay Address to Output	19	25	22	28	ns
t_{PLH}	Propagation delay G to Output	21	25	24	28	ns
t_{PHL}	Propagation delay G to Output	21	25	24	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pf

Figure 3: Switching Characteristics

54HSC/T139

Dual 2 to 4 Decoders/Multiplexers

GEC PLESSEY
SEMICONDUCTORS

General Description

The 54HSC/T139 consists of Two Independent 2 to 4 Line Decoders/Demultiplexers.

Inputs			Outputs			
Enable	Select					
$\overline{G}$	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

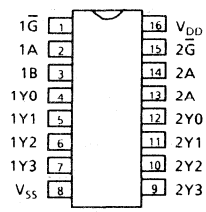

Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay Address to Output	16	25	19	28	ns
t_{PHL}	Propagation delay Address to Output	17	25	20	28	ns
t_{PLH}	Propagation delay G to Output	16	25	19	28	ns
t_{PHL}	Propagation delay G to Output	17	25	20	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

54HSC/T148

8-Line to 3-Line Octal Priority Encoders

General Description

The 54HSC/T148 is an 8 to 3 Line Priority Encoder. Data inputs and outputs are active at the low logic level. Data is accepted on the eight priority inputs (I0-I7). The binary code, corresponding to the highest priority input which is low, is generated on the address outputs (A0-A2) if the enable input is high.

The group select (GS) is low when one or more priority inputs and the enable input (EI) are low. The enable output (EO) is low when all priority inputs are high and the enable is low. When the enable input is high all outputs are high.

Inputs									Outputs				
EI	I0	I1	I2	I3	I4	I5	I6	I7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

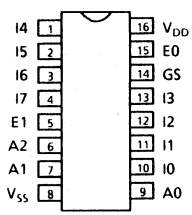

Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay EI to A	14	25	17	28	ns
t_{PHL}	Propagation delay EI to A	15	25	18	28	ns
t_{PLH}	Propagation delay EI to GS	15	25	18	28	ns
t_{PHL}	Propagation delay EI to GS	15	25	18	28	ns
t_{PLH}	Propagation delay EI to EO	14	25	17	28	ns
t_{PHL}	Propagation delay EI to EO	15	25	18	28	ns
t_{PLH}	Propagation delay I to A	12	25	15	28	ns
t_{PHL}	Propagation delay I to A	14	25	17	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

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General Description

The 54HSC/T151 is a 1 of 8 Data Selector. When the strobe input is low the device is enabled. When high this forces the W-output high and the Y-output low.

Inputs				Outputs	
Select			Strobe		
C	B	A	$\overline{STR}$	Y	W
X	X	X	H	L	H
L	L	L	L	D_0	D_0B
L	L	H	L	D_1	D_1B
L	H	L	L	D_2	D_2B
L	H	H	L	D_3	D_3B
H	L	L	L	D_4	D_4B
H	L	H	L	D_5	D_5B
H	H	L	L	D_6	D_6B
H	H	H	L	D_7	D_7B

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

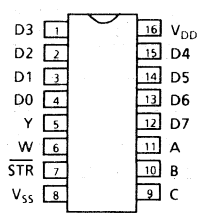


Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay A B or C to Y	15	25	18	28	ns
t_{PHL}	Propagation delay A B or C to Y	16	25	19	28	ns
t_{PLH}	Propagation delay A B or C to W	14	25	17	28	ns
t_{PHL}	Propagation delay A B or C to W	15	25	18	28	ns
t_{PLH}	Propagation delay Strobe to Y	14	25	17	28	ns
t_{PHL}	Propagation delay Strobe to Y	16	25	19	28	ns
t_{PLH}	Propagation delay Strobe to W	14	25	17	28	ns
t_{PHL}	Propagation delay Strobe to W	15	25	18	28	ns
t_{PLH}	Propagation delay D_0-D_7 to Y	12	25	15	28	ns
t_{PHL}	Propagation delay D_0-D_7 to Y	14	25	17	28	ns
t_{PLH}	Propagation delay D_0-D_7 to W	12	25	15	28	ns
t_{PHL}	Propagation delay D_0-D_7 to W	14	25	17	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

54HSC/T154

4 to 16 Line Decoders/Demultiplexers

General Description

The 54HSC/T154 consists of a 4 to 16 Line Decoder/Demultiplexer.

Inputs						Outputs															
$\overline{G1}$	$\overline{G2}$	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay low to high level output for change in A B C or D input	18	30	21	33	ns
t_{PHL}	Propagation delay high to low level output for change in A B C or D input	21	30	24	33	ns
t_{PLH}	Propagation delay low to high level output for change in G1 or G2	21	30	24	33	ns
t_{PHL}	Propagation delay high to low level output for change in G1 or G2	21	30	24	33	ns

V_{CC} = 5V, T_{MAX} = +125°C, C_L = 50pF

Figure 2: Switching Characteristics

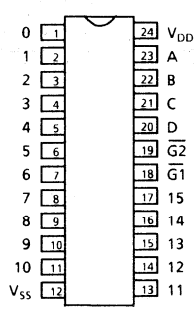


Figure 3: Pin Out

7

Quad 2-Line to 1-Line Data Selectors/Multiplexers

General Description

The 54HSC/T157 is a Quadruple 2-Line to 1-Line Data Selector with non-inverted output. The strobe must be low to enable the device. When select is low, A is selected. When select is high, B is selected.

Inputs				Output
$\overline{STR}$	Select	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

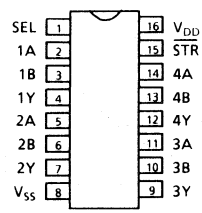


Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay A or B to Y	14	25	17	28	ns
t_{PHL}	Propagation delay A or B to Y	15	25	18	28	ns
t_{PZH}	Propagation delay Strobe to Y	14	25	17	28	ns
t_{PZL}	Propagation delay Strobe to Y	15	25	18	28	ns
t_{PHZ}	Propagation delay Select to Y	14	25	17	28	ns
t_{PLZ}	Propagation delay Select to Y	15	25	18	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

54HSC/T238

3-Line to 8-Line Decoder/Demultiplexer

General Description

The 54HSC/T238 is a 3-Line to 8-Line Decoder/Multiplexer, with unlatched inputs and non-inverted outputs.

Enable Inputs		Select Inputs			Outputs							
E_3	$\overline{E}_2/\overline{E}_1$	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	H	H	L	L	L	H	L	L	L	L
H	L	H	L	L	L	L	L	L	H	L	L	L
H	L	H	L	H	L	L	L	L	L	H	L	L
H	L	H	H	L	L	L	L	L	L	L	H	L
H	L	H	H	H	L	L	L	L	L	L	L	H

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

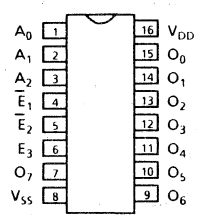


Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay, address to output, low to high level output	16	24	19	27	ns
t_{PHL}	Propagation delay, address to output, high to low level output	17	25	20	28	ns
t_{PLH}	Propagation delay, enable to output, low to high level output	19	27	22	30	ns
t_{PHL}	Propagation delay, enable to output, high to low level output	19	27	22	30	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

7

54HSC/T253

Dual 4 to 1 Data Selectors/Multiplexers

GEC PLESSEY
SEMICONDUCTORS

General Description

The 54HSC/T253 is a Dual 4-Line to 1-Line Data Selector/Multiplexer with tri-state outputs.

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

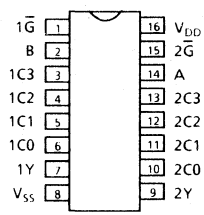


Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay Data to Output	14	25	17	28	ns
t_{PHL}	Propagation delay Data to Output	15	25	18	28	ns
t_{PLH}	Propagation delay Select to Output	14	25	17	28	ns
t_{PHL}	Propagation delay Select to Output	15	25	18	28	ns
t_{PZL}	Propagation delay Tri-state to Output Low	12	25	15	28	ns
t_{PZH}	Propagation delay Tri-state to Output High	13	25	16	28	ns
t_{PLZ}	Propagation delay Low to Tri-state	12	25	15	28	ns
t_{PHZ}	Propagation delay High to Tri-state	13	25	16	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

54HSC/T164

8-Bit Parallel Output Serial Shift Register

General Description

The 54HSC/T164 is an 8-Bit Parallel Output Serial Shift Register with asynchronous clear.

Inputs				Outputs		
$\overline{CLEAR}$	CLOCK	A	B	Q_A	Q_B	Q_H
L	X	X	X	L	L	L
H	L	X	X	Q_{AO}	Q_{BO}	Q_{HO}
H	↑	H	H	H	Q_{AN}	Q_{GN}
H	↑	L	X	L	Q_{AN}	Q_{GN}
H	↑	X	L	L	Q_{AN}	Q_{GN}

H = high level, L = low level, X = irrelevant, ↑ = transition from low to high level. Q_{AO}, Q_{BO}, Q_{HO} = the level of Q_A, Q_B or Q_H, respectively, before the indicated steady-state input conditions were set up. Q_{AN}, Q_{BN}, Q_{HN} = the level of Q_A or Q_G before the latest ↑ transition of the clock. Indicates a one bit shift.

Figure 1: Function Table

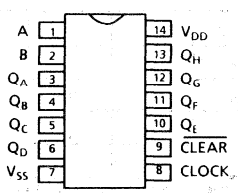


Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay. Q output from clock input, low to high level output.	15	25	18	28	ns
t_{PHL}	Propagation delay, Q output from clock input, high to low level output.	15	25	18	28	ns
t_{PHL}	Propagation delay. Q output from clear input, high to low level output.	15	25	18	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

7

54HSC/T165

Parallel Load 8-Bit Shift Register

GEC PLESSEY
SEMICONDUCTORS

General Description

The 54HSC/T165 is an 8-Bit Serial Shift Register that shifts the data in the direction of Q_A to Q_H when clocked.

Inputs					INTERNAL OUTPUTS		OUTPUT
SHIFT/$\overline{\text{LOAD}}$	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	Q_A	Q_B	Q_H
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{AO}	Q_{BO}	Q_{HO}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{AO}	Q_{BO}	Q_{HO}

H = high level, L = low level, X = irrelevant, ↑ = transition from low to high level, a . . . h = the level of steady state inputs at inputs A through H. Q_O = level of Q before the indicated steady state input conditions were set up. Q_n = level of Q before the most recent active transition indicated by ↑.

Figure 1: Function Table

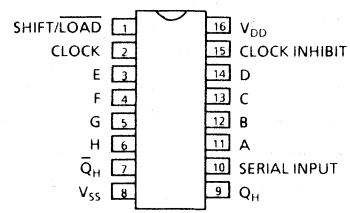


Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay Load to Any Output	18	25	21	28	ns
t_{PHL}	Propagation delay Load to Any Output	16	25	19	28	ns
t_{PLH}	Propagation delay Clock to Any Output	18	25	21	28	ns
t_{PHL}	Propagation delay Clock to Any Output	18	25	21	28	ns
t_{PLH}	Propagation delay H to Q_H	18	25	21	28	ns
t_{PHL}	Propagation delay H to Q_H	18	25	21	28	ns
t_{PLH}	Propagation delay H to QB_H	18	25	21	28	ns
t_{PHL}	Propagation delay H to QB_H	18	25	21	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

54HSC/T166
8-Bit Shift Register

General Description

The 54HSC/T166 is an 8-Bit parallel in or serial in, serial out Shift Register with a gated clock input and an overriding clear input.

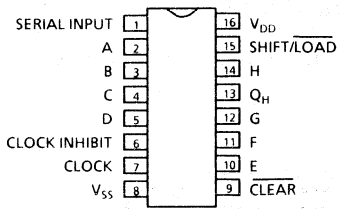


Figure 1: Pin Out

Inputs						INTERNAL OUTPUTS		OUTPUT
$\overline{CLEAR}$	SHIFT/$\overline{LOAD}$	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{AO}	Q_{BO}	Q_{HO}
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{AO}	Q_{BO}	Q_{HO}

H = high level, L = low level, X = irrelevant, ↑ = transition from low to high level, a . . . h = the level of steady state inputs at inputs A through H. Q_O = level of Q before the indicated steady state input conditions were set up. Q_n = level of Q before the most recent active transition indicated by ↑.

Figure 2: Function Table

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PHL}	Propagation delay Clear to Q_H	15	25	18	28	ns
t_{PHL}	Propagation delay Clock to Q_H	15	25	18	28	ns
t_{PLH}	Propagation delay Clock to Q_H	15	25	18	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

7

General Description

The 54HSC/T521 is an 8-Bit Magnitude Comparator.

Inputs		Outputs
Data P, Q	Enable $\overline{G}$	$\overline{P=Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

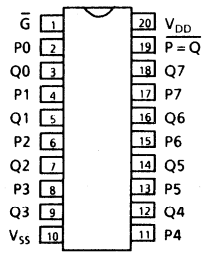


Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay P or Q to PN = QN	15	25	18	28	ns
t_{PHL}	Propagation delay P or Q to PN = QN	16	25	19	28	ns
t_{PLH}	Propagation delay GN to PN = QN	14	25	17	28	ns
t_{PHL}	Propagation delay GN to PN = QN	15	25	18	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

54HSC/T240
Octal 3-State Driver, Inverting

General Description

The 54HSC/T240 is an Octal 3-State Driver, inverting.

Inputs		Outputs
$\overline{E}$	I_{0-3}	$\overline{O}_{0-3}$
L	L	H
L	H	L
H	X	Z

H = high level, L = low level, X = irrelevant, Z = high impedance

Figure 1: Function Table

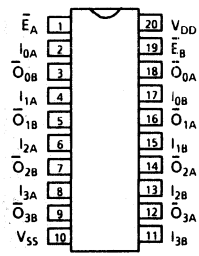


Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay, low to high level output	12	20	15	23	ns
t_{PHL}	Propagation delay, high to low level output	14	22	17	25	ns
t_{PZL}	Propagation delay, enable to low level	19	27	21	30	ns
t_{PZH}	Propagation delay, enable to high level	14	22	17	25	ns
t_{PLZ}	Propagation delay, disable from low	22	30	25	33	ns
t_{PHZ}	Propagation delay, disable from high	21	30	24	33	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

7

54HSC/T241

Octal 3-State Driver, Complementary Enable

GEC PLESSEY
SEMICONDUCTORS

General Description

The 54HSC/T241 is an Octal 3-State Driver, complementary enable.

Inputs			Outputs
$\overline{E}_A$	E_B	I_{0-3}	O_{0-3}
L	H	L	H
L	H	H	L
H	L	X	Z

H = high level, L = low level, X = irrelevant, Z = high impedance

Figure 1: Function Table

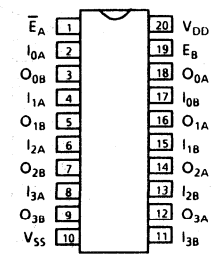


Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay, low to high level output	11	19	14	22	ns
t_{PHL}	Propagation delay, high to low level output	13	21	16	24	ns
t_{PZL}	Propagation delay, enable to low level	19	27	21	30	ns
t_{PZH}	Propagation delay, enable to high level	19	27	21	30	ns
t_{PLZ}	Propagation delay, low to disable	22	30	25	33	ns
t_{PHZ}	Propagation delay, high to disable	21	30	24	33	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

54HSC/T244
Octal 3-State Driver

General Description

The 54HSC/T244 is an Octal 3-State Driver.

Inputs		Outputs
$\overline{E}$	$I_{0\text{-}3}$	$O_{0\text{-}3}$
L	L	L
L	H	H
H	X	Z

H = high level, L = low level, X = irrelevant, Z = high impedance

Figure 1: Function Table

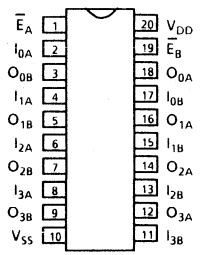


Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay, low to high level output	11	19	14	22	ns
t_{PHL}	Propagation delay, high to low level output	13	21	16	24	ns
t_{PZL}	Propagation delay, enable to low level	19	27	21	30	ns
t_{PZH}	Propagation delay, enable to high level	19	27	21	30	ns
t_{PLZ}	Propagation delay, low to disable	22	30	25	33	ns
t_{PHZ}	Propagation delay, high to disable	21	30	24	33	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

7

54HSC/T540

Octal 3-State Driver/Buffer Inverting

GEC PLESSEY
SEMICONDUCTORS

General Description

The 54HSC/T540 is an Octal 3-State Driver/Buffer Inverting.

Inputs			Outputs
$\overline{E}_A$	$\overline{E}_B$	I_{0-7}	$\overline{O}_{0-7}$
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

H = high level, L = low level, X = irrelevant, Z = high impedance

Figure 1: Function Table

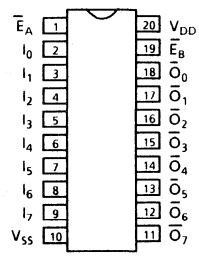


Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay, low to high level output	13	21	16	24	ns
t_{PHL}	Propagation delay, high to low level output	13	21	16	24	ns
t_{PZL}	Propagation delay, enable to low level	21	29	24	32	ns
t_{PZH}	Propagation delay, enable to high level	16	24	19	27	ns
t_{PLZ}	Propagation delay, low to disable	24	32	27	35	ns
t_{PHZ}	Propagation delay, high to disable	23	31	26	34	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

54HSC/T541
Octal 3-State Driver/Buffer

General Description

The 54HSC/T541 is an Octal 3-State Driver/Buffer.

Inputs			Outputs
$\overline{E}_A$	$\overline{E}_B$	I_{0-7}	O_{0-7}
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

H = high level, L = low level, X = irrelevant, Z = high impedance

Figure 1: Function Table

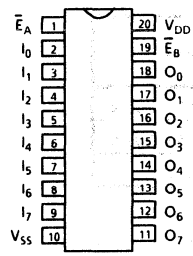


Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay, low to high level output	11	19	14	22	ns
t_{PHL}	Propagation delay, high to low level output	13	21	16	24	ns
t_{PZL}	Propagation delay, enable to low level	21	29	24	32	ns
t_{PZH}	Propagation delay, enable to high level	16	24	19	27	ns
t_{PLZ}	Propagation delay, low to disable	24	32	27	35	ns
t_{PHZ}	Propagation delay, high to disable	23	31	26	34	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

7

General Description

The 54HSC/T245 is an Octal Bus Transceiver.

Inputs		Outputs
$\overline{E}$	DIR	
L	L	Bus B data to Bus A data
L	H	Bus B data to Bus A data
H	X	Isolation

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

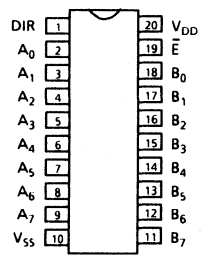


Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay, low to high level output	10	25	13	28	ns
t_{PHL}	Propagation delay, high to low level output	11	25	14	28	ns
t_{PZL}	Propagation delay, enable to low level	21	30	24	33	ns
t_{PZH}	Propagation delay, enable to high level	16	25	19	28	ns
t_{PLZ}	Propagation delay, low to disable	24	30	27	33	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

54HSC/T373

Octal Transparent Latch, 3-State Outputs

General Description

The 54HSC/T373 is an Octal Transparent Latch with 3-State Outputs.

Inputs			Outputs
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level, X = irrelevant, Z = high impedance

Figure 1: Function Table

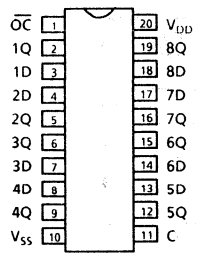


Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)			HST (TTL Comp.)			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH}	Propagation delay, low to high level output	-	19	27	-	19	30	ns
t_{PHL}	Propagation delay, high to low level output	-	19	27	-	19	30	ns
t_{PZL}	Propagation delay, enable to low level	-	13	21	-	13	24	ns
t_{PZH}	Propagation delay, enable to high level	-	16	24	-	16	27	ns
t_{PLZ}	Propagation delay, low to disable	-	14	22	-	17	25	ns
t_{PHZ}	Propagation delay, high to disable	-	13	21	-	16	24	ns
t_{SU}	Propagation delay, set up time	15	-	-	18	-	-	ns
t_H	Propagation delay, hold time	0	-	-	0	-	-	ns
t_W	Propagation delay, minimum pulse width	15	-	-	18	-	-	ns
t_{PLHE}	Propagation delay, C to high output	19	-	27	22	-	30	ns
t_{PHLE}	Propagation delay, C to low output	19	-	27	22	-	30	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

7

54HSC/T573

Octal Transparent Latch, 3-State Outputs

GEC PLESSEY
SEMICONDUCTORS

General Description

The 54HSC/T573 is an Octal Transparent Latch with 3-State Outputs.

Inputs			Outputs
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level, X = irrelevant, Z = high impedance

Figure 1: Function Table

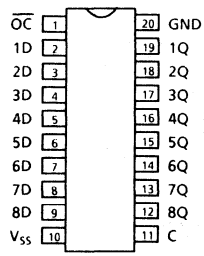


Figure 2: Pin Out

Symbol	Parameter	HSC (CMOS Comp.)			HST (TTL Comp.)			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH}	Propagation delay, low to high level output	-	19	27	-	22	30	ns
t_{PHL}	Propagation delay, high to low level output	-	19	27	-	22	30	ns
t_{PZL}	Propagation delay, enable to low level	-	13	21	-	16	24	ns
t_{PZH}	Propagation delay, enable to high level	-	16	24	-	19	27	ns
t_{PLZ}	Propagation delay, low to disable	-	14	22	-	17	25	ns
t_{PHZ}	Propagation delay, high to disable	-	13	21	-	16	24	ns
t_{SU}	Propagation delay, set up time	15	-	-	18	-	-	ns
t_H	Propagation delay, hold time	0	-	-	0	-	-	ns
t_W	Propagation delay, minimum pulse width	15	-	-	18	-	-	ns
t_{PLHE}	Propagation delay, C to high output	19	-	27	22	-	30	ns
t_{PHLE}	Propagation delay, C to low output	19	-	27	22	-	30	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 3: Switching Characteristics

54HSC/T670

4 x 4 Register Files with Tri-State Outputs

General Description

The 54HSC/T670 is a register storing 4 words of 4 bits each. Separate on-chip decoding is provided for addressing the four word locations to either write or retrieve data. This allows simultaneous writing into one location and reading from another location.

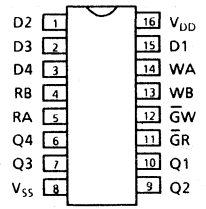


Figure 1: Pin Out

Write Inputs			Word			
WB	WA	$\overline{GW}$	1	2	3	4
L	L	L	Q = D	Q0	Q0	Q0
L	H	L	Q0	Q = D	Q0	Q0
H	L	L	Q0	Q0	Q = D	Q0
H	H	L	Q0	Q0	Q0	Q = D
X	X	H	Q0	Q0	Q0	Q0

Q_0 = level of Q before inputs were established
H = high level, L = low level, X = irrelevant

Figure 2: Write Function Table

Read Inputs			Outputs			
RB	RA	$\overline{GR}$	Q1	Q2	Q3	Q4
L	L	L	W1D1	W1D2	W1D3	W1D4
L	H	L	W2D1	W2D2	W2D3	W2D4
H	L	L	W3D1	W3D2	W3D3	W3D4
H	H	L	W4D1	W4D2	W4D3	W4D4
X	X	H	Z	Z	Z	Z

H = high level, L = low level, X = irrelevant, Z = high impedance

Figure 3: Read Function Table

Symbol	Parameter	HSC (CMOS Comp.)		HST (TTL Comp.)		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay Read Select to Q	25	30	28	33	ns
t_{PHL}	Propagation delay Read Select to Q	18	25	21	28	ns
t_{PLH}	Propagation delay Write Enable to Q	18	25	21	28	ns
t_{PHL}	Propagation delay Write Enable to Q	18	25	21	28	ns
t_{PLH}	Propagation delay Data to Q	27	35	30	38	ns
t_{PHL}	Propagation delay Data to Q	23	25	26	28	ns
t_{PZH}	Propagation delay Read Enable to Q	18	25	21	28	ns
t_{PZL}	Propagation delay Read Enable to Q	18	25	21	28	ns
t_{PHZ}	Propagation delay Read Enable to Q	18	25	21	28	ns
t_{PLZ}	Propagation delay Read Enable to Q	18	25	21	28	ns

V_{CC} = 5V, T_{MAX} = + 125°C, C_L = 50pF

Figure 4: Switching Characteristics

7

Timing Diagrams

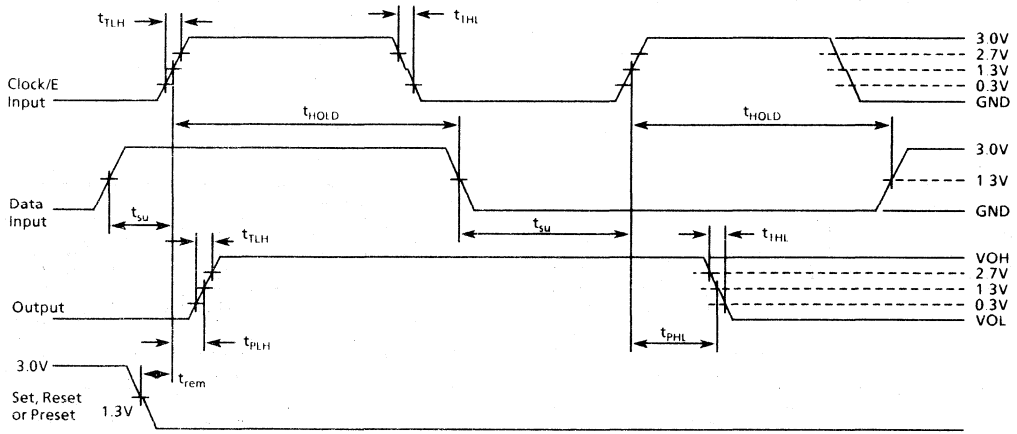


Figure 3: Set-up times, hold times, removal time and propagation delay times

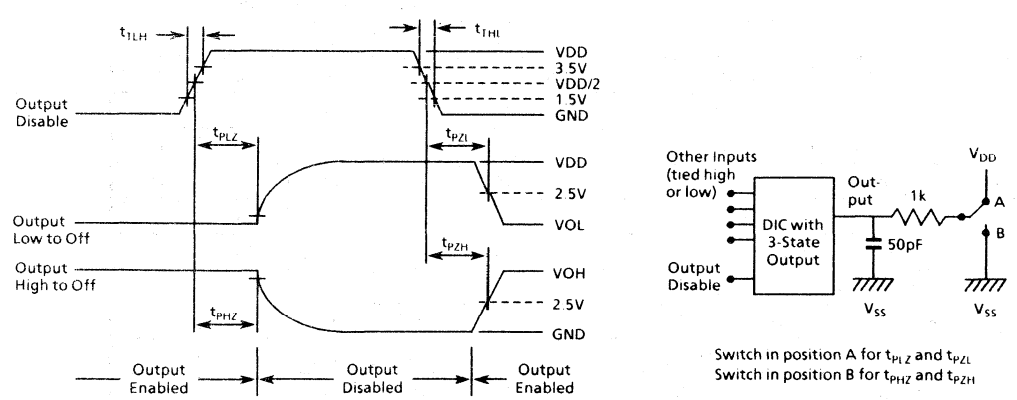


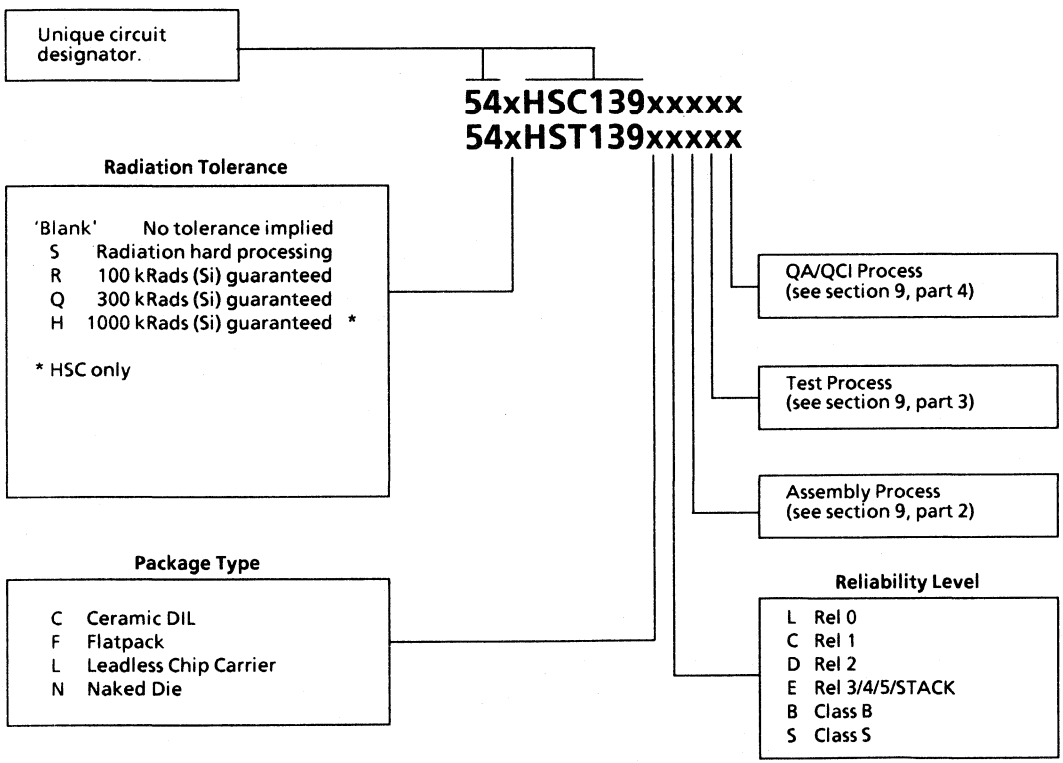
Figure 4: Three-state propagation delay wave shapes and test circuit

54HSC/T Series

Radiation Hard High Speed CMOS/SOS Logic

Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



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SEMICONDUCTORS

S10503FDS Issue 2.2 October 1990

54 HSC/T 630

Radiation Hard 16-Bit Parallel Error Detection & Correction

Features

- **Radiation Hard:**
  Dose rate upset exceeding $3x10^{10}$ Rad (Si)/sec.
  Total dose for functionality upto $1x10^{6}$ Rad (Si).
- **High SEU immunity, latch up free**
- **CMOS-SOS technology**
- **All inputs & outputs fully TTL compatible (54 HST 630) or CMOS compatible (54 HSC 630)**
- **Low power**
- **Detects and corrects single-bit errors**
- **Detects and flags dual-bit errors**
- **High speed:**
  Write cycle- Generates checkword in 40ns typ.
  Read cycle- Flags errors in 20ns typ.

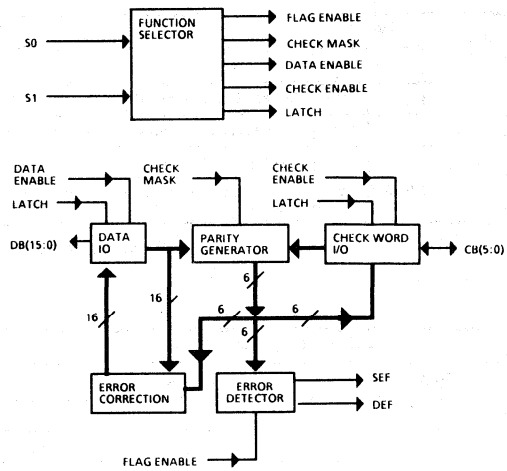

Figure 1: Block Diagram

General Description

The 54HSC/T630 is a 16-bit parallel Error Detection and Correction circuit. It uses a modified Hamming code to generate a 6-bit check word from each 16-bit data word. The check word is stored with the data word during a memory write cycle. During a memory read cycle a 22-bit word is taken from memory and checked for errors.

Single bit errors in data words are flagged and corrected. Single bit errors in check words are flagged but not corrected. The position of the incorrect bit is pinpointed, in both cases, by the 6-bit error syndrome code which is output during the error correction cycle.

Two bit errors are flagged but not corrected. Any combination of two bit errors occurring within the 22-bit word read from memory, (ie two errors in the 16-bit data word, two bits in the 16-bit check word or one error in each) will be correctly identified.

The gross errors of all bits, low or high, will be detected.

The control signals S1 and S0 select the function to be performed by the EDAC. They control the generation of check words and the latching and correction of data (see table 1). When errors are detected, flags are placed on outputs SEF and DEF (see table 2).

7

Memory Cycle	Control		EDAC Function	Data I/O	Checkword	Error Flags	
	S1	S0				SEF	DEF
WRITE	Low	Low	Generates Checkword	Input Data	Output Checkword	Low	Low
READ	Low	High	Read Data &Checkword	Input Data	Input Checkword	Low	Low
READ	High	High	Latch & Flag Error	Latch Data	Latch Checkword	Enabled	Enabled
READ	High	Low	Correct Data Word & Generate Syndrome Bits	Output Corrected Data	Output Syndrome Bits	Enabled	Enabled

Table 1. Control Functions

Total Number of Errors		Error Flags		Data Correction
16-bit Data	6-bit Checkword	SEF	DEF	
0	0	Low	Low	Not Applicable
1	0	High	Low	Correction
0	1	High	Low	Correction
1	1	High	High	Interrupt
2	0	High	High	Interrupt
0	2	High	High	Interrupt

Table 2. Error Functions

Error Detection & Correction

During a memory write cycle, six check bits (CB0-CB5) are generated by eight-input parity generators using the data bits defined in Table 3. During a memory read cycle, the 6-bit checkword is retrieved along with the actual data.

Error detection is accomplished as the 6-bit checkword and the 16-bit data word from memory are applied to internal parity generators/checkers. If the parity of all six groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be low. It should be noted that the sense of two of the check bits, bits CB0 and CB1, is inverted to ensure that the gross-error condition of all lows and all highs is detected.

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set high. Any single error in the 16-bit data word will change the sense of exactly three bits of the 6-bit checkword. Any single error in the 6-bit checkword changes the sense of only that one bit. In either case, the single error flag will be set high while the dual error flag will remain low.

Any two-bit error will change the sense of an even number of check bits. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set high when any two-bit error is detected.

Three or more simultaneous bit errors can fool the EDAC into believing that no error, a correctable error, or an uncorrectable error has occurred and produce erroneous results in all three cases.

Error correction is accomplished by identifying the bad bit and inverting it. Identification of the erroneous bit is achieved by comparing the 16-bit word and 6-bit checkword from memory with the new checkword with one (checkword error) or three (data word error) inverted bits.

As the corrected word is made available on the data word I/O port, the checkword I/O port presents a 6-bit syndrome error code. This syndrome code can be used to identify the corrupted bit in memory (see Table 4. below).

Checkword Bit	16-bit Data Word															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0	X	X		X	X				X	X	X			X		
CB1	X		X	X		X	X		X			X			X	
CB2		X	X		X	X		X		X			X			X
CB3	X	X	X				X	X			X	X	X			
CB4				X	X	X	X	X						X	X	X
CB5									X	X	X	X	X	X	X	X

The six check bits are parity bits derived from the matrix of data bits as indicated by 'X' for each bit.

Table 3. Check Word Generation

Syndrome Error Code	Error Location																						
	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8	DB9	DB10	DB11	DB12	DB13	DB14	DB15	CB0	CB1	CB2	CB3	CB4	CB5	No Error
CB0	L	L	H	L	L	H	H	H	L	L	L	H	H	L	H	H	L	H	H	H	H	H	H
CB1	L	H	L	L	H	L	L	H	L	H	H	L	H	H	L	H	H	L	H	H	H	H	H
CB2	H	L	L	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	L	H	H	H	H
CB3	L	L	L	H	H	H	L	L	H	H	L	L	L	H	H	H	H	H	H	L	H	H	H
CB4	H	H	H	L	L	L	L	L	H	H	H	H	H	L	L	L	H	H	H	H	L	H	H
CB5	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	H	H	H	H	H	L	H

Table 4. Error Syndrome Codes

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Radiation Hard 16-Bit Parallel Error Detection & Correction

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Applications

Although many semiconductor memories have separate input and output pins, it is possible to design the error detection and correction function using a single EDAC . EDAC data and check bit pins function as inputs or outputs dependent upon the state of control signals S0 and S1. It becomes necessary to use wired AND logic, with fairly complex timing system, to control the EDAC and data bus. This scheme becomes difficult to implement both in terms of board layout and timing. System performance is also adversely affected. See Figure 2.

Optimised systems can be implemented using two EDAC's in parallel. One of the units is used strictly as an encoder during the memory write cycle. Both controls S0 and SI are grounded. The encoder chip will generate the 6-bit check word for memory storage along with the 16-bit data.

The second of the two EDAC's will be used as a decoder during the memory read cycle. This decoder chip requires timing pulses for correct operation. Control SI is set low and S0 high as the memory read cycle begins. After the memory output data is valid, the control SI input is moved from the low to a high. This low-to-high transition latches the 22-bit word from memory into internal registers of this second EDAC and enables the two error flags. If no error occurs, the CPU can accept the 16-bit word directly from memory. If a single error has occurred, the CPU must move the control SO input from the high to a low to output corrected data and the error syndrome bits. Any dual error should be an interrupt condition.

In most applications , status registers will be used to keep tabs on error flags and error syndrome bits. If repeated patterns of error flags and syndrome bits occur, the CPU will be able to recognize these symptoms as a "hard" error. The syndrome bits can be used to pinpoint the faulty memory chip. See Figure 3.

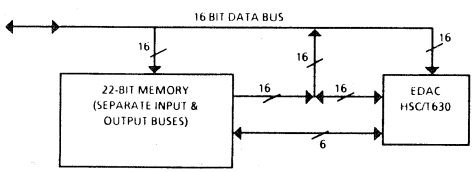
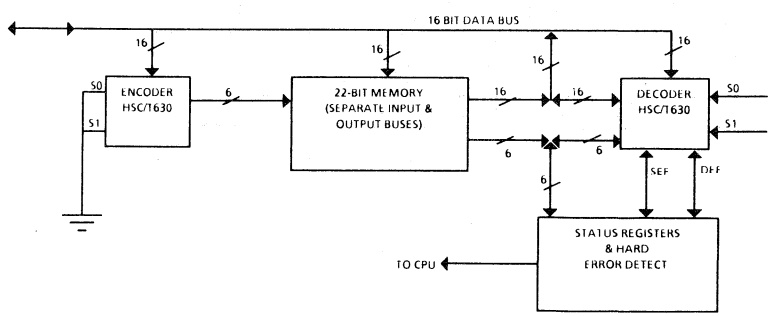


Figure 2. Error Detection and Correction using a single EDAC Unit



S1	S0	FUNCTION
L	H	Start READ
H	H	Latch data & flag errors
H	L	Correct data & output syndrome bits

Figure 3. Error Detection and Correction using two EDAC Units

54 HSC/T 630

Radiation Hard 16-Bit Parallel Error Detection & Correction

Ratings and Characteristics

Parameter	Min.	Max.	Units
Supply voltage	-0.5	10	V
Input voltage	V_{SS}-0.3	V_{DD} + 0.3	V
Current through any pin	-20	20	mA
Operating temperature	-55	125	°C
Storage temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5: Absolute Maximum Ratings

Symbol	Parameter	Conditions	Total Dose Radiation Not Exceeding $3x10^5$ Rad (Si)			HSC Only Total Dose ≤1 MRad (Si)		Units
			Min.	Typ.	Max.	Min.	Max.	
V_{DD}	Supply voltage	-	4.5	5.0	5.5	4.5	5.5	V
V_{IH1}	TTL input high voltage	-	2.0	-	-	-	-	V
V_{IL1}	TTL input low voltage	-	-	-	0.8	-	-	V
V_{OH1}	TTL output high voltage	I_{OH} = -4mA	2.4	-	-	-	-	V
V_{OL1}	TTL output low voltage	I_{OL} = 12mA (CB or DB), I_{OL} = 4mA(SEF or DEF)	-	-	0.4	-	-	V
V_{IH2}	CMOS input high voltage	-	3.5	-	-	3.5	-	V
V_{IL2}	CMOS input low voltage	-	-	-	1.5	-	1.0	V
V_{OH2}	CMOS output high voltage	I_{OH} = -4mA	V_{DD} - 0.5	-	-	V_{DD} - 0.5	-	V
V_{OL2}	CMOS output low voltage	I_{OL} = 12mA (CB or DB), I_{OL} = 4mA(SEF or DEF)	-	-	0.5	-	0.5	V
I_{IL}	Input low current	V_{DD} = 5.5, V_{IN} = V_{SS}	-	-	-10	-	-100	uA
I_{2L}	IO low current	V_{DD} = 5.5, V_{IN} = V_{SS}	-	-	-50	-	-100	uA
I_{IH}	Input high current	V_{DD} = 5.5, V_{IN} = V_{DD}	-	-	10	-	100	uA
I_{2H}	IO high current	V_{DD} = 5.5, V_{IN} = V_{DD}	-	-	50	-	100	uA
I_{DD}	Power supply current	V_{DD} = Max, S0 & S1 at 4.5V, All CB & DB pins grounded, DEF & SEF open	-	-	1	-	10	mA

V_{DD} = 5V ± 10%, over full operating temperature range.

Table 6: DC Electrical Characteristics

7

Parameter	From (Input)	To (Output)	Min.	Max.	Units	Conditions
t_{PLH} Propagation delay time, low-to-high-level output (note 4)	DB	CB	-	58	ns	S0 = 0V, S1 = 0V
t_{PHL} Propagation delay time, high-to-low-level output (note 4)	DB	CB	-	58	ns	S0 = 0V, S1 = 0V
t_{PLH} Propagation delay time, low-to-high-level output (note 5)	S1 ↑	DEF	-	29	ns	S0 = 3V
t_{PLH} Propagation delay time, low-to-high-level output (note 5)	S1 ↑	SEF	-	29	ns	S0 = 3V
t_{PZH} Output enable time to high level (note 6)	S0 ↓	CB, DB	-	40	ns	S1 = 3V (fig. 5)
t_{PZL} Output enable time to low level (note 6)	S0 ↓	CB, DB	-	45	ns	S1 = 3V (fig. 4)
t_{PHZ} Output disable time from high level (note 7)	S0 ↑	CB, DB	-	45	ns	S1 = 3V (fig. 5)
t_{PLZ} Output disable time from low level (note 7)	S0 ↑	CB, DB	-	65	ns	S1 = 3V (fig. 4)
t_s Set-up time to S1 ↑	CB, DB	-	30	-	ns	-
t_h Hold time after S1 ↑	CB, DB	-	15	-	ns	-

1. V_{DD} = 5V ± 10% and C_L = 50pF, over full operating temperature range.
2. Input Pulse V_{SS} to 3.0 Volts.
3. Times Measurement Reference Level 1.5 Volts.
4. These parameters describe the time intervals taken to generate the check word during the memory write cycle.
5. These parameters describe the time intervals taken to flag errors during memory read cycle.
6. These parameters describe the time intervals taken to correct and output the data word and to generate and output the syndrome error code during the memory read cycle.
7. These parameters describe the time intervals taken to disable the CB & DB buses in preparation for a new data word during the memory read cycle.

Table 7: AC Electrical Characteristics

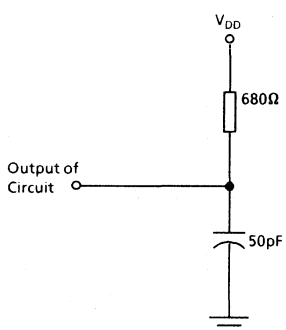


Figure 4. Output Load Circuit

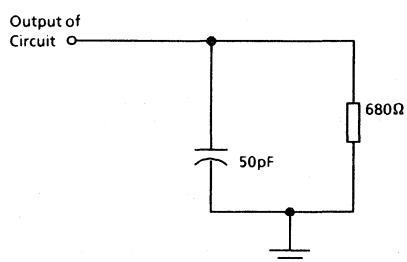


Figure 5. Output Load Circuit

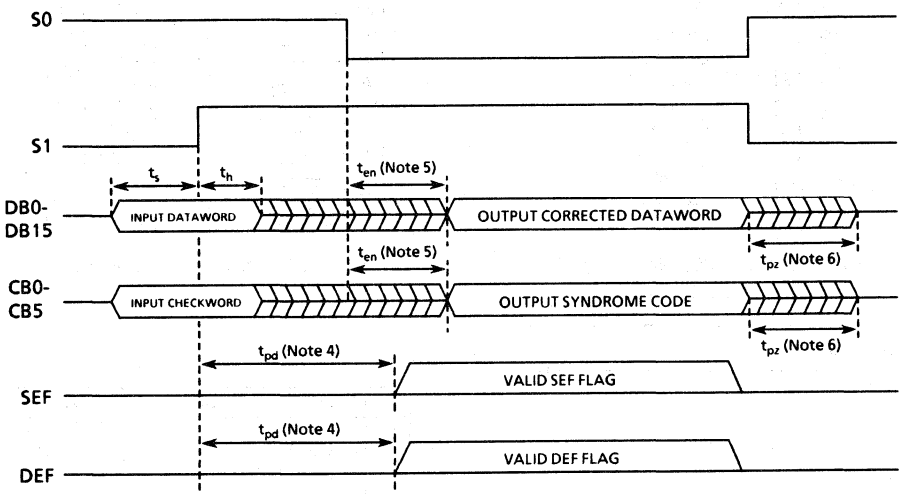


Figure 6. Read, Flag, and Correct, Mode Switching Waveforms.

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Radiation Hard 16-Bit Parallel Error Detection & Correction

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Pin Assignment

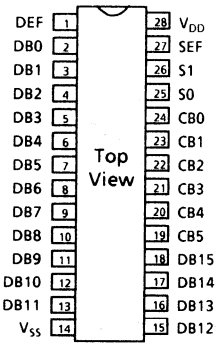


Fig. 7 28-Lead Ceramic DIL (solder seal) package style C

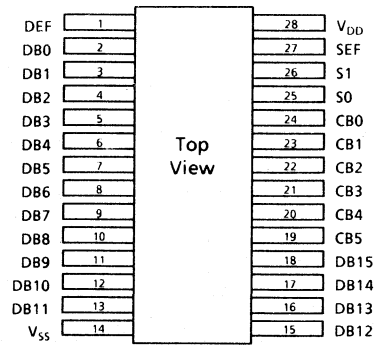


Fig. 8 28-Lead Flatpack (solder seal) package style F

Package Outline

Ref.	Min.	Nom.	Max.
A	-	-	5.60 (0.220)
A_1	0.83 (0.015)	-	1.53 (0.060)
b	0.35 (0.014)	-	0.59 (0.023)
c	0.20 (0.008)	-	0.36 (0.014)
D	-	-	36.02 (1.418)
e	-	2.54(0.100) typ.	-
e_1	-	15.24(0.600) typ.	-
H	4.71 (0.185)	-	5.38 (0.212)
M_E	-	-	15.90 (0.626)
Z	-	-	1.27 (0.050)
W	-	-	1.53 (0.060)
Dimensions in mm (inches)			

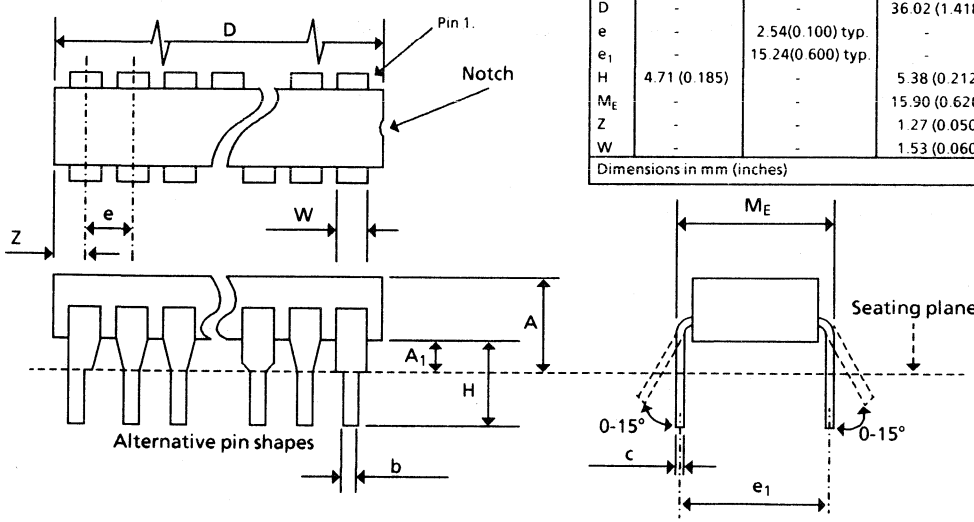
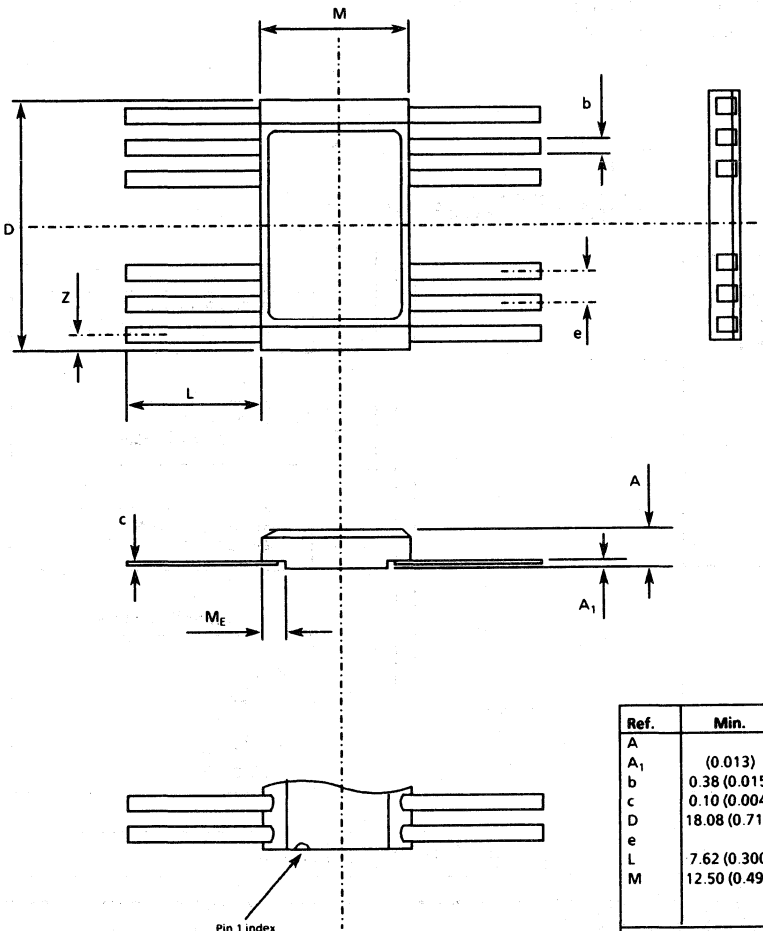


Figure 9. 28-Lead Ceramic DIL (solder seal) - package style C

54 HSC/T 630

Radiation Hard 16-Bit Parallel Error Detection & Correction



Ref.	Min.	Nom.	Max.
A			2.36 (0.093)
A_1	(0.013)		(0.017)
b	0.38 (0.015)		0.48 (0.019)
c	0.10 (0.004)		0.18 (0.007)
D	18.08 (0.712)		18.49 (0.728)
e		1.27 (0.050)	
L	7.62 (0.300)		9.91 (0.390)
M	12.50 (0.492)		12.09 (0.508)

Dimensions in mm (inches)

MEDL XG530

Figure 10: 28-lead Ceramic Flatpack (solder seal) - Package style F

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Radiation Hard 16-Bit Parallel Error Detection & Correction

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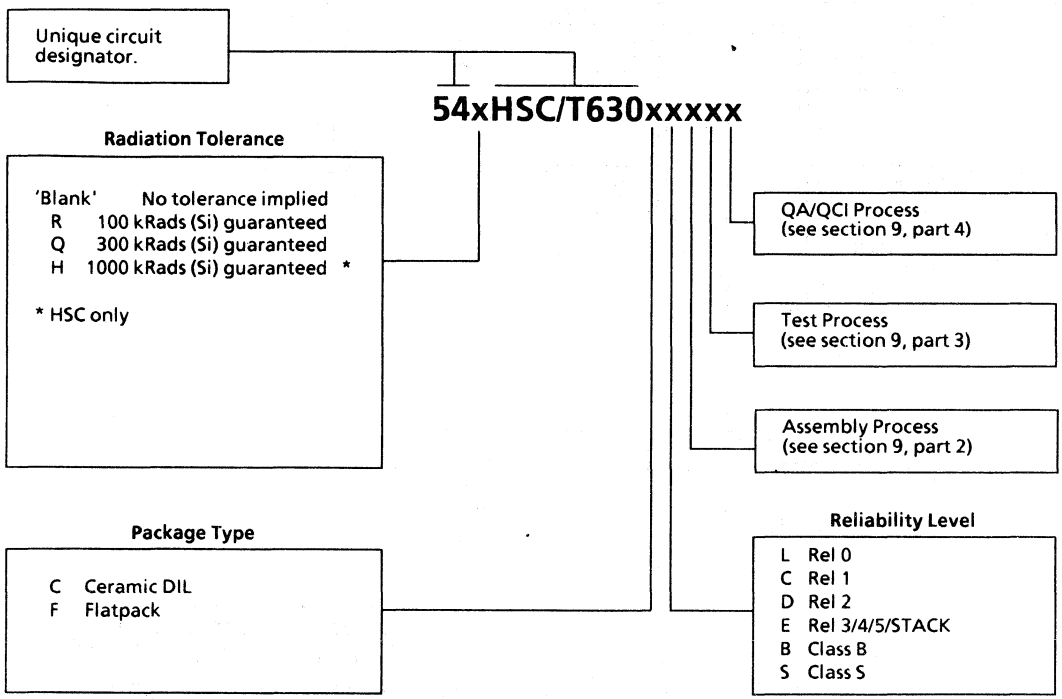
SEMICONDUCTORS

Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

Radiation Performance

Total Dose (Function to spec)	$3x10^5$ Rad (Si)
Total Dose (Function to 1MRad (Si) spec)	$1x10^6$ Rad (Si)
Transient Upset (stored data loss)	$3x10^{10}$ Rad (Si) /s
Transient Upset (survivability)	$>1x10^{12}$ Rad (Si)/s
Neutron Hardness (Function to spec)	$1x10^{15}$ neutrons/cm^2
Latch-up	Not possible

section 8

SEMICONDUCTOR ASICs & FOUNDRY SERVICE

GEC PLESSEY

SEMICONDUCTORS

S21600FDS Issue 1.2 November 1990

MA9000A Sea of Gates

Radiation Hard Advanced Gate Array Design System

Features

- **Channelless array architecture**
- **Typical gate delay 1.0nS - toggle rates of 100MHz achievable**
- **1.25uW/MHz power dissipation per active gate**
- **Extensive CAD design and support system**
- **Comprehensive library of logic cells and logic function building macros, with RAM & ROM**
- **Double-Level-Metal CMOS/SOS Technology**
- **High SEU immunity, latch-up free**
- **Radiation hard to 1MRad(Si)**

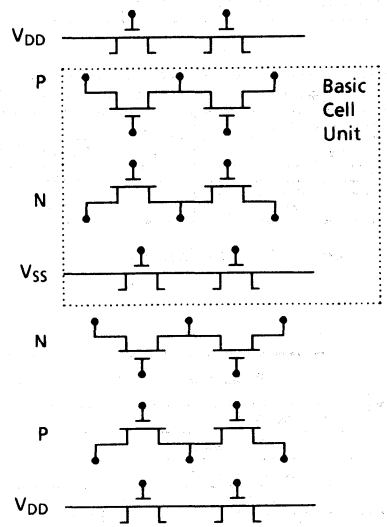


Figure 1: Basic Cell Unit

General Description

The logic building block is a six transistor 'cell-unit', equivalent in size to a two input NAND gate. The cell contains four transistors for building logic circuits and two transistors which are used in RAM macros. These extra two transistors are placed under the logic power routing and so have no detrimental effect upon overall area. Back-to-back cell units form the core of the array.

The interconnection patterns that cause groups of cell-units to become defined logic cells, and the models which are used to simulate these cells, are stored as software in libraries. Cells up to the complexity of multiple bit shift registers are treated in this way.

Array Options

Array type	Cell units	Bonding pads		
		I/O	Power	Total
MA9140	14112	102	8	110
MA9200	20296	120	8	128

Any I/O site may be configured as a power pad to give flexible bonding option, but to standardise testing preferred positions exist. Each cell-unit is the equivalent to either one 2 input NAND gate or one RAM storage bit.

8

DC Charcteristics and Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0.5	7	V
V_I	Input voltage	-0.3	V_{DD} + 0.3	V
T_A	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Figure 2: Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH1}	TTL input high voltage	-	2.0	-	-	V
V_{IL1}	TTL input low voltage	-	-	-	0.8	V
V_{IH2}	CMOS input high voltage	-	70	-	-	%V_{DD}
V_{IL2}	CMOS input low voltage	-	-	-	30	%V_{DD}
V_{OH1}	TTL output high voltage	I_{OH} = -2.0mA	2.4	-	-	V
V_{OL1}	TTL output low voltage	I_{OL} = 5.0mA	-	-	0.4	V
V_{OH2}	CMOS output high voltage	I_{OH} = -4mA	90	-	-	%V_{DD}
V_{OL2}	CMOS output low voltage	I_{OL} = 4mA	-	-	10	%V_{DD}
I_L	Input leakage current	-	-	-	10	uA
I_{OZ}	Output leakage current	Tristate Output	-	-	10	uA
I_{DD}	Static power supply current	-	-	0.5	5	mA

V_{DD} = 5V ± 10%, over full operating temperature range

Figure 3: Electrical Characteristics

AC Characteristics

Cell Name	Function	O/P Edge	Inherent Delay	Per 1pF Load*	Units
NOP	Inverting buffer	Rising	0.3	0.2	ns
		Falling	0.3	0.2	
NAND2	2 input NAND	Rising	0.7	5.0	ns
		Falling	0.5	4.8	
DT	D type	Rising CK - QB	2.7	8.9	ns
		Falling CK - QB	3.0	4.8	
		Data set-up time	3.1	-	
		Data Hold time	1.9	-	

* 1pF is equivalent to fanout of 8 standard gates.

Figure 4: Electrical Characteristics

Propagation Delay

Worst case maximum propagation delays for 5 volts working and 25°C are stated in the cell libraries. These are for the data change or state change which gives the greatest delay. Typical process figures under the same conditions are generally 75% of those listed.

Use the following to predict delays at any other working temperature or voltage:

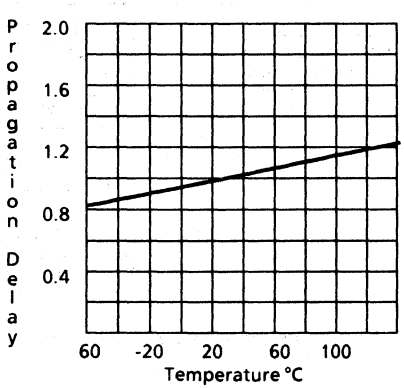


Figure 5: Propagation Delay Vs Temperature

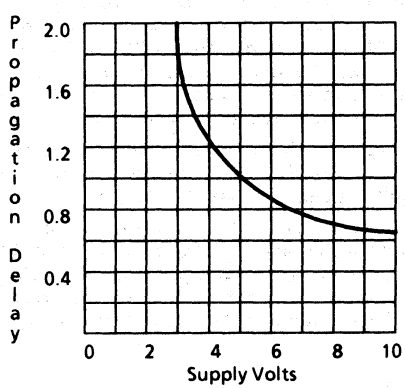


Figure 6: Propagation Delay Vs Supply Voltage

8

Radiation Hard Advanced Gate Array Design System

GEC PLESSEY
SEMICONDUCTORS

Standard Package Options

Marconi offer a wide range of packages as standard. Other package styles are available. If you require a package not covered on this list, contact Marconi.

Ceramic DIL	24	28	40	48	64	-
Cerdip	24	28	40	48	-	-
Leaded Flatpack	28	42	48	64	84	132
Pin Grid Array	68	84	100	120	144	-
Ceramic LCC	(40)	44	(48)	68	84	-
Cerquad	44	68	84	-	-	-

Figure 7: Standard Package Options

Development Interfaces

All design activities prior to mask creation, including automatic layout may be carried out by the equipment manufacturer, and may be delegated to a Marconi design centre.

The full design package runs on a Vax/11 series system, MicroVax (including Daisy LOGICIAN MicroVax combination), and Apollo and Mentor workstations. MEDL support for the DAZIX workstation permits schematic entry of data, workfile verification by simulation and the production of the HILO formatted data base required for automatic layout.

Design specific software, including schematic capture and simulation libraries for DAZIX and Mentor workstations, is supplied by Marconi.

Connection to the Marconi design centre via an X25 protocol or similar telephone link or the use of terminals within a Marconi 'design shop' are other possible options which permit a customer to participate in design activities without involvement in major capital outlay.

Training courses that cover all aspects of design and cater for different levels of starting experience are run at the Marconi Wembley Design centre. Some of these courses may be combined with 'design shop' activities.

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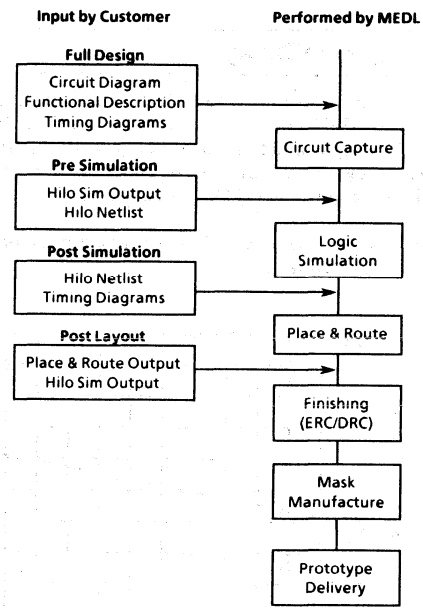


Figure 8: Development Interfaces

MA9000A Sea of Gates

Radiation Hard Advanced Gate Array Design System

RadiationTolerance

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

Total Dose (Function to specification) note 1	$1x10^6$ Rad(Si)
Total Dose (Function to specification) note 2	$3x10^5$ Rad(Si)
Transient Upset (stored data loss)	10^{11} Rad(Si)/sec
Transient Upset (survivability)	$>10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>10^{15}$ neutrons/cm^2
Single Event Upset (GSO 10% worst case)	$<5x10^{-11}$ errors/bitday
Latch-up	Not possible

1 Circuits with all CMOS type inputs
2 Circuits with all TTL type inputs

Table 9: Radiation Hardness Parameters

Macro Design Service

Marconi offer a flexible macro design service to support customer requirements for non-standard cells. Listed are examples of some customer specified Macros that have been designed.

- MA29xx bit slice series elements.
- ALU
- Asynchronous counters
- Parity detectors
- Ripple carry adders
- Selectors
- Gray counters
- Johnson counters
- Lookahead adders

The MA9000A Sea of Gates is a particularly effective route for creating RAM macros.

For more information on Macros and additions to the family contact our nearest office.

MA9000A Sea of Gates

Radiation Hard Advanced Gate Array Design System

GEC PLESSEY

SEMICONDUCTORS

Cell Library Quick Guide

Cell Name	Function	Cell Units
COMBINATIONAL GATES		
INV	Inverter	1
INVB	Fast inverter	1
INVC	Super fast inverter	2
BUFF	Non-inverting buffer	1
BUFFB	Fast non-inverting buffer	2
BUFFC	Super fast non-inverting buffer	3
NAND2	2 input NAND	1
NAND2B	Fast 2 input NAND	2
NAND3	3 input NAND	2
NAND4	4 input NAND	2
AND2	2 input AND	2
AND3	3 input AND	2
AND4	4 input AND	3
NOR2	2 input NOR	1
NOR2B	Fast 2 input NOR	2
NOR3	3 input NOR	2
NOR4	4 input NOR	2
OR2	2 input OR	2
OR3	3 input OR	2
OR4	4 input OR	3
ANDNOR	2 + 2 input AND/NOR	2
ORNAND	2 + 2 OR/NAND	2
EXNOR	Exclusive NOR	4
EXOR	Exclusive OR	4
SEL2INV	Select 1 of 2 (inverting)	4
SEL2	Select 1 of 2	4
SEL4INV	4 bit data selector (inverting)	8
SEL4	4 bit data selector	8
ARITHMETIC		
HAD	Half adder	4
FAD	Full adder	8
FLAD	Fast look ahead adder	6
LAH2	2 bit look ahead unit	12
LAH3	3 bit look ahead unit	16
LAH4	4 bit look ahead unit	25
SIMPLE LATCHES		
NASR	NAND set reset-latch	3
NOSR	NOR set-reset latch	3
CLOCKED LATCHES		
DL	D-latch (Active low)	4
DLH	D-latch (Active high)	4
SDL	Set D-latch	4
RDL	Reset D-latch	4
SRDL	Set/reset D-latch	6
EDGE TRIGGERED LATCHES		
RETS		8
SRETS		8
MASTER-SLAVE FLIP-FLOPS		
DT	D-type	6
D2T	Dual input D-type	8
SDT	Set D-type	4
RDT	Reset D-type	8
SRDT	Set/reset D-type	8

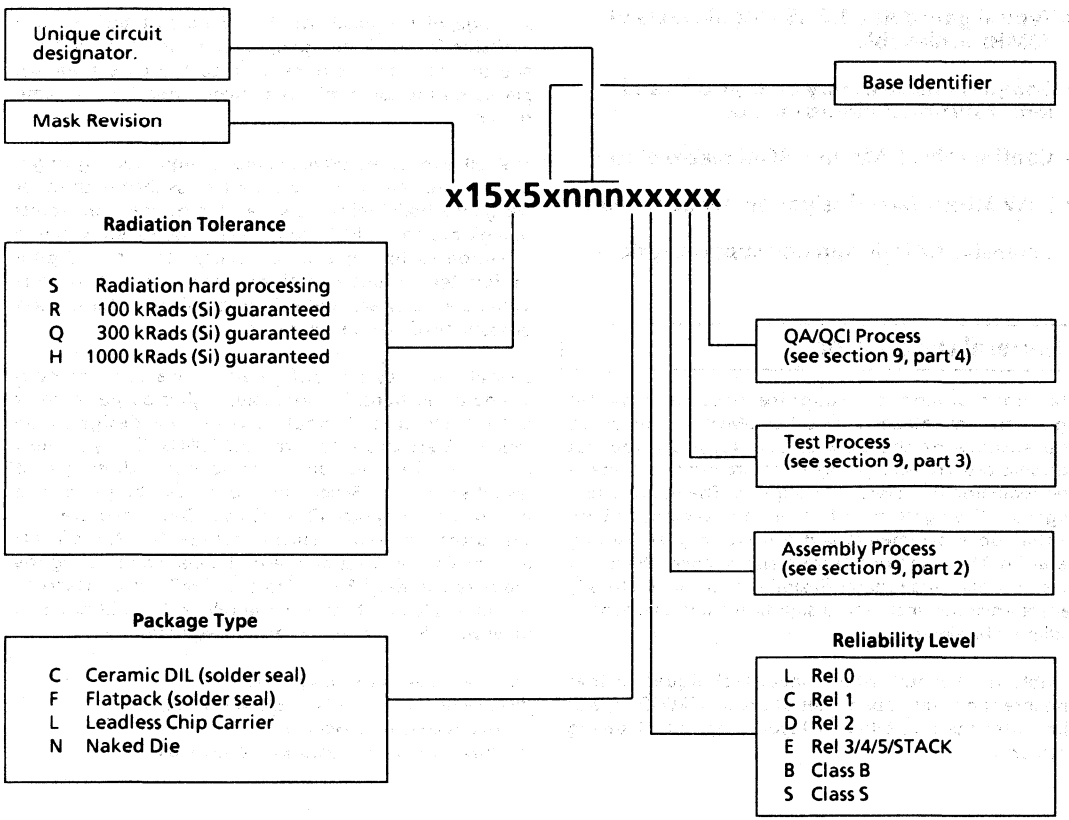
Cell Name	Function	Cell Units
TOGGLE FLIP-FLOPS		
STT	Set T-type	8
RTT	Reset T-type	8
SRTT	Set/reset T-type	8
SYNCHRONOUS COUNTER		
SYNC	Synchronous counter stage	8
REGISTERS / SHIFT REGISTERS		
SHR4	Multibit serial register	30
SHR8	Multibit serial register	54
RSHR4	Multibit serial reg. with reset	30
RSHR8	Multibit serial reg. with reset	54
DREG4	Multibit parallel register	15
DREG8	Multibit parallel register	27
DREGT4	Multibit parallel register with tri-state outputs	25
DREGT8	Multibit parallel register with tri-state outputs	45
INVERTING TRI-STATE BUFFERS		
TRIBUFF	Tristate buffer (enable high)	2
TRIBUFFL	Tristate buffer (enable low)	2
TRINV	Tristate inv buffer (enable high)	2
TRINVL	Tristate inv buffer (enable low)	2
INPUT OUTPUT AND PERIPHERAL CELLS		
TTLIP	TTLIN Non-inverting	
TTLIPN	TTLIN Inverting	
CMOSIP	CMOSIN Non-inverting	
CMOSIPN	CMOSIN Inverting	
CSCHMITT	CMOS Schmitt Non-inverting	
CSCHMITTN	CMOS Schmitt Inverting	
BOP	Buffered Output Non-inverting	
NOP	Buffered Output Inverting	
TRIOUT	Tri-state Output Non-inverting	
TRIOUTN	Tri-state Output Inverting	
BODN	Buffered Open Drain Output Pull Down	
NODN	Inverted Open Drain Output Pull Down	
BODP	Buffered Open Drain Output Pull Up	
NODP	Inverted Open Drain Output Pull Up	
PDOL	Pull Down 25k ohms approx	
PDOH	Pull Down 50k ohms approx	
PUPL	Pull Up 25k ohms approx	
PUPH	Pull Up 50k ohms approx	
POWER SUPPLY PADS		
VDD		
VSS		

MA9000A Sea of Gates

Radiation Hard Advanced Gate Array Design System

Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



GEC PLESSEY

SEMICONDUCTORS

S21502FDS Issue 1.3 November 1990

MACROSOS 1

Radiation Hard Standard Cell Design System

Features

- **Radiation Hard to 1MRad(Si)**
- **High SEU immunity, latch-up free**
- **Double-Level-Metal CMOS/SOS technology**
- **2.5 micron design rules**
- **Typical gate delay 1.2 nS - toggle rates of 70MHz achievable**
- **Comprehensive library of logic cells and logic function building macros**
- **Configurable RAM and ROM macro blocks**
- **3uW/MHz power dissipation per active gate**
- **Extensive CAD design and support system**

General Description

Marconi's Silicon on Sapphire process provides significant advantages over other CMOS technologies. The absence of the bulk silicon substrate reduces parasitic capacitance, giving an improvement in speed and reduction in power consumption. The use of a self-aligning silicon gate gives further improvements in both of the above parameters and achieves higher packing densities. The sapphire substrate also removes the risk of 'latch-up' allowing greater flexibility of use in electrically severe environments, and a significant improvement in radiation hardness.

Double level metal interconnect techniques further enhance the speed capabilities of the MACROSOS 1, and eliminates the possibility of layout dependent timing problems.

The cells in the core area are designed to have a common height, the cell width being dependent on the complexity of the cell. The cell width is the minimum possible although, in some circumstances, this is increased to achieve adequate drive capability. The cells and the interconnect between cells are placed on a regular grid in such a way that design rule infringements are impossible.

A range of standard input and output buffers are available for use in the peripheral areas. These buffers, and the interconnect from them to the core area are placed on the same grid as the core area for the same reason.

The cell layout method eliminates design faults, giving a much better chance of first time success than with other design methodologies. However, the normal constraints of logic design apply. Circuits must be designed with due attention to timing and testability etc. Good digital design techniques combined with the use of our simulation software and cell libraries gives the highest probability of first time design success.

Special cells may be configured by Marconi for non-standard functions. For example, higher output current buffers and special input cells can be designed on request. Marconi's extensive MACROSOS library support covers initial circuit capture to layout including post layout simulation. Schematic capture can be performed with Mentor Graphics' IDEA series or DAZIX capture. Our supported simulation suites include GenRad's HILO Mentor Sim and Daisy Sim; layout is performed using the industry standard Silvar Lisco CALMP suite. Marconi would be pleased to supply the relevant cell libraries to meet your development interface requirements.

CAL-MP is a trademark of Silvar Lisco Inc.
IDEA series is a trademark of Mentor Graphics Corp.
HILO is a trade mark of GenRad Ltd.
DAZIX is a trademark of DAZIX Systems Corporation.

DC Charcteristics and Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0.5	10	V
V_I	Input voltage	-0.3	V_{DD} + 0.3	V
T_A	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Figure 1: Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	3.0	5.0	7.0	V
V_{IH1}	TTL input high voltage	-	2.0	-	-	V
V_{IL1}	TTL input low voltage	-	-	-	0.8	V
V_{IH2}	CMOS input high voltage	-	70	-	-	%V_{DD}
V_{IL2}	CMOS input low voltage	-	-	-	30	%V_{DD}
V_{OH1}	TTL output high voltage	I_{OH} = -2.0mA	4.0	-	-	V
V_{OL1}	TTL output low voltage	I_{OI} = 5.0mA	-	-	0.4	V
V_{OH2}	CMOS output high voltage	I_{OH} = -1mA	90	-	-	%V_{DD}
V_{OL2}	CMOS output low voltage	I_{OI} = 5.0mA	-	-	10	%V_{DD}
I_L	Input leakage current	-	-	-	10	uA
I_{OZ}	Output leakage current	Tristate Output	-	-	10	uA
I_{DD}	Power supply current	-	-	0.1	1	mA

V_{DD} = 5V ± 10%, over full operating temperature range.

Figure 2: Electrical Characteristics

8

AC Characteristics

Cell Name	Function	O/P Edge	Inherent Delay	Per 1pF Load*	Units
C102	CMOS input/output	Rising	0.3	0.2	ns
		Falling	0.3	0.2	
NOR2	2 input NOR	Rising	0.8	5.5	ns
		Falling	0.8	3.6	
RDT	Reset D type	Rising CK - QB	3.8	5.0	ns
		Falling CK - QB	4.4	5.1	
		Data set-up time	2.8	-	
		Data Hold time	0.7	-	

* 1pF is equivalent to fanout of 8 standard gates.

Figure 3: Electrical Characteristics

Propagation Delay

Worst case maximum propagation delays for 5 volts working and 25°C are stated in the cell libraries. These are for the data change or state change which gives the greatest delay. Typical process figures under the same conditions are generally 60% of those listed.

Use the following to predict delays at any other working temperature or voltage:

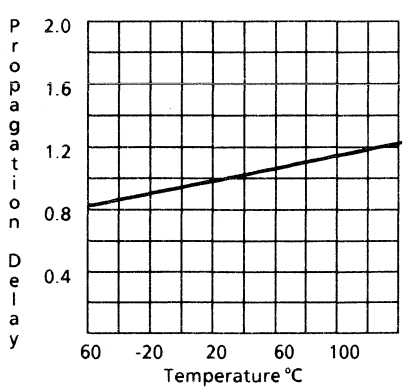


Figure 4: Propagation Delay Vs Temperature

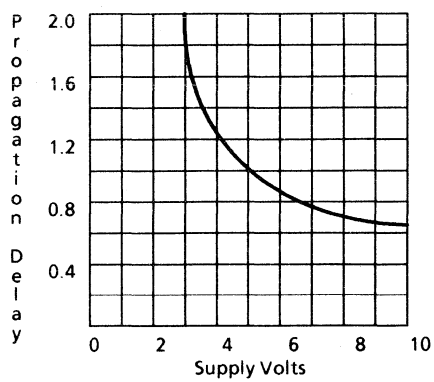


Figure 5: Propagation Delay Vs Supply Voltage

MACROSOS 1

Radiation Hard Standard Cell Design System

GEC PLESSEY

SEMICONDUCTORS

Standard Package Options

Marconi offer a wide range of packages as standard. Other package styles are available. If you require a package not covered on this list, contact Marconi.

Ceramic DIL	24	28	40	48	64	-
Cerdip	24	28	40	48	-	-
Leaded Flatpack	28	42	48	64	84	132
Pin Grid Array	68	84	100	120	144	-
Ceramic LCC	(40)	44	(48)	68	84	-
Cerquad	44	68	84	-	-	-

Figure 6: Standard Package Options

Development Interfaces

All design activities prior to mask creation, including automatic layout may be carried out by the equipment manufacturer, and may be delegated to a Marconi design centre.

The full design package runs on a Vax/11 series system, MicroVax (including Daisy LOGICIAN MicroVax combination), or on Apollo and Mentor workstations. MEDL support for the DAZIX workstation permits schematic entry of data, workfile verification by simulation and the production of the HILO formatted data base required for automatic layout.

Design specific software, including schematic capture and simulation libraries for DAZIX and Mentor workstations, is supplied by Marconi.

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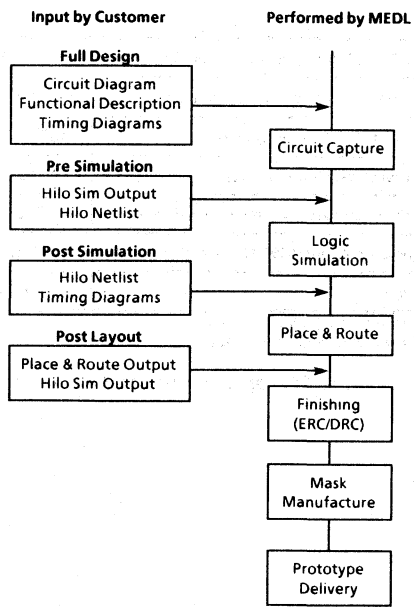


Figure 7: Development Interfaces

8

GEC PLESSEY
SEMICONDUCTORS

MACROSOS 1
Radiation Hard Standard Cell Design System

RadiationTolerance

Total Dose Radiation Testing
For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

Total Dose (Function to specification) note 1	$1x10^{6}$ Rad(Si)
Total Dose (Function to specification) note 2	$3x10^{5}$ Rad(Si)
Transient Upset (stored data loss)	$3x10^{10}$ Rad(Si)/sec
Transient Upset (survivability)	$>10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$1x10^{15}$ neutrons/cm^2
Single Event Upset) (GSO 10% worst case)	$<10^{-10}$ errors/bitday
Latch-up	Not possible

1. Circuits with all CMOS type inputs.
2. Circuits with all TTL type inputs.

Table 8: Radiation Hardness Parameters

LSI Macros

Memory
- Configurable static RAM and ROM.

Bit Slice Elements
- 4 bit Microprocessor Slice
- 4 bit Sequencer
- 12 bit Microprogram Controller
- Status and Shift Control Units
- DMA Address Generator

Microprocessor Peripherals
- Parallel Peripheral Interface
- Programmable Communications Interface
- DMA Controller

Interface Family
- Memory Error Detector and Corrector
- Manchester Encoder / Decoder
- Octal Latches
- Octal Buffers
- Octal Tranceivers
- Address Decoders

For more information on LSI Macros and additions to the family contact our nearest office.

GEC PLESSEY
SEMICONDUCTORS

Cell Library Quick Guide

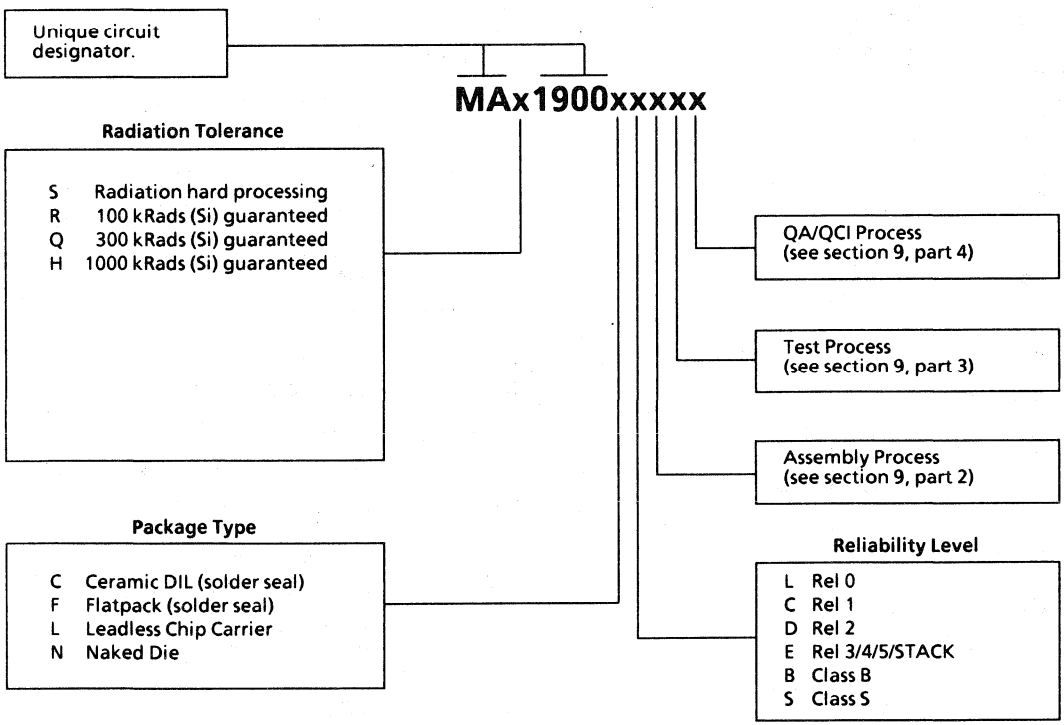
Cell Name	Function	Cell Units
COMBINATIONAL GATES		
INV	Inverter	1
DUALINV	Dual inverter	1
INVB	Fast inverter	1
INVC	Super fast inverter	2
BUFF	Non-inverting buffer	1
BUFFB	Fast non-inverting buffer	2
BUFFC	Super fast non-inverting buffer	3
NAND2	2 input NAND	1
NAND2B	Fast 2 input NAND	2
NAND3	3 input NAND	2
NAND4	4 input NAND	2
AND2	2 input AND	2
AND3	3 input AND	2
AND4	4 input AND	3
NOR2	2 input NOR	1
NOR2B	Fast 2 input NOR	2
NOR3	3 input NOR	2
NOR4	4 input NOR	2
OR2	2 input OR	2
OR3	3 input OR	2
OR4	4 input OR	3
ANDNOR	2 + 2 input AND/NOR	2
ANDOR	2 + 2 input AND/OR	3
ORNAND	2 + 2 OR/NAND	2
ORAND	2 + 2 OR/AND	3
EXNOR	Exclusive NOR	3
EXORN	Exclusive OR	3
SEL2INV	Select 1 of 2 (inverting)	3
SEL2	Select 1 of 2	3
SEL4INV	4 bit data selector (inverting)	6
SEL4	4 bit data selector	7
ARITHMETIC		
HAD	Half adder	4
FAD	Full adder	7
FLAD	Fast look ahead adder	6
LAH2	2 bit look ahead unit	10
LAH3	3 bit look ahead unit	14
LAH4	4 bit look ahead unit	24
SIMPLE LATCHES		
NASR	NAND set reset-latch	3
NOSR	NOR set-reset latch	3
CLOCKED LATCHES		
DL	D-latch (Active low)	4
DLH	D-latch (Active high)	4
SDL	Set D-latch	4
RDL	Reset D-latch	4
SRDL	Set/reset D-latch	5

Cell Name	Function	Cell Units
MASTER-SLAVE FLIP-FLOPS		
DT	D-type	6
D2T	Dual input D-type	8
SDT	Set D-type	7
RDT	Reset D-type	7
SRDT	Set/reset D-type	8
TOGGLE FLIP-FLOPS		
STT	Set T-type	7
RTT	Reset T-type	7
SRTT	Set/reset T-type	8
SYNCHRONOUS COUNTER		
SYNC	Synchronous counter stage	10
REGISTERS / SHIFT REGISTERS		
SHRx	Multibit (x = 2-8) serial register	16-46
RSHRx	Multibit (x = 2-8) serial reg. with reset	24-54
DREGx	Multibit parallel register (x = 2-8)	8-26
DREGTx	Multibit parallel register (x = 2-8) with tri-state outputs	10-34
HPLSx	Half parallel loading shift registers (x = 2-8)	22-64
INVERTING TRI-STATE BUFFERS		
TRIBUFF	Tristate buffer (enable high)	2
TRIBUFFL	Tristate buffer (enable low)	2
TRINV	Tristate inv. buffer (enable high)	2
TRINVL	Tristate inv. buffer (enable low)	2
INPUT OUTPUT AND PERIPHERAL CELLS		
DIP	Direct input (protection cicuit only)	
PUP	Pull up (approx 35 Kohms)	
PDO	Pull down (approx 35 Kohms)	
TSCHMITT	TTL compatible Schmitt	
CSCHMITT	CMOS compatible Schmitt	6
CMOSIN	CMOS buffer (non-inverting)	5
TTLIN	TTL buffer (non-inverting)	2
NOP	Push/pull output buffer (inverting)	3
WNOP	Multiple NOP	
BOP	Push/pull output buffer (non-inverting)	
ZOP	Tri-state output buffer	
ODN	Open drain output pull down	
ODP	Open drain output pull up	
TRIOP	Tristate I/O buffer	4
BUSINT	Bus interface	6
STEPUP	Output Buffer	
POWER SUPPLY PADS		
VDD	V_{DD} pad	
VSS	V_{SS} pad	

MACROSOS 1
Radiation Hard Standard Cell Design System

Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



GEC PLESSEY

SEMICONDUCTORS

S21300FDS Issue 1.1 November 1990

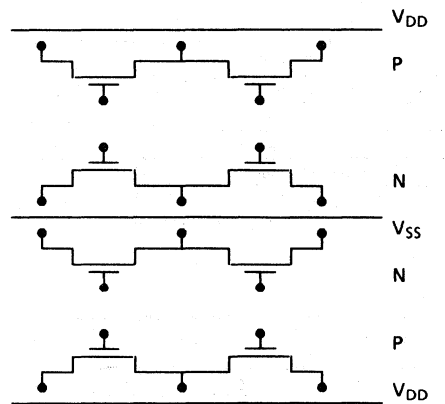
MA9000 Series

Silicon-on-Sapphire Radiation Hard Gate Arrays

Features

- **Radiation Hard to 1MRad(Si)**
- **High SEU immunity, latch-up free**
- **Double-Level-Metal CMOS/SOS Technology**
- **2.5 micron design rules**
- **Typical gate delay 1.2 nS with 2 loads, 60MHz toggle speeds**
- **Comprehensive library of logic cells and logic function building macros**
- **100% automatic place and route for up to 90% utilisation**

Cell Unit



General Description

The logic building block for the Marconi double level metal CMOS/SOS gate arrays is a four transistor 'cell-unit' equivalent in size to a 2 input NAND gate. Back to back cell-units as illustrated, organised in rows, form the core of the array.

The interconnection patterns that cause groups of cell-units within a row, to become defined logic cells, and the models which are used to simulate these cells, are stored as software in LIBRARIES. Cells up to the complexity of, say, multiple bit shift registers are treated in this way.

Higher complexity functions are described by MACROS as the interconnection of defined cells. Macros are 'hard', 'soft', or 'firm' according to the constraints that are applied to the distribution of the component cells within the array and whether the full function is simulated by a model or by the additive effects of the component cells.

Array Options

Array type	Cell units	Bonding pads Total	I/O	Power
MA9007	748	48	46	2
MA9024	2484	84	80	4
MA9040	4048	106	102	4

Each cell-unit is equivalent to a 2 input NAND gate.

Any I/O site may be configured as a power pad to give flexible bonding options, but to standardise testing preffered positions exist.

8

DC Charcteristics and Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0.5	10	V
V_I	Input voltage	-0.3	V_{DD} + 0.3	V
T_A	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Figure 1: Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	3.0	5.0	7.0	V
V_{IH1}	TTL input high voltage	-	2.0	-	-	V
V_{IL1}	TTL input low voltage	-	-	-	0.8	V
V_{IH2}	CMOS input high voltage	-	70	-	-	%V_{DD}
V_{IL2}	CMOS input low voltage	-	-	-	30	%V_{DD}
V_{OH1}	TTL output high voltage	I_{OH} = -2.0mA	4.0	-	-	V
V_{OL1}	TTL output low voltage	I_{OL} = 5.0mA	-	-	0.4	V
V_{OH2}	CMOS output high voltage	I_{OH} = -1mA	90	-	-	%V_{DD}
V_{OL2}	CMOS output low voltage	I_{OL} = 5.0mA	-	-	10	%V_{DD}
I_L	Input leakage current	-	-	-	10	uA
I_{OZ}	Output leakage current	Tristate Output	-	-	10	uA
I_{DD}	Power supply current	-	-	0.1	1	mA

V_{DD} = 5V ± 10%, over full operating temperature range.

Figure 2: Electrical Characteristics

AC Characteristics

Cell Name	Function	O/P Edge	Inherent Delay	Per 1pF Load*	Units
C102	CMOS input/output	Rising	0.3	0.2	ns
		Falling	0.3	0.2	
NOR2	2 input NOR	Rising	0.8	5.5	ns
		Falling	0.8	3.6	
RDT	Reset D type	Rising CK - QB	3.8	5.0	ns
		Falling CK - QB	4.4	5.1	
		Data set-up time	2.8	-	
		Data Hold time	0.7	-	

* 1pF is equivalent to fanout of 8 standard gates.

Figure 3: Electrical Characteristics

Propagation Delay

Worst case maximum propagation delays for 5 volts working and 25°C are stated in the cell libraries. These are for the data change or state change which gives the greatest delay. Typical process figures under the same conditions are generally 60% of those listed.
Use the following to predict delays at any other working temperature or voltage:

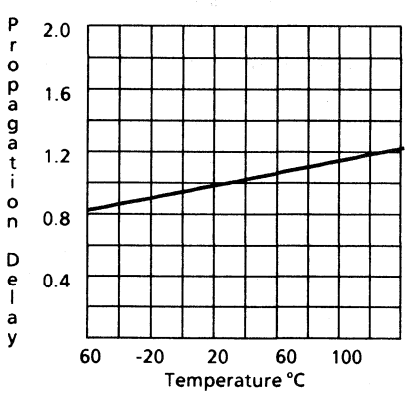


Figure 4: Propagation Delay Vs Temperature

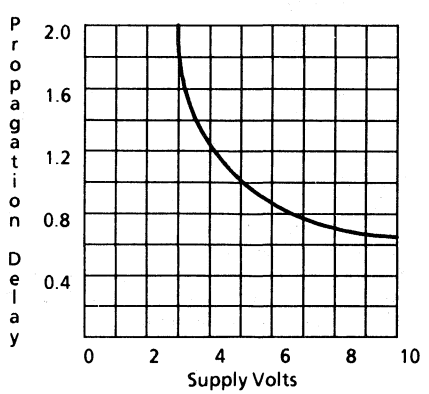


Figure 5: Propagation Delay Vs Supply Voltage

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Silicon-on-Sapphire Radiation Hard Gate Arrays

GEC PLESSEY
SEMICONDUCTORS

Package Options

	MA9007	MA9024	MA9040
DIL 14	X		
DIL 16	X		
DIL 20	X		
DIL 24	X	X	
DIL 28	X	X	
DIL 40	X	X	
DIL 48	X	X	X
DIL 64		X	X
LCC 28	X		
LCC 40	X	X	
LCC 44	X		
LCC 48	X	X	X
LCC 68		X	X
LCC 84		X	X
FPK 14	X		
FPK 16	X		
FPK 20	X		
FPK 24	X	X	
FPK 28	X	X	
FPK 42	X	X	
FPK 48	X	X	
FPK 64		X	X
FPK 80		X	X
PGA 68		X	X
PGA 84		X	X
PGA 120		X	X
PGA 144		X	X

DIL = Dual in line
LCC = Leadless chip carrier
FPK = Leaded flatpack
PGA = Pin grid array
These are standard packages. If your package requirement is not shown above, discuss other options with a Marconi applications engineer.

RadiationTolerance

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

Total Dose (Function to specification) note 1	$1x10^{6}$ Rad(Si)
Total Dose (Function to specification) note 2	$3x10^{5}$ Rad(Si)
Transient Upset (stored data loss)	$3x10^{10}$ Rad(Si)/sec
Transient Upset (survivability)	$>10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$1x10^{15}$ neutrons/cm^{2}
Single Event Upset) (GSO 10% worst case)	$<10^{-10}$ errors/bitday
Latch-up	Not possible

1. Circuits with all CMOS type inputs.
2. Circuits with all TTL type inputs.

Table 8: Radiation Hardness Parameters

MA9000 Series

Silicon-on-Sapphire Radiation Hard Gate Arrays

GEC PLESSEY
SEMICONDUCTORS

Cell Library Quick Guide

Cell Name	Function	Cell Units
COMBINATIONAL GATES		
INV	Inverter	1
DUALINV	Dual inverter	1
INVB	Fast inverter	1
INVC	Super fast inverter	2
BUFF	Non-inverting buffer	1
BUFFB	Fast non-inverting buffer	2
BUFFC	Super fast non-inverting buffer	3
NAND2	2 input NAND	1
NAND2B	Fast 2 input NAND	2
NAND3	3 input NAND	2
NAND4	4 input NAND	2
AND2	2 input AND	2
AND3	3 input AND	2
AND4	4 input AND	3
NOR2	2 input NOR	1
NOR2B	Fast 2 input NOR	2
NOR3	3 input NOR	2
NOR4	4 input NOR	2
OR2	2 input OR	2
OR3	3 input OR	2
OR4	4 input OR	3
ANDNOR	2 + 2 input AND/NOR	2
ANDOR	2 + 2 input AND/OR	3
ORNAND	2 + 2 OR/NAND	2
ORAND	2 + 2 OR/AND	3
EXNOR	Exclusive NOR	3
EXORN	Exclusive OR	3
SEL2INV	Select 1 of 2 (inverting)	3
SEL2	Select 1 of 2	3
SEL4INV	4 bit data selector (inverting)	6
SEL4	4 bit data selector	7
ARITHMETIC		
HAD	Half adder	4
FAD	Full adder	7
FLAD	Fast look ahead adder	6
LAH2	2 bit look ahead unit	10
LAH3	3 bit look ahead unit	14
LAH4	4 bit look ahead unit	24
SIMPLE LATCHES		
NASR	NAND set reset-latch	3
NOSR	NOR set-reset latch	3
CLOCKED LATCHES		
DL	D-latch (Active low)	4
DLH	D-latch (Active high)	4
SDL	Set D-latch	4
RDL	Reset D-latch	4
SRDL	Set/reset D-latch	5

Cell Name	Function	Cell Units
MASTER-SLAVE FLIP-FLOPS		
DT	D-type	6
D2T	Dual input D-type	8
SDT	Set D-type	7
RDT	Reset D-type	7
SRDT	Set/reset D-type	8
TOGGLE FLIP-FLOPS		
STT	Set T-type	7
RTT	Reset T-type	7
SRTT	Set/reset T-type	8
SYNCHRONOUS COUNTER		
SYNC	Synchronous counter stage	10
REGISTERS / SHIFT REGISTERS		
SHRx	Multibit (x = 2-8) serial register	16-46
RSHRx	Multibit (x = 2-8) serial reg. with reset	24-54
DREGx	Multibit parallel register (x = 2-8)	8-26
DREGTx	Multibit parallel register (x = 2-8) with tri-state outputs	10-34
HPLSx	Half parallel loading shift registers (x = 2-8)	22-64
INVERTING TRI-STATE BUFFERS		
TRIBUFF	Tristate buffer (enable high)	2
TRIBUFFL	Tristate buffer (enable low)	2
TRINV	Tristate inv. buffer (enable high)	2
TRINVL	Tristate inv. buffer (enable low)	2
INPUT OUTPUT AND PERIPHERAL CELLS		
DIP	Direct input (protection cicuit only)	
PUP	Pull up (approx 35 Kohms)	
PDO	Pull down (approx 35 Kohms)	
TSCHMITT	TTL compatible Schmitt	
CSCHMITT	CMOS compatible Schmitt	6
CMOSIN	CMOS buffer (non-inverting)	5
TTLIN	TTL buffer (non-inverting)	2
NOP	Push/pull output buffer (inverting)	3
WNOP	Multiple NOP	
BOP	Push/pull output buffer (non-inverting)	
ZOP	Tri-state output buffer	
ODN	Open drain output pull down	
ODP	Open drain output pull up	
TRIOP	Tristate I/O buffer	4
BUSINT	Bus interface	6
STEPUP	Output Buffer	
POWER SUPPLY PADS		
VDD	V_{DD} pad	
VSS	V_{SS} pad	

8

MA9000 Series

Silicon-on-Sapphire Radiation Hard Gate Arrays

Macros

The following Macros are included in the MA9000 library. Marconi is constantly adding new Macros to the library, please contact our nearest office for information on the latest additions.

Macro name	Macro name
ACOUNTn	Asynchronous counters
ALU4	ALU
GCOUNTn	Gray counters
JCOUNTn	Johnson counters
LADDn	Lookahead adders
MCOMPn	Magnitude comparators
PARITYn	Parity detectors
RADDn	Ripple carry adders
SEL8	Select 1 of 8
SEL16	Select 1 of 16
M2901	4 bit slice microprocessor
M2909	4 bit microprogram controller
M2902	Look ahead carry unit
M2910	12 bit microprogram sequencer
M2918	Pipeline register

Development Interfaces

All design activities prior to mask creation, including automatic layout may be carried out by the equipment manufacturer, or may be delegated to a Marconi design centre.

The full design package runs on a Vax/11 series system, MicroVax (including Daisy LOGICIAN MicroVax combination), or on Apollo and Mentor workstations. Other workstations, which include Daisy or Valid, permit schematic entry of data, workfile verification by simulation and the production of the HILO formatted data base required for automatic layout.

Design specific software, including schematic capture and simulation libraries for Daisy and Mentor workstations, is supplied by Marconi.

Connection to the Marconi design centre via an X25 protocol or similar telephone link or the use of terminals within a Marconi 'design shop' are other possible options which permit a customer to participate in design activities without involvement in major capital outlay.

Training courses that cover all aspects of design and cater for different levels of starting experience are run at the Marconi Wembley Design centre. Some of these courses may be combined with 'design shop' activities.

Apollo is a trademark of Apollo Computers Ltd.

Daisy is a trademark of Daisy Systems Corporation.

HILO is a trademark of GenRad Ltd.

Valid is a trademark of Valid Logic Systems, Inc.

VAX is a trademark of Digital Equipment Corporation.

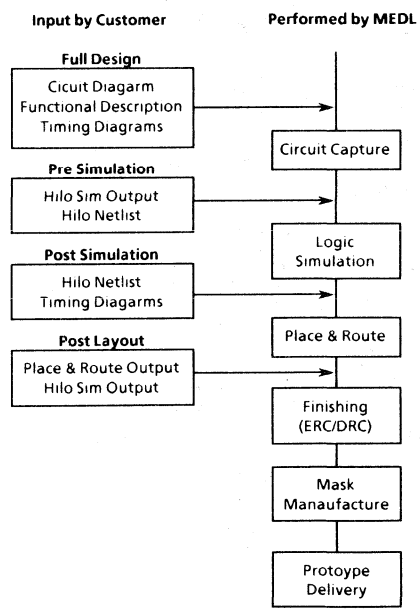
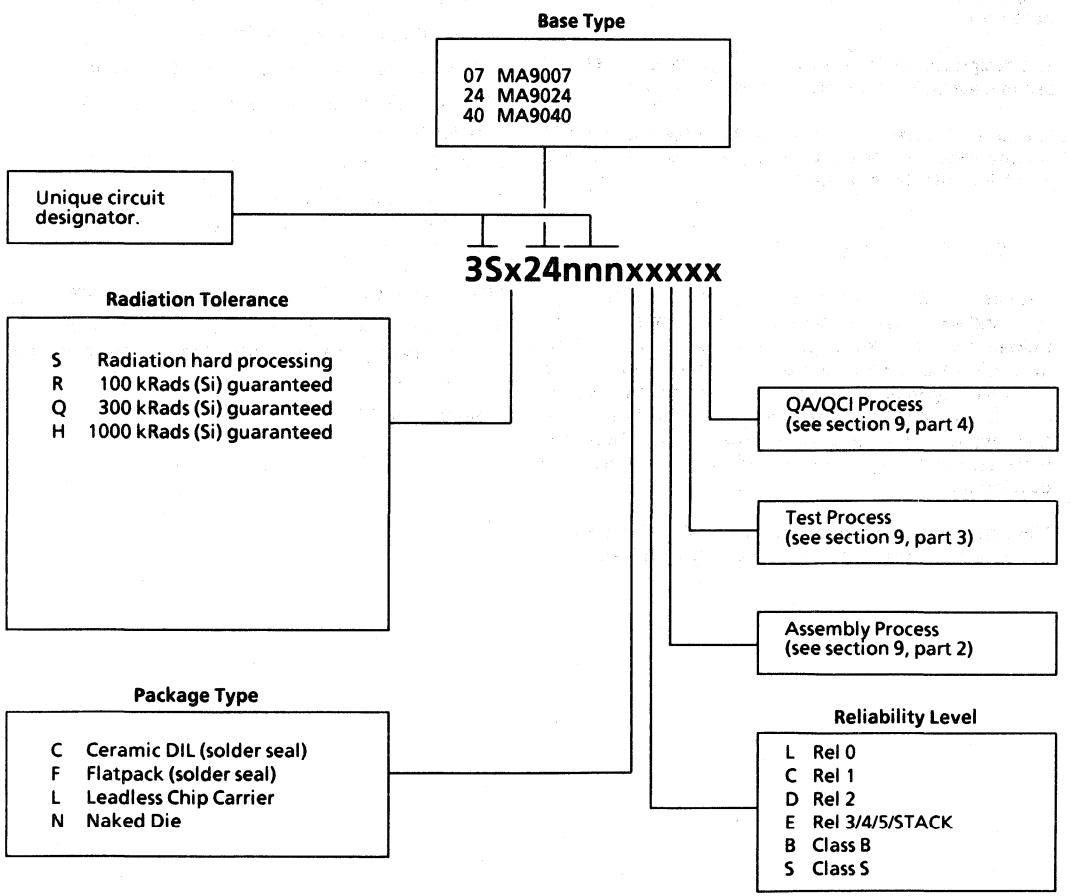


Figure 7: Development Interfaces

Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.



CAD Support

Marconi Electronic Devices support VAX, APOLLO and DAISY platforms for design entry, and GenRad HILO, Mentor Graphics' QUICKSIM and Daisy DLS for logic simulation of SOS ASIC designs.

MEDL's own software (MARRS) is used to layout SOS gate array designs; SILVAR-LISCO's SC2 is used for the layout of standard cell designs and designs to be implemented on MEDL's Sea of Gates utilise layout software. Mentor Graphics' CHIPGRAPH is used for editing layouts when necessary.

The design routes used for gate array, standard cell and Sea of Gate SOS designs are illustrated in figure 1.

The SOS ASIC design routes are the subject of a MEDL Quality Assurance specification, (spec. number RG 001) which is available on request.

The Design Interface

It is possible for customers with the appropppriate design tools and ASIC design experience to perform some of the tasks in the design route, for example schematic capture, simulation and even layout of SOS designs. The point in the design cycle at which the customer hands the design data over to MEDL is called the 'Design Interface'. MEDL field application engineers are available to discuss the most appropriate design interface for a particular development.

The design interfaces supported by MEDL are illustrated in figure 2 and are described in the sections following.

Design Interface 1 - FULL DESIGN INTERFACE

The customer provides a full requirement specification and MEDL perform all design functions from schematic capture to the production of tested samples.

A summary of the deliverables expected from the two parties when using this interface point follows:

The customer shall provide MEDL with the following:

- Target functional specification, including block diagrams and circuit diagrams where avialble.
- Inspection/screening requirements.
- Required package type, and pinout if known.
- Envoronmental specification (supply voltage, temperature range etc.).
- Interface specification (e.g. CMOS/TTL output drive).
- Timing requirements(e.g. maximum clock speed, critical paths, with timing diagarms where appropriate).

MEDL shall provide the customer with the following:

- Fully tested samples of the device using a pinout previously agreed with the customer if not originally specified.
- Colour plot of ASIC.

Design Interface 2 - POST SIMULATION INTERFACE

The customer performs schematic capture and simulation and passes 'fault free' design file (HILO netlist) to MEDL. MEDL then perform the layout, supplying track capacitance data to the customer for post layout simulation. When a successful post layout simulation has been performed, MEDL take the design to the production of tested samples.

A summary of the deliverables expected from the two parties when using this interface point follows:

The customer shall provide MEDL with the following:

- Circuit description file in HILO3 format (HILO netlist).
- Test vectors in Fairchild format.
- Procurement specification.
- Circuit diagram
- Target Pinout.
- MENTOR/DAISY design tree, i.e. complete hierarchical design (optional).
- Timing information (including critical paths).

MEDL shall provide the customer with the following:

- Track capacitance file (to enable the customer to perform post-layout simulation), Mentor route only.
- Tested samples of the device.
- Colour plot of ASIC.

Design Interface 3 - POST LAYOUT INTERFACE

The customer performs schematic capture, simulation and layout. MEDL carries out design checks, produces the PG tape and masks, and finally the tested samples.

A summary of the deliverables expected from the two parties when using this interface point follows:

The customer shall provide MEDL with the following:

- Circuit description file in HILO3 format (HILO netlist).
- Test vectors in Fairchild format.
- Procurement specification.
- Circuit diagram.
- GDSII layout file.
- Target Pinout.
- MENTOR/DAISY design tree, i.e. complete hierarchical design (optional).
- Timing information (including critical paths).
- Bonding diagram.

MEDL shall provide the customer with the following:

- Tested samples of the device.
- Colour plot of ASIC.

Quality Assurance Procedures

It is obviously necessary to clearly define the respective responsiblities of the customer and MEDL inthe case of each design interface. This is defined initially in a design work statement completed jointly by both parties. The subsequent monitoring of the development project is a subject of a MEDL Quality Assurance document QAP 014E, and entail a number of design reviews at defined stages (control points) of the project. The completed control point forms, form a record of development progress. Both the QAP 014E document and the associated QAP 014 forms are available on request.

SOS ASIC Design Routes

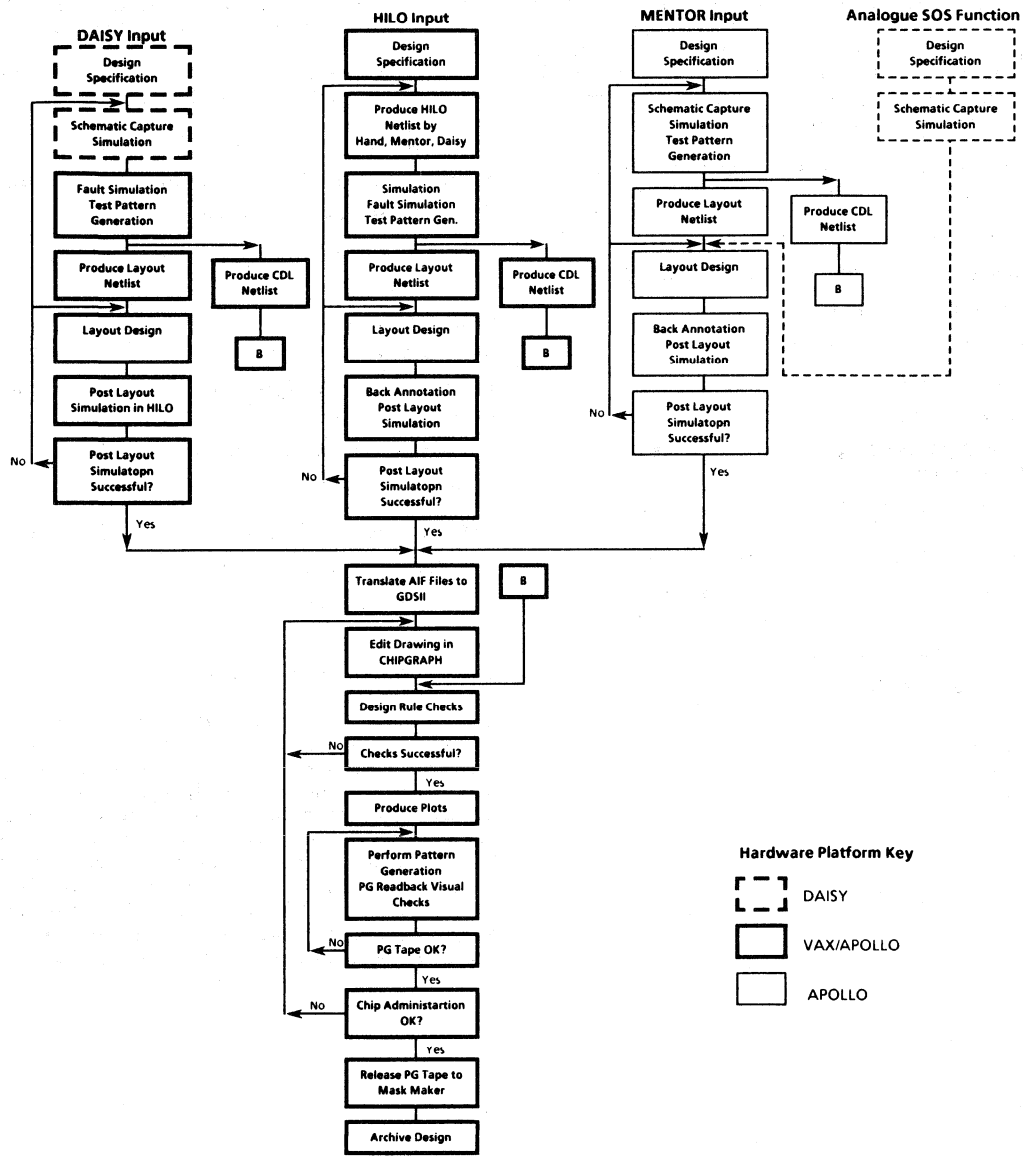


Figure 1: SOS ASIC Design Routes

SOS ASIC Design Interfaces

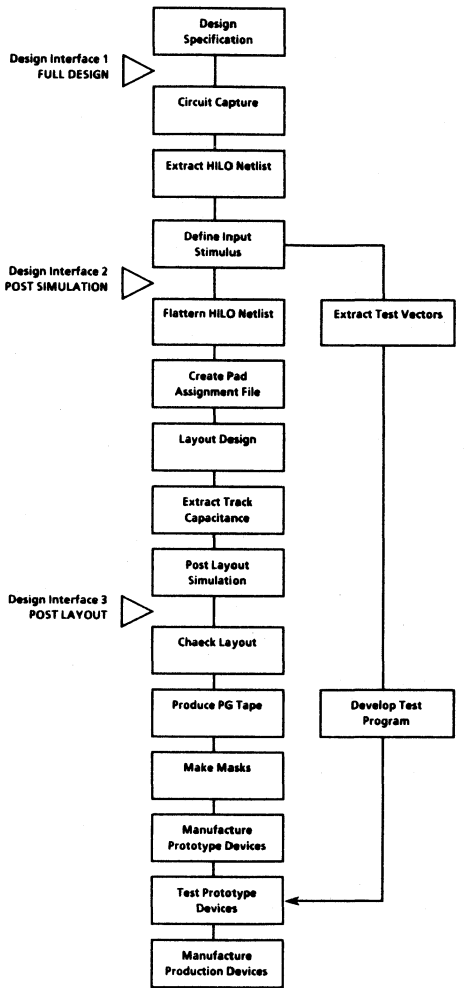


Figure 2: SOS ASIC Design Interfaces

GEC PLESSEY

SEMICONDUCTORS

C11200FDS Issue 1.1 December 1990

MA6561

High Speed 8 Bit Flash Analog-to-Digital Converter

(Preliminary Data)

Features

- **CMOS Silicon-on-Sapphire**
- **50MHz sample rate**
- **Low input capacitance**
- **8 bit tri-state data output with overflow bit**
- **± 0.5 LSB accuracy typical**
- **Single 5V supply voltage**
- **2 devices cascadable for 9 bit output**
- **2 devices paralleled for double sample rate**

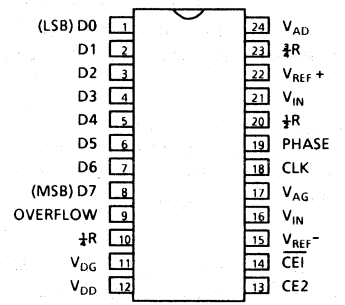
General Description

The MA6561 is a high speed CMOS SOS analog-to-digital converter which uses a full-flash pipelined architecture to provide high conversion rates with low input capacitance. This device is functionally compatible with the RCA part CA3318.

The overflow bit makes possible the connection of two converters in series. This produces a 9 bit high speed converter increasing the resolution of the conversion system. The tri-state data outputs allow two MA6561 devices to be connected in parallel so that the sample rate can be doubled by taking samples from alternate devices.

The MA6561 operates with input voltages between 0V and 5V and a full scale range between 1V and 3V. The power consumption depends on the clock frequency and is typically 845mW with a 2V input voltage range at a conversion rate of 50 MSamples/s.

Pin Out (Figure 1)



V_{DD}	Digital positive supply
V_{DG}	Digital ground
V_{AD}	Analog positive supply
V_{AG}	Analog ground
V_{IN}	Analog input voltage
V_{REF} +	Positive voltage reference
V_{REF} -	Negative voltage reference
¼R, ¼R, ¼R	Reference resistor taps
CLK	Clock input
D0-D7	Digital data outputs (D7 most significant)
OVERFLOW	Overflow ($V_{IN} > V_{REF}$ +)
$\overline{PHASE}$	Clock phase select
$\overline{CE1}$,CE2	Chip select inputs

Applications

The high conversion rate makes the MA6561 suited for applications such as video signal digitising, high speed digitising oscilloscopes, high speed digital signal processing and high performance hybrid analog-to-digital conversion systems.

8

High Speed 8 Bit Flash Analog-to-Digital Converter
(Preliminary Data)

Operation

The MA6561 analog-to-digital converter is based on a pipelined full-flash technique which results in very high speed performance.

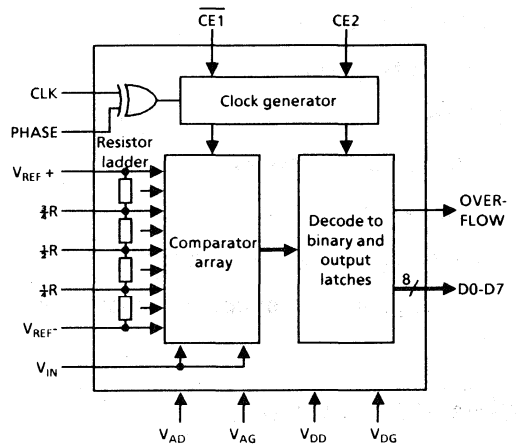
Figure 2 shows the block diagram of the MA6561. The comparator array effectively consists of 256 comparators which simultaneously compare the input voltage with 256 reference levels which are generated by an on-chip resistor ladder.

With the PHASE input low, the analog input voltage is compared with the 256 reference levels on the falling edge of the clock. A 256 level thermometer code is generated and the final result is decoded to an 8 bit binary word and latched. The pipelining used to maximise throughput results in a sample-to-data out delay of five clock periods as shown in Figure 3.

Both ends of the reference string should be driven by external voltage references to define the converter zero and full scale levels. The reference resistor ladder is tapped at three points to allow decoupling and external trimming to maximise integral linearity.

The tri-state data outputs are controlled by chip enable inputs. For D0 to D7 to be enabled, $\overline{CE1}$ must be low and CE2 must be high. The OVERFLOW output only requires CE2 to be high to be enabled. This scheme is used to facilitate the cascading of devices.

Block Diagram (Figure 2)



The PHASE input is provided to allow the operation of the converter to be defined by the rising or the falling edge of the clock. This facility is incorporated to allow two MA6561s to be operated in parallel on different clock phases for double speed operation.

The OVERFLOW output goes high when the analog input voltage exceeds the $V_{REF}+$ level. This can be used as an error signal or to enable a second MA6561 and generate a ninth bit when two MA6561s are cascaded for 9 bit operation.

MA6561

High Speed 8 Bit Flash Analog-to-Digital Converter
(Preliminary Data)

Pin Description

CLK
Clock input. With the PHASE input logic low, the falling edge of the clock defines the point at which the analog input level is converted.

PHASE
Clock phase input. The CLK input is Exclusive-ORed with the PHASE input to allow the converter operation to be defined by either the rising or falling edge of the clock. With PHASE logic low, the analog input is converted on the falling edge of the clock.

D0-D7
Digital data outputs - D0 is the least significant bit with D7 the most significant bit. The data outputs are tri-state and are enabled with $\overline{CE1}$ logic low and CE2 logic high. Valid data for a specific sample is available five full clock cycles after the analog value was sampled.

OVERFLOW
The OVERFLOW output goes high when the analog input voltage exceeds the $V_{REF}+$ level.

$\overline{CE1}$, CE2
Chip enable inputs. D0-D7 and OVERFLOW outputs are enabled as shown in the table below:

$\overline{CE1}$	CE2	D0-D7	OVERFLOW
0	0	Hi-Z	Hi-Z
0	1	Outputs	Output
1	0	Outputs	Illegal output
1	1	Hi-Z	Output

V_{IN}
Analog inputs. The analog inputs are sampled on each clock cycle and converted to an 8 bit value which is available at the data outputs after five full clock cycles.

To achieve high accuracy at high speed, V_{IN} must be driven by a low impedance to ensure that the input settles to within one least significant bit between conversions.

The two analog inputs should be tied together externally.

$V_{REF}+$
Positive voltage reference input, used to define the full scale analog input level.

$V_{REF}-$
Negative voltage reference input, used to define the zero analog input level. In many applications, $V_{REF}-$ may be connected to analog ground.

$\frac{3}{4}R$, $\frac{1}{2}R$, $\frac{1}{4}R$
Reference resistor ladder taps which are pinned out for decoupling. They can also be driven by external reference drivers to improve the integral linearity of the converter.

V_{AD}
Analog positive supply.

V_{AG}
Analog ground.

V_{DD}
Digital positive supply.

V_{DG}
Digital ground.

MA6561

High Speed 8 Bit Flash Analog-to-Digital Converter

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GEC PLESSEY

SEMICONDUCTORS

Absolute Maximum Ratings (Table 1)

Parameter	Minimum	Maximum	Units
Analog supply Voltage V_{AD}-V_{AG}	-0.3	7	V
Digital supply Voltage V_{DD}-V_{DG}	-0.3	7	V
Digital input Voltage	V_{DG}-0.3	V_{DD} + 0.3	V
Operating Temperature	-55	125	°C
Storage temperature	-55	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics (Table 2)

Parameter	Minimum	Typical	Maximum	Units
Operating Supply Voltage (over full temperature range)	4.5	5.0	5.5	V
DC Power Dissipation	-	325	-	mW
AC Power Dissipation		10.4		mW/MHz
Resolution	-	8	-	Bits
Integral Linearity (note 2)	-	±0.5	±1	LSB
Differential Linearity	-	±0.25	±0.5	LSB
Bandwidth (note 3)	-	6.6	-	MHz
Offset Error	-10	-	10	mV
Gain Error	-	1.5	-	LSB
Full Scale Range, V_{REF} + minus V_{REF}- (note 4)	1.0	2.0	3.0	V
Input Voltage Range	0	2.0	5.0	V
Positive Reference Voltage, V_{REF} +	1.0	3.5	5.0	V
Negative Reference Voltage, V_{REF}-	0.0	1.5	4.0	V
V_{IN} Capacitance	-	14	-	pF
V_{IN} Source Resistance	0	25	50	Ω
Reference resistor ladder Impedance	-	268	-	Ω
Conversion Rate	40	50	60	MSamples/s
Minimum Clock High or Clock Low Time	-	7	-	ns
Minimum Clock Frequency (note 5)	-	0.5	10	MHz

Notes:

1 Except where otherwise stated, test conditions are as follows:

Temperature	25°C.
V_{DD}, V_{AD}	5 V.
V_{REF} +	3.5V.
V_{REF}-	1.5V.
V_{IN} source resistance	50Ω
F_{CLK}	10MHz, 50% duty cycle

2 Without external midpoint trim. Integral linearity is ± 0.5 LSB maximum with trim.

3 For 0.5 LSB maximum additional error on a full scale input sinewave. 3dB point is typically 85MHz. The typical figure quoted is for CLK_{HIGH} = 10ns and CLK_{LOW} = 90ns.

4 Maximum bandwidth and sampling rate depend on full scale range.

5 The typical value is at 25°C. The maximum value of 10MHz clock frequency is for operation at 75°C Full characterisation has yet to be carried out above this temeperature.

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High Speed 8 Bit Flash Analog-to-Digital Converter
(Preliminary Data)

Timing Diagrams

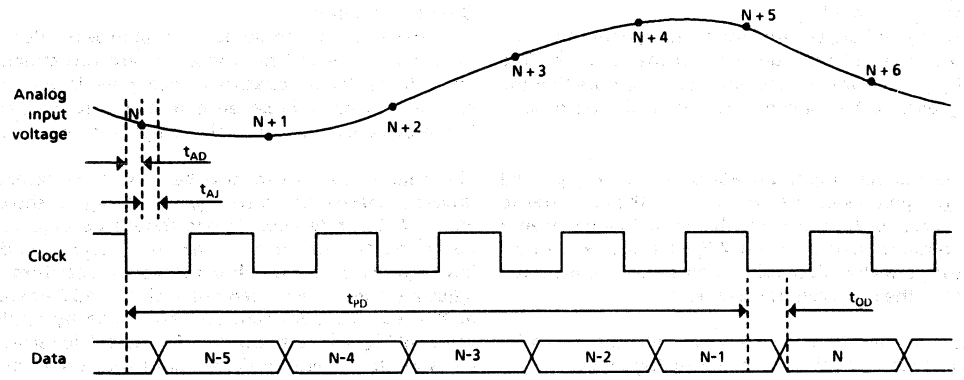

Figure 3 - General Timing Diagram (Phase = 0)

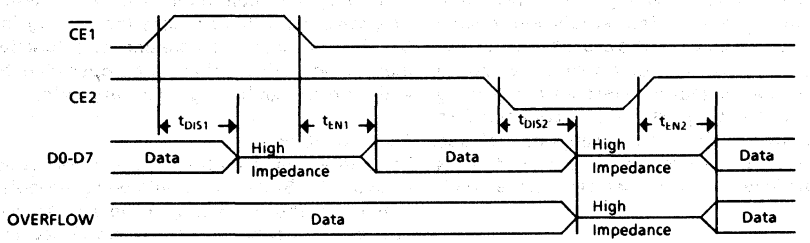

Figure 4 - Output enable timing diagram

Parameter	Typical	Units
V_{IN} Aperture delay, t_{AD}	12.2	ns
V_{IN} Aperture jitter, t_{AJ}	<24	ps
Data/overflow pipeline delay, t_{PD}	5	Clock cycles
Data/overflow output delay (2) (to valid logic threshold) t_{OD}	38	ns
CEI (bar) to data disable, t_{DIS1}	25	ns
CEI (bar) to data enable, t_{EN1} (2) (to valid logic threshhold)	25	ns
CE2 to data/overflow disable, t_{DIS2}	32	ns
CE2 to data/overflow enable, t_{EN2} (2) (to valid logic threshhold)	33	ns

Table 3. General Timing Figures

High Speed 8 Bit Flash Analog-to-Digital Converter
(Preliminary Data)

Application Details

Grounding / Decoupling
The analog and digital grounds of the system should be kept separate and only connected at the converter. The use of ground planes is recommended to ensure that the analog data to be converted is free of digital ground noise.

Reference drivers, input amplifiers, reference taps, and the V_{AD} supply should be decoupled at the converter to analog ground. All capacitors should be low impedance 100nF ceramics in parallel with 4.7µF tantalum capacitors to ensure effective decoupling and should be mounted as close to the converter as possible.

If V_{AD} is derived from V_{DD}, a small inductor should be used to reduce digital noise on the analog supply.

Application circuit
Figure 5 shows a typical application with the MA6561 functioning as a high performance 8 bit high speed data acquisition front-end. $V_{REF}+$ and $V_{REF}-$ are derived from a single 2.5V voltage reference. Emitter followers driving the V_{REF} inputs ensure that current is available for a large full scale range. The reference driver circuitry can be simplified if the input signal is referenced to analog ground, in which case $V_{REF}-$ should be connected to analog ground. Decoupling of the supplies, voltage reference inputs and reference resistor ladder is important to achieve full 8 bit performance at high speed.

Offset and gain trims
Offset correction should be carried out in the pre-amp circuitry by introducing a DC shift to V_{IN} or by adjusting the op-amp offset trim. The trim should be carried out by applying the input voltage that corresponds to the first code transition and trimming until the transition is observed.

The gain trim should also be carried out in the pre-amp circuitry by introducing a gain adjustment. When this is not possible, an adjustment to the reference voltage should be made.

To achieve gain trim, first adjust offset trim as above and then set V_{IN} to full scale. Following this, adjust the pre-amp gain or $V_{REF}+$ until the OVERFLOW output goes logic high.

Quarter point trims
The quarter points should be decoupled with 100nF low inductance ceramic (chip capacitors are recommended) and 4.7µF tantalum capacitors. Decoupling is required to reduce the dynamic impedance of the resistor ladder and becomes more important as the sample rate is increased.

The quarter points can also be driven by reference drivers connected between $V_{REF}+$ and $V_{REF}-$ as shown in Figure 4. The reference drivers should be adjusted to compensate for non-linearities introduced by inaccuracies in the on-chip reference resistors The adjustment must be carried out with the ADC operating at the required clock rate and are made by applying values of V_{IN} that correspond to ¼, ½, and ¾ full scale and adjusting the reference drivers until the correct output code transitions are observed. Note that the adjustments are interactive, so more than one pass will required.

Analog input bandwidth
To achieve maximum input bandwidth requires the use of a sample and hold before the analog input of the MA6561. Without a sample and hold function, the best input bandwidth is achieved by operating the MA6561 with a clock input having a low duty cycle.

9 bit resolution
To achieve 9 bit resolution, the reference resistor ladders of two MA6561 devices should be totem-poled as shown in figure 7. The aim is to split the 9 bit transfer function between two MA6561 converters. Since the absolute resistance value of each ladder may vary, external trim of the mid-reference voltage may be required.

The data outputs of the two devices (D0-D7) should be connected together. The OVERFLOW output of the lower MA6561 is used as the ninth bit, and to select which of the two MA6561 converters supplies the lower 8 bits of data. When the OVERFLOW output goes high, data must come from the upper device. When it goes low, data must come from the lower device. This is done by connecting the lower overflow signal to the $\overline{CE1}$ control of the lower device and the CE2 control of the upper device.

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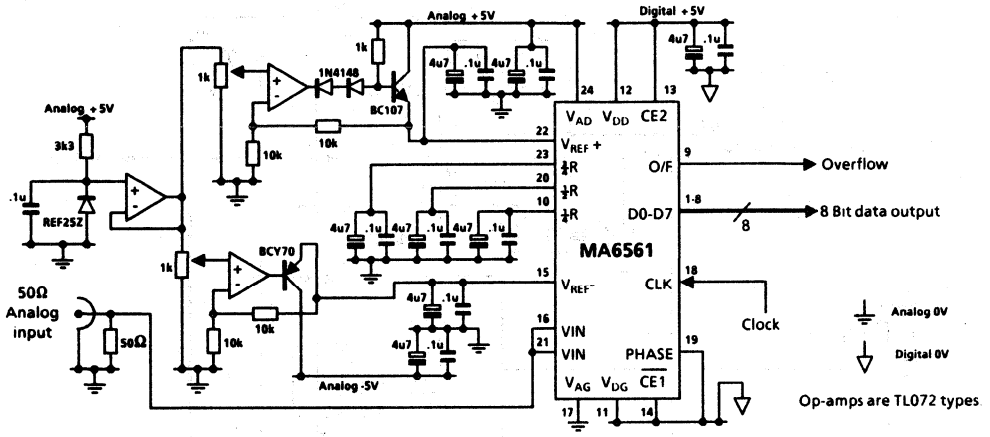
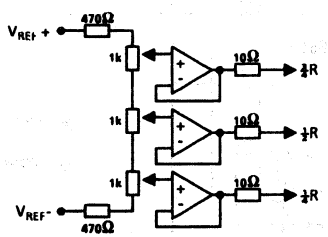
High Speed 8 Bit Flash Analog-to-Digital Converter

(Preliminary Data)

Typical Application (Figure 5)



Reference Driver Circuitry (Figure 6)



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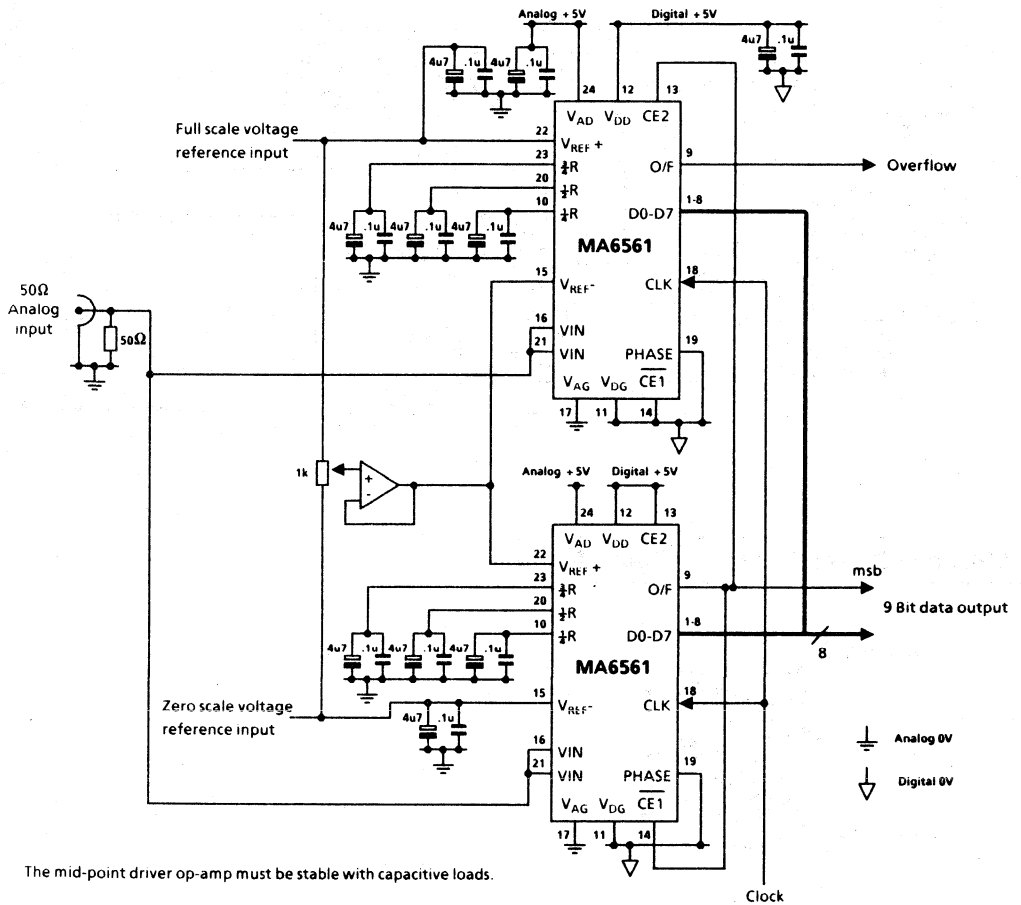
High Speed 8 Bit Flash Analog-to-Digital Converter

(Preliminary Data)

Expansion To 9 Bits (Figure 7)



The mid-point driver op-amp must be stable with capacitive loads.

MA6561

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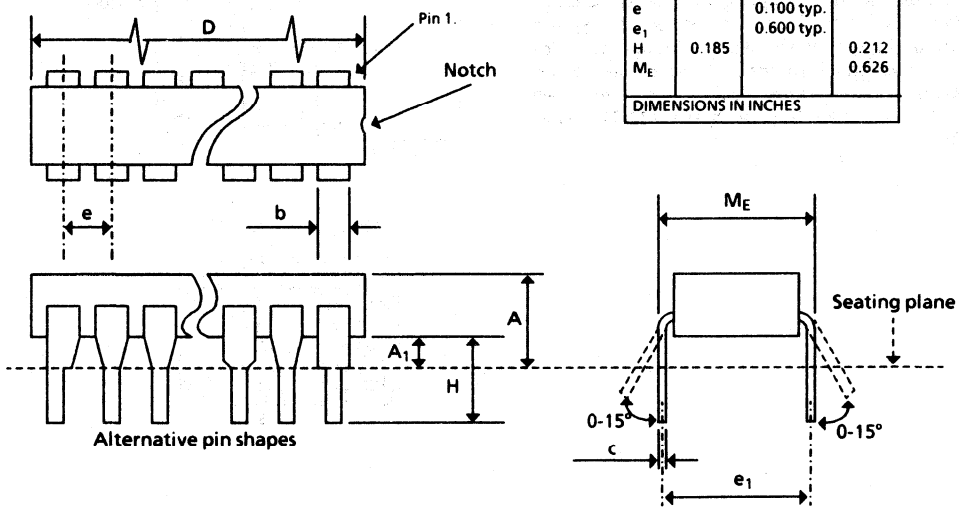
Packaging Information

24 Lead Ceramic Dual-in-line.

Ref.	Min.	Nom.	Max.
A			0.220
A_1	0.015		0.060
b	0.014		0.023
c	0.008		0.014
D			1.212
e		0.100 typ.	
e_1		0.600 typ.	
H	0.185		0.212
M_E			0.626

DIMENSIONS IN INCHES



Ordering Information

MA6561CCC - Ceramic Dual-in-line

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High Speed 8 Bit Flash Analog-to-Digital Converter
(Preliminary Data)

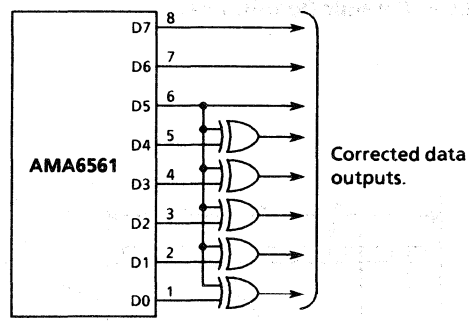
Appendix

Data coding error

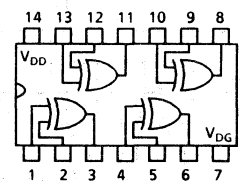
First samples of the AMA6561 have a data coding error. However, this error can be corrected with a simple external logic modification to allow full evaluation of the device.

The data coding error requires that for a true binary output, data lines D0 to D4 be Exclusive-Ored with D5. This can be implemented using two 74 series quad EXOR devices. 74AC86 devices are recommended as they are directly compatible with the AMA6561 and will not compromise speed performance. If the system being driven is sensitive to skew on the data lines introduced by the fix, then include a latch such as a 74AC574 after the logic fix.

Data Coding Logic Fix

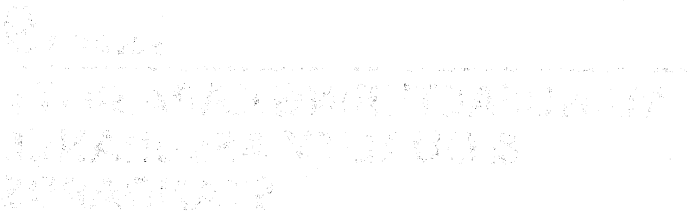


74AC86 in 14 pin DIL



section 9

MANUFACTURING CAPABILITY & QUALITY ASSURANCE STANDARDS



PART 1: INTRODUCTION AND USING THE DOCUMENT

Introduction:

At the GPS Lincoln site, a systematic manufacturing code has been adopted to enable easier specification of the manufacturing and quality inspection requirements for all integrated circuits.

This code is very similar in structure to the one previously used by MEDL as regards radiation tolerance, package and general quality level selection but allows for more flexibility and easier understanding of the manufacturing process flows required to meet given quality levels. This is of particular significance for higher rel products where the old code effectively restricted the number of manufacturing options that could be offered to customers.

The new code is directly related to process modules on the site CAM system. This minimises the risk of any process related manufacturing errors whilst at the same time enabling a large variety of flow options to be offered to the customer.

Please consult with factory services or marketing in Lincoln if any more information is required.

Using the Manufacturing Capability Document.

On the next page is a diagram showing the form of the device name and manufacturing code used for integrated circuits at GPS Lincoln.

Each empty box represents an alphabetic character. The options for the first three of these "boxes" are shown on the diagram. Reference to parts 2,3 and 4 of this document will explain in detail the assembly, test and QA/QCI options offered for the last three. Using just five characters after the device name in this way allows for many package, rel and manufacturing options to be specified whilst causing a minimum of confusion.

In parts 2,3 and 4 the specific options for each manufacturing area are indicated by letters in the appropriate "boxes". Characters not applicable to that area are simply shown by empty "boxes" as on the device name diagram. Note that only the last four characters of the code are shown in these process definitions.

The document can be used in two ways, either as a reference to check what a particular code represents or as an options specification to build up the code for a specific requirement.

For example: A device of name: **MAS17501FSBAF**

The letter **S** at position MA**S**17501FSBAF signifies a rad hard process.
The letter **F** at position MAS17501**F**SBAF signifies a flatpack package.
The letter **S** at position MAS17501F**S**BAF signifies Class S manufacture.

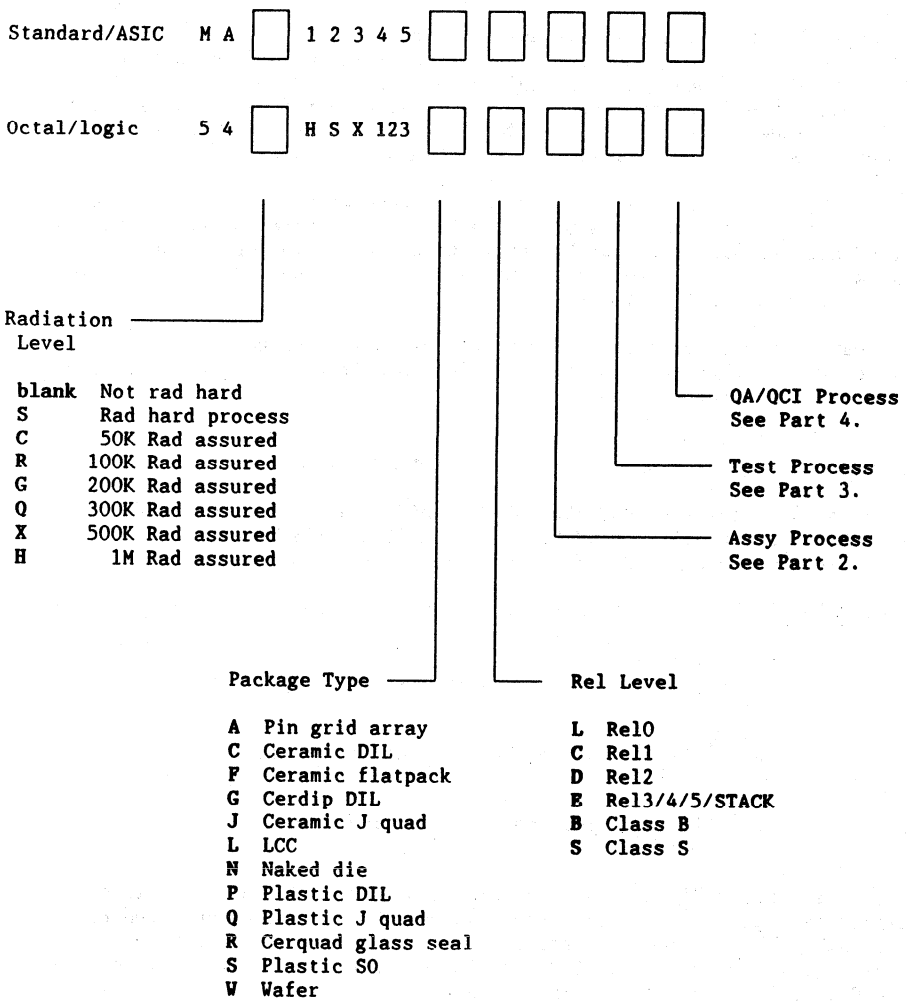
The code **BAF** is built up using parts 2,3 and 4 of the document as follows:

S	B			for the assembly process (from part 2)
S		A		for the test process (from part 3)
S			F	for the QA/QCI option (from part 4)

Thus, device **MAS17501FSBAF** is manufactured on a rad hard process, in a flatpack package to a standard space assembly but less PIND and bond pull tests. It is then tested to a standard (3 burnin) MILSTD Class S test process and is subject to a QCI involving group A and B tests, with generic group D data being supplied with the shipment.

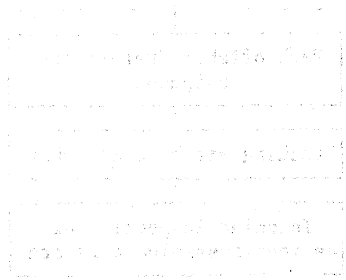
Note regarding naked dice:
Naked dice are usually supplied to only two code options; **NC** (2nd optical inspection to BS9400) and **NB** (2nd optical inspection to MILSTD 883 2010 condition B) although space level dice (**NS**) can be supplied to special order. Naked dice qualification on a per lot basis is also available if required.

Structure of IC Name and Manufacturing Code



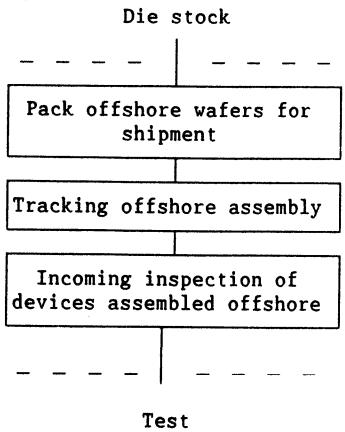
Note: For naked dice, the last three code letters are not applicable.
For wafers, the last four code letters are not applicable.

PART 2: ASSEMBLY PROCESSES

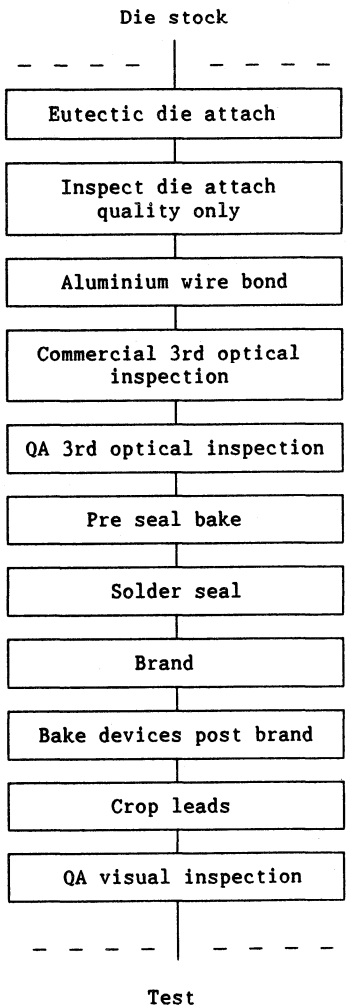


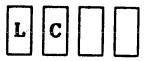
L A

Offshore assembly.

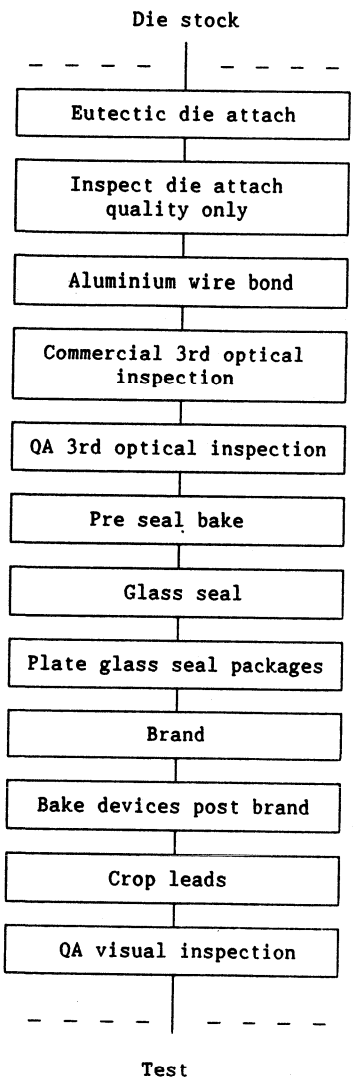


L B Solder seal, DIL or flatpack packages.



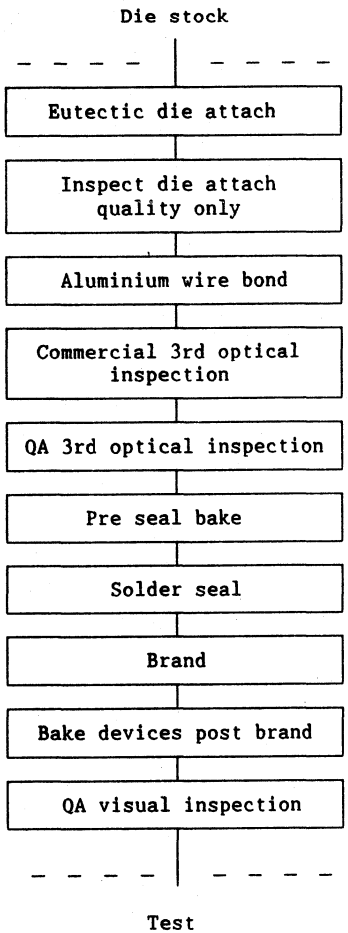


Glass seal, cerdip packages.



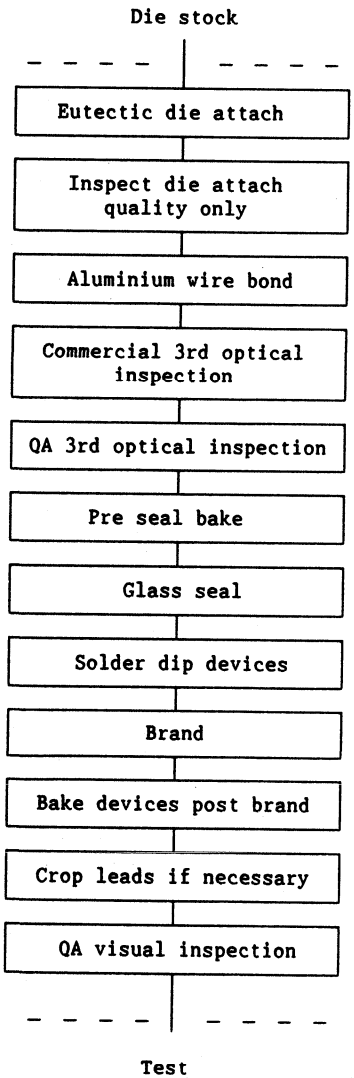
L D

Solder seal, PGA/LCC packages.

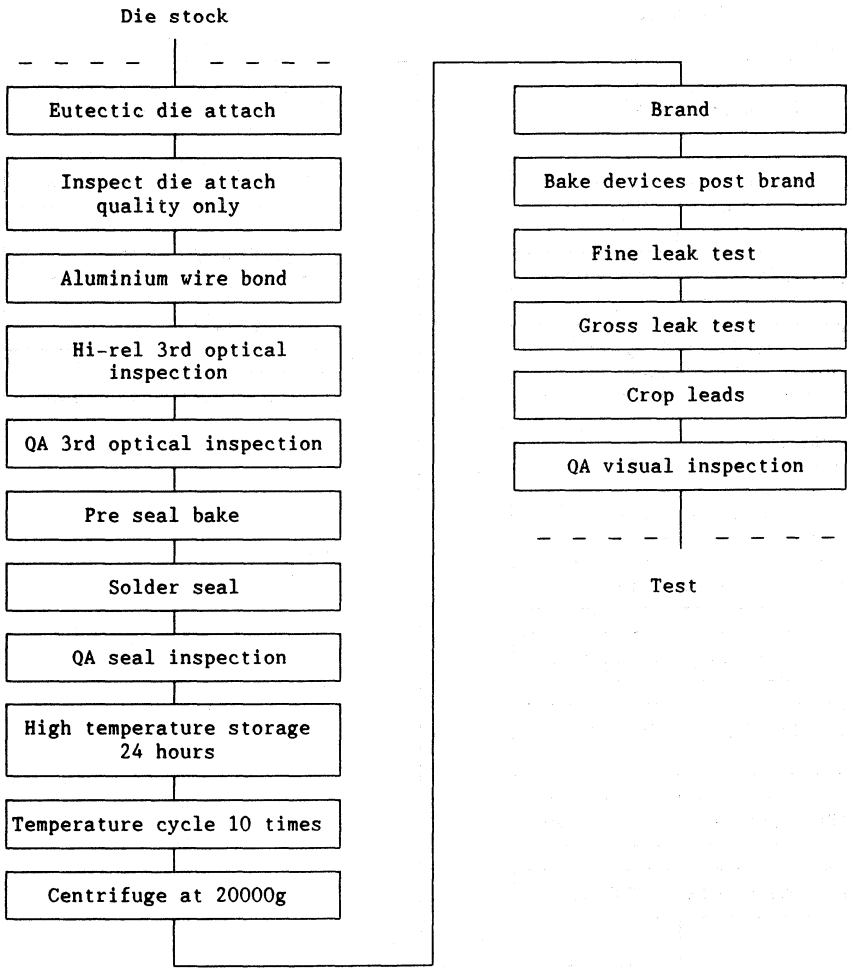


L E

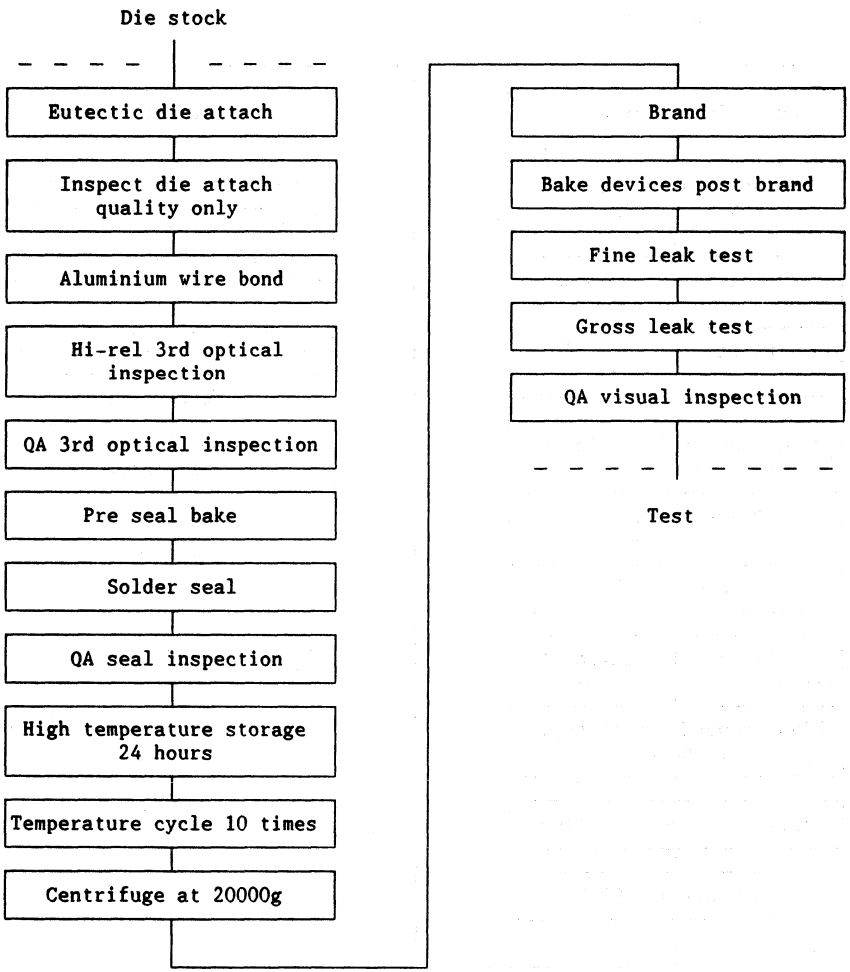
Glass seal, cerquad packages.



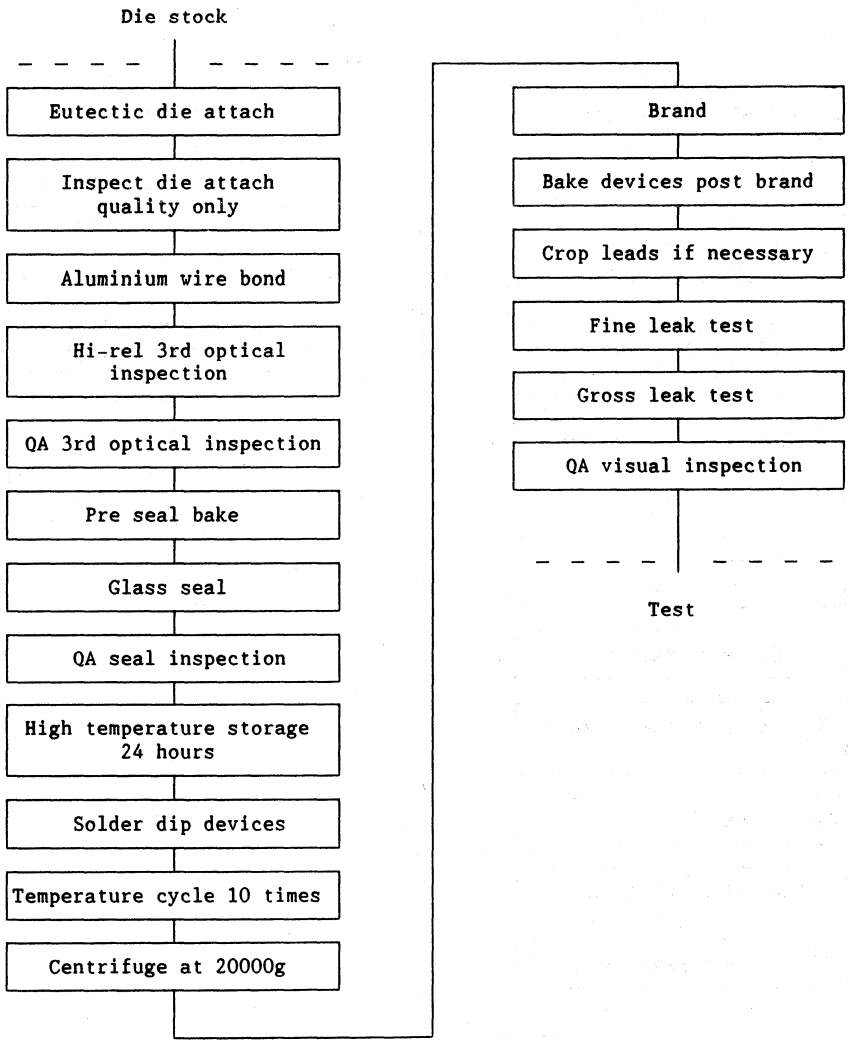
C A Solder seal, DIL or flatpack packages.



C B Solder seal, PGA/LCC packages.

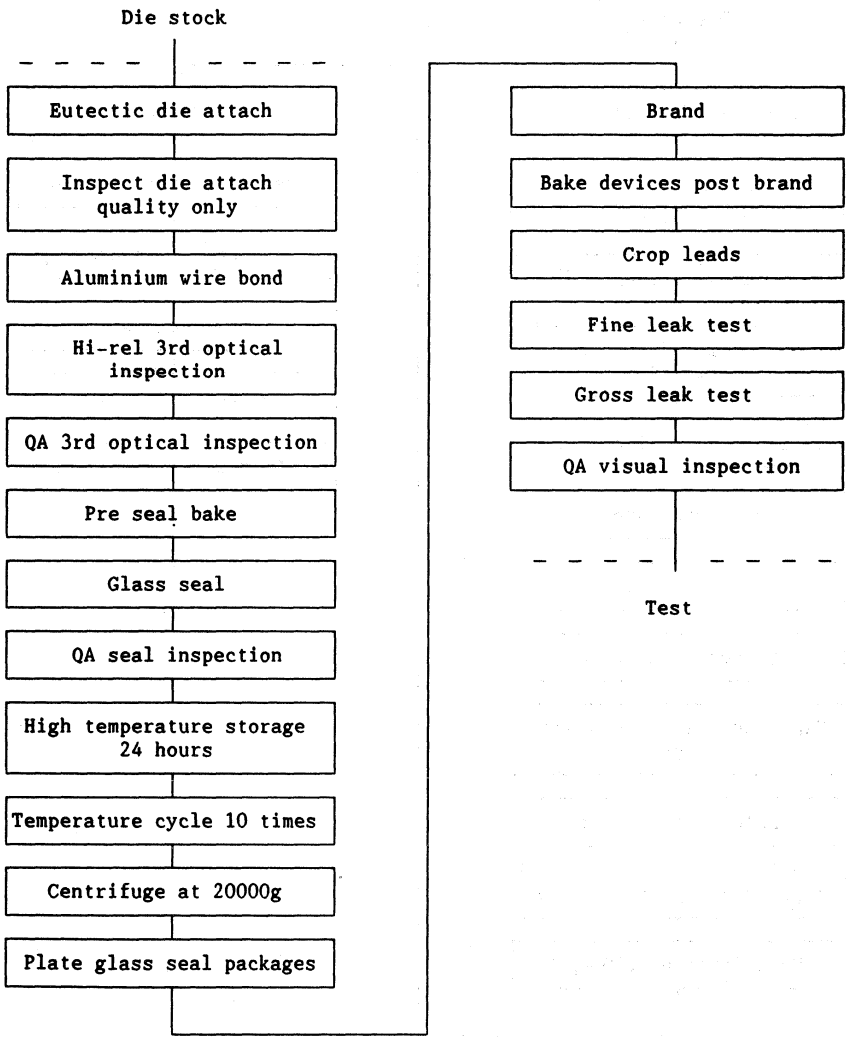


C C Glass seal, cerquad packages.

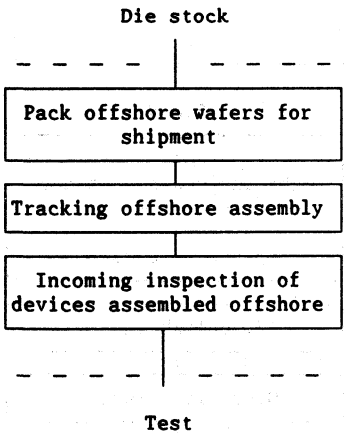


9

C D Glass seal with plate, cerdip packages.

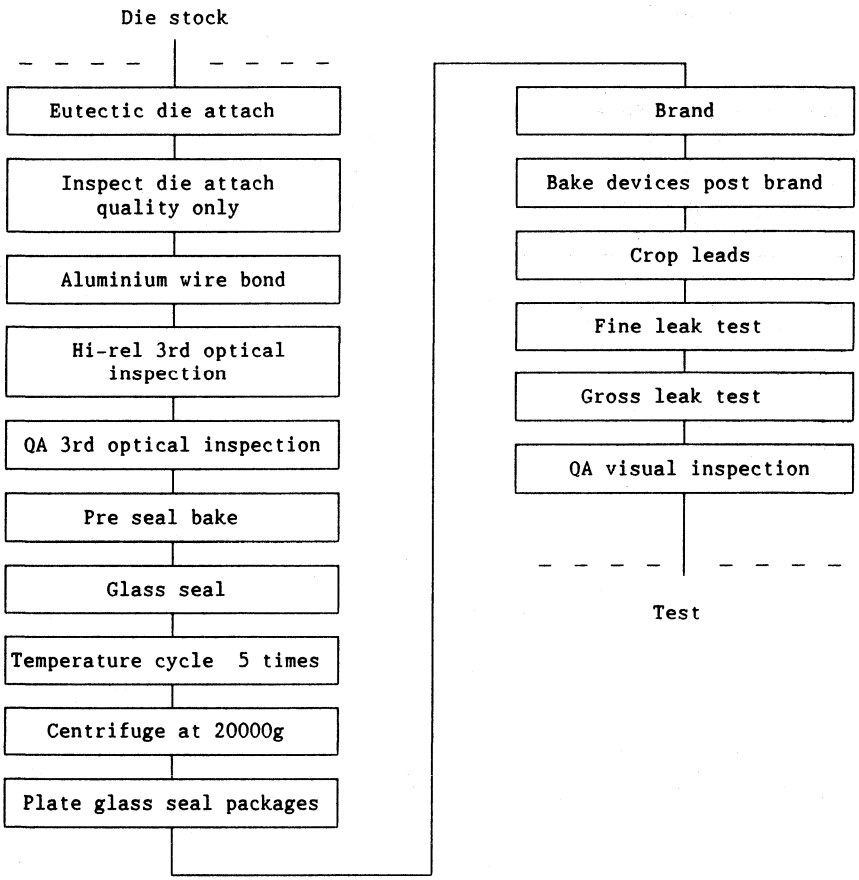


D A Offshore assembly.



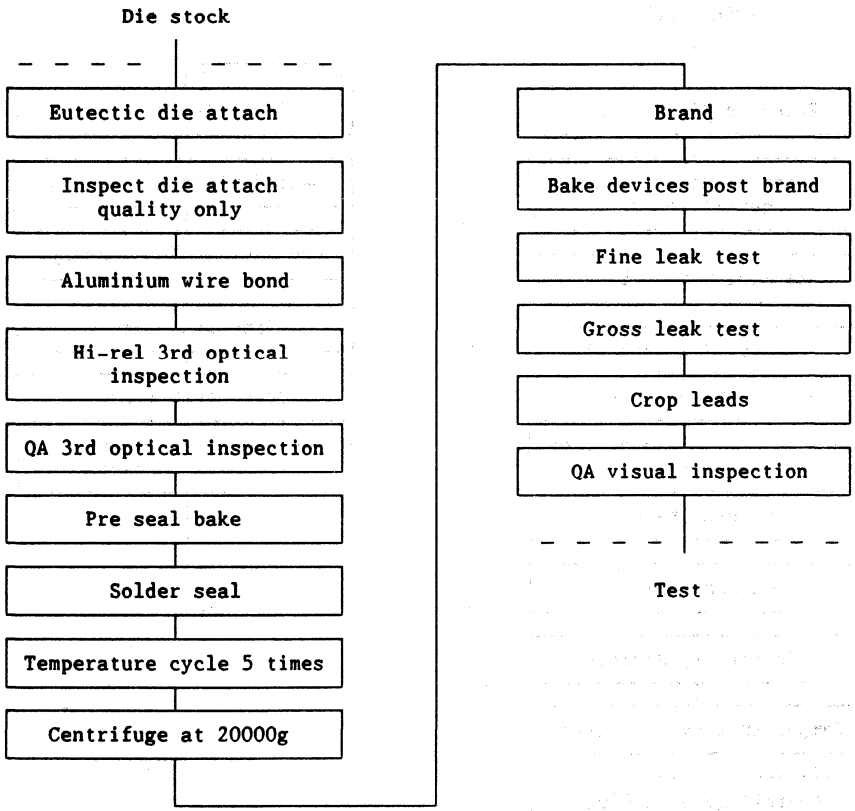
D B

Glass seal, cerdip packages.



D C

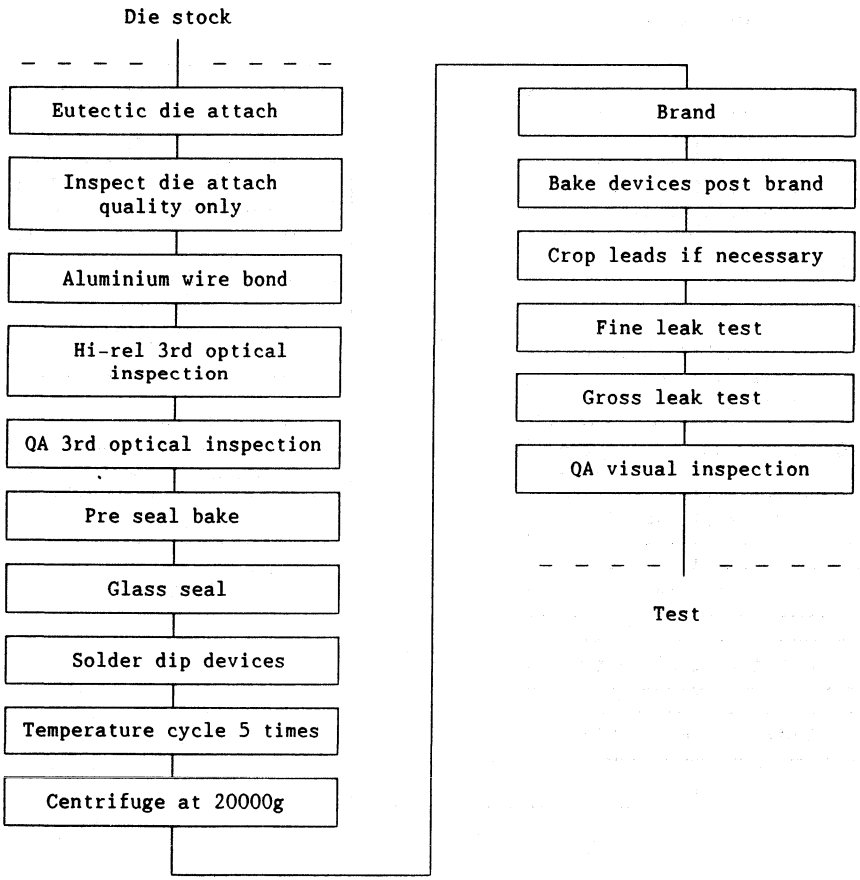
Solder seal, DIL/flatpack packages.



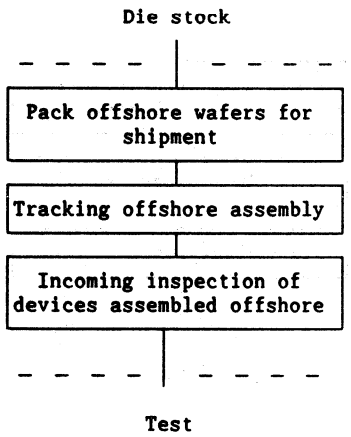
9

D D

Glass seal, cerquad packages.

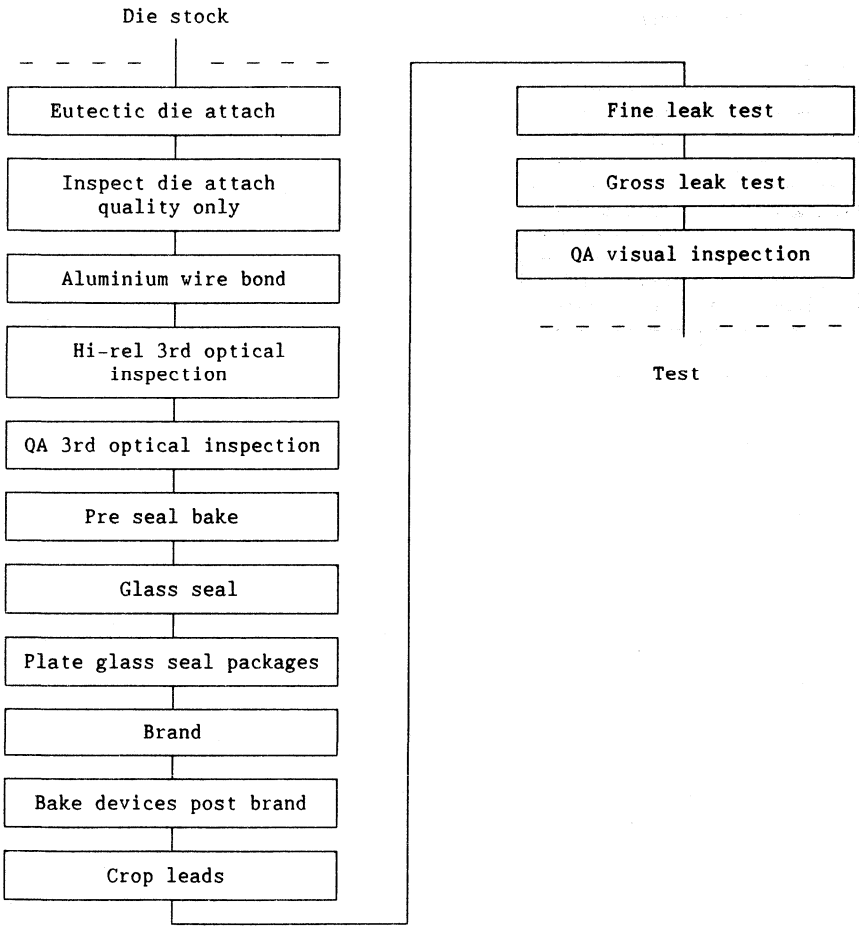


E A Offshore assembly.

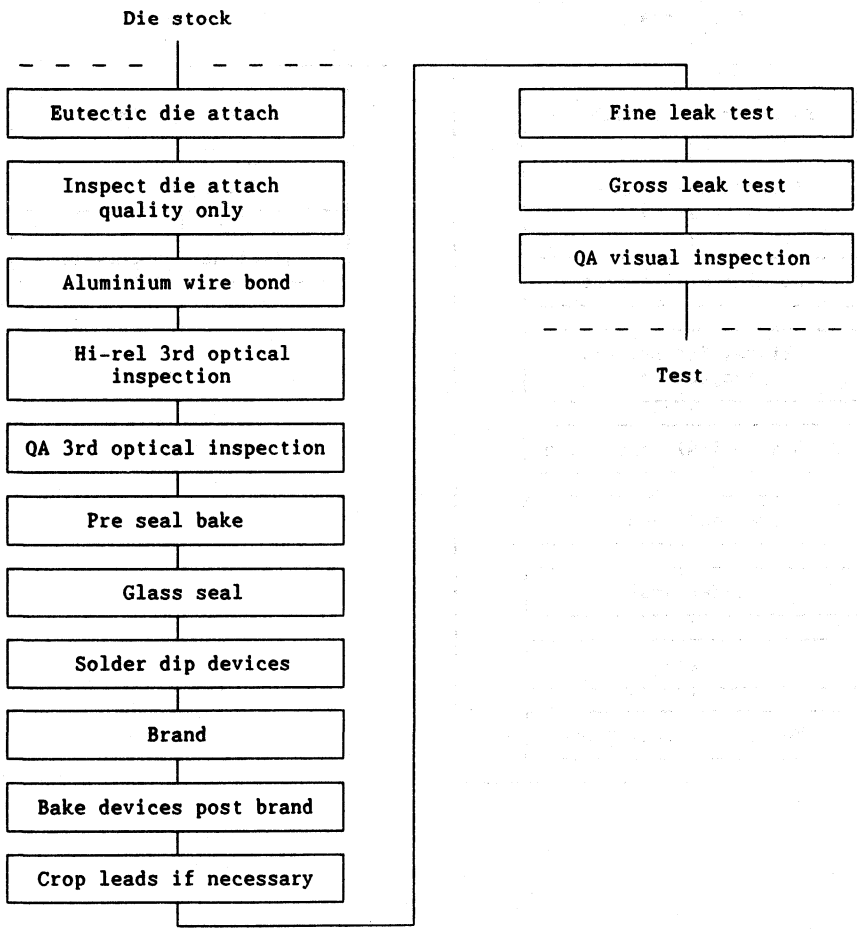


E B

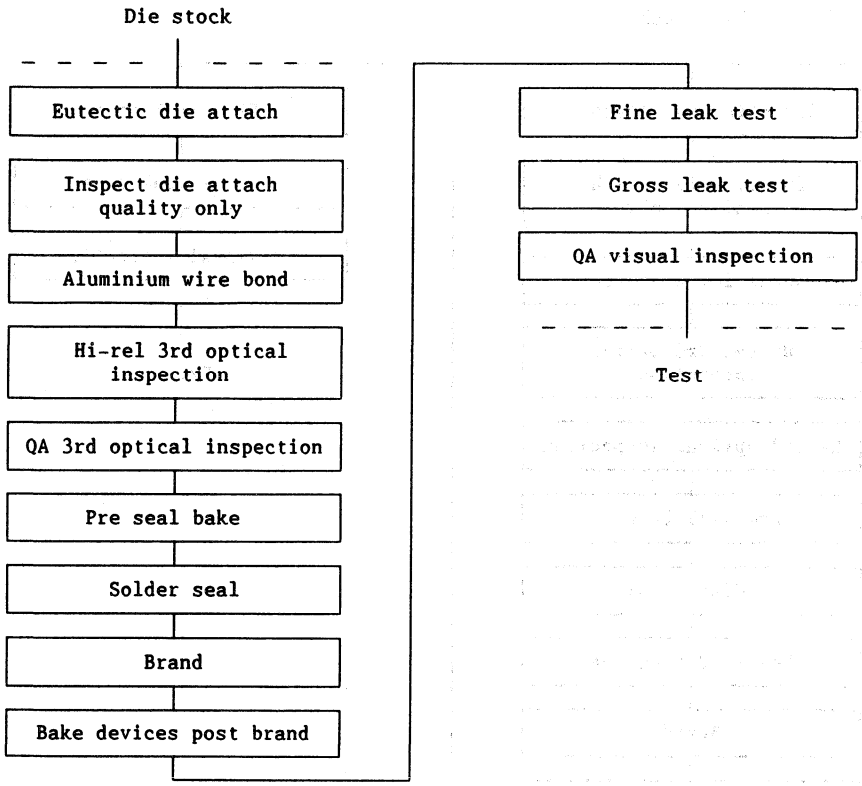
Glass seal, cerdip packages.

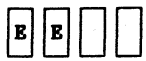


E C Glass seal, cerquad packages.

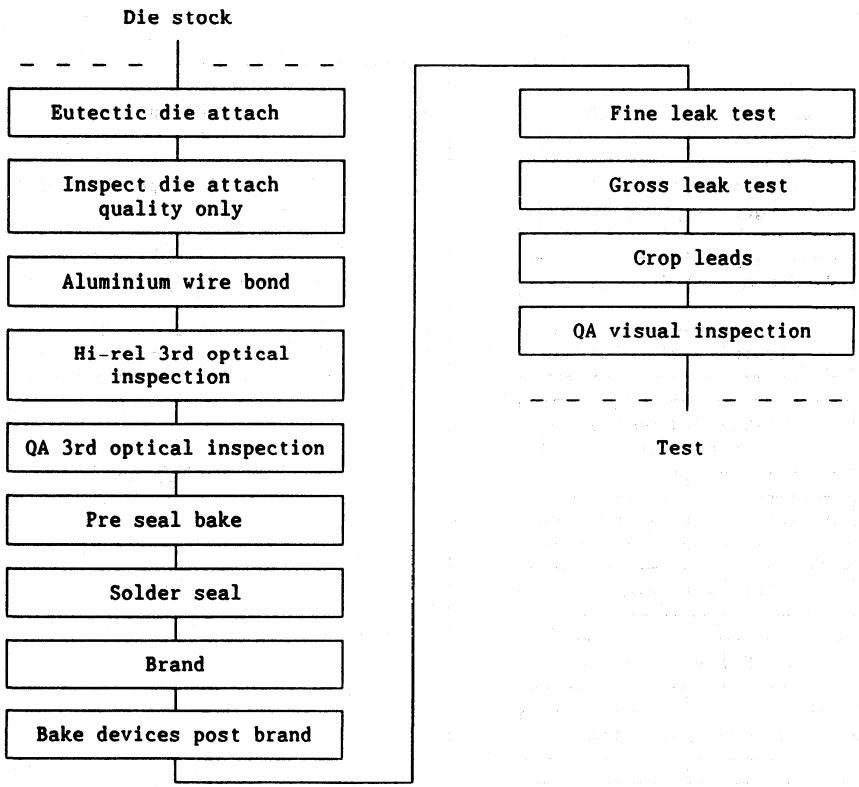


E D Solder seal, PGA/LCC packages.



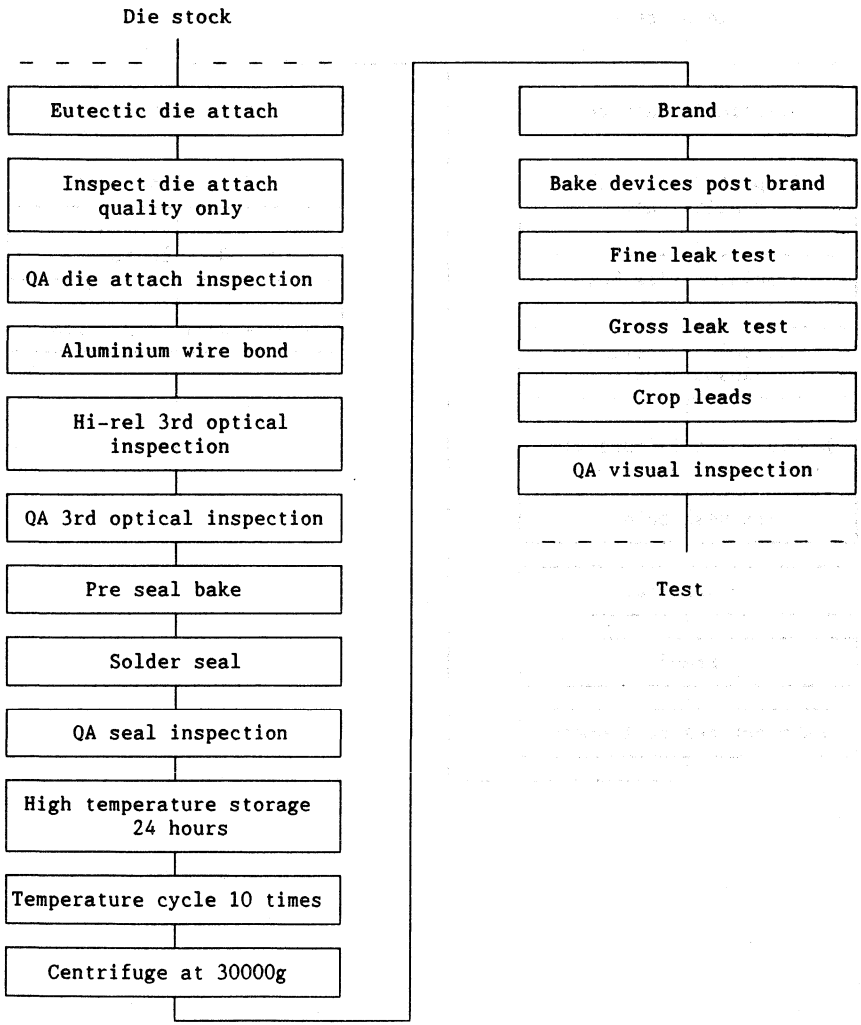


Solder seal, DIL/flatpack packages.



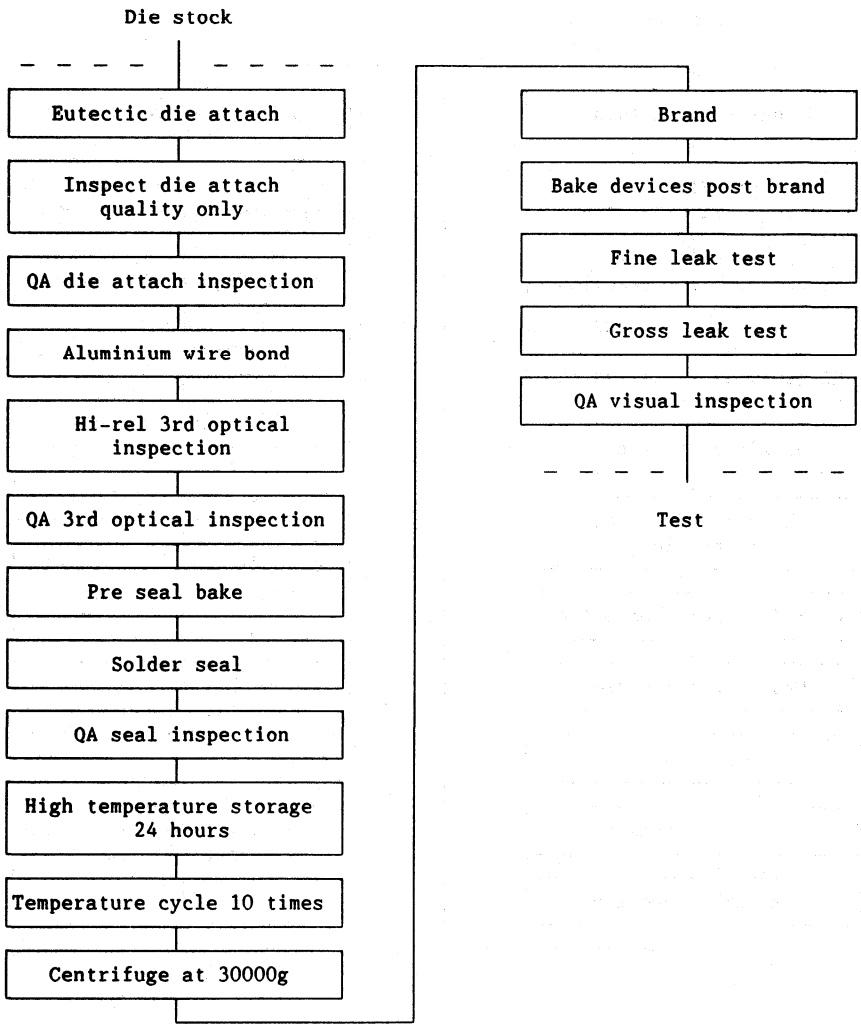
B A

Standard solder seal, DIL/flatpacks.



B B

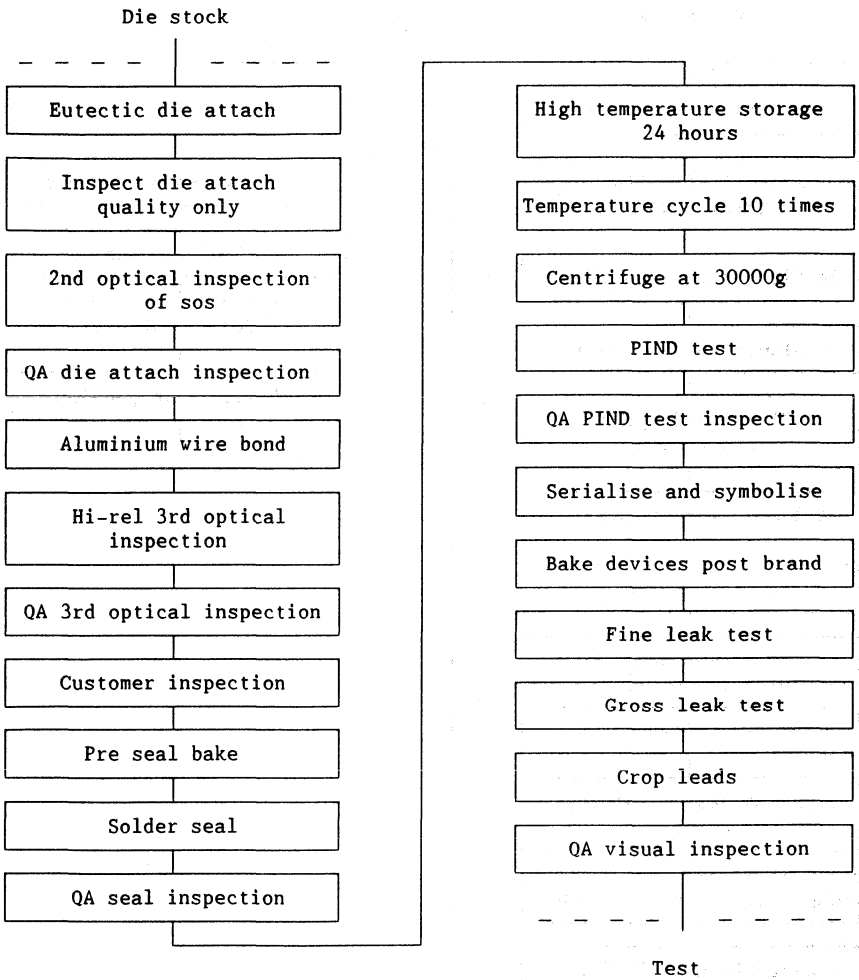
Standard solder seal, PGA/LCC packages.



9

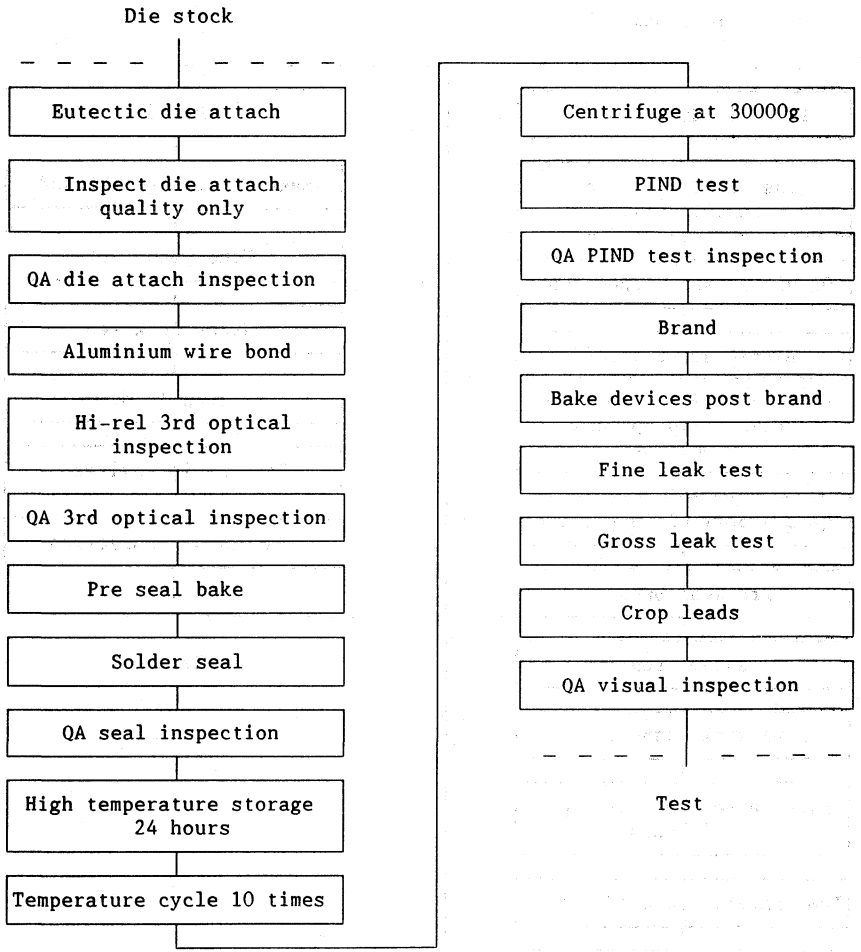
B C

Solder seal, DIL/flatpack packages with PIND and customer pre cap.



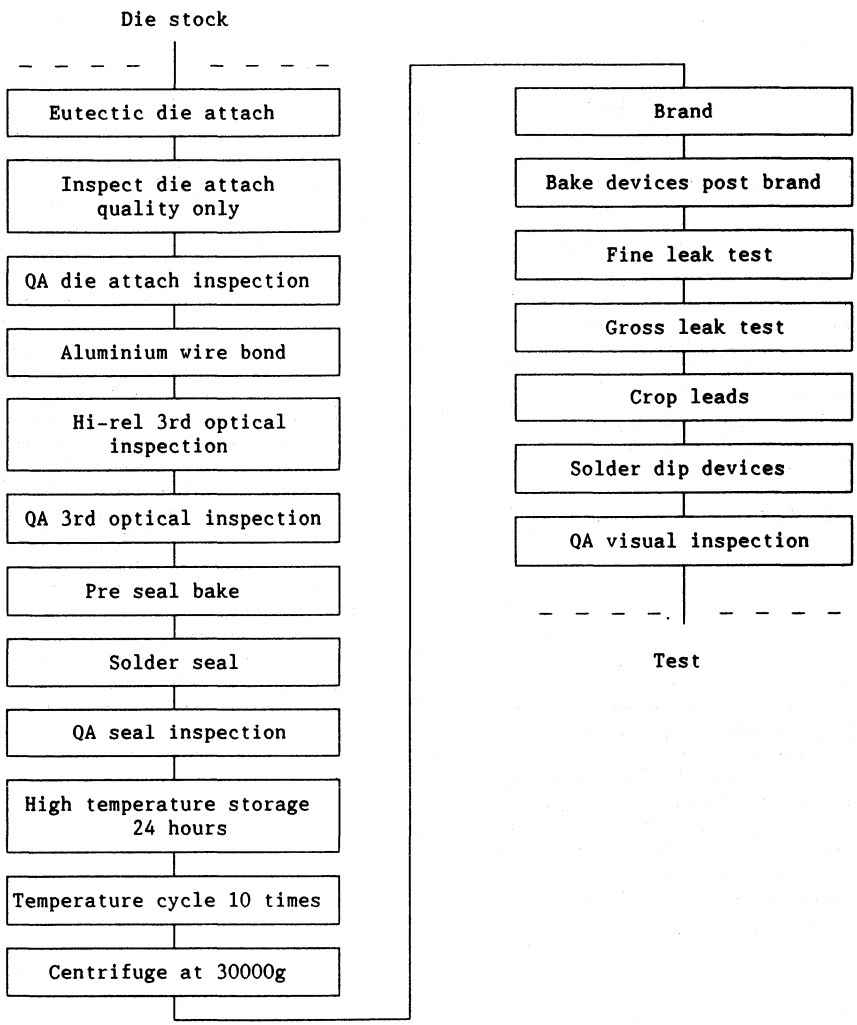
B D

Solder seal, DIL/flatpack packages with PIND.



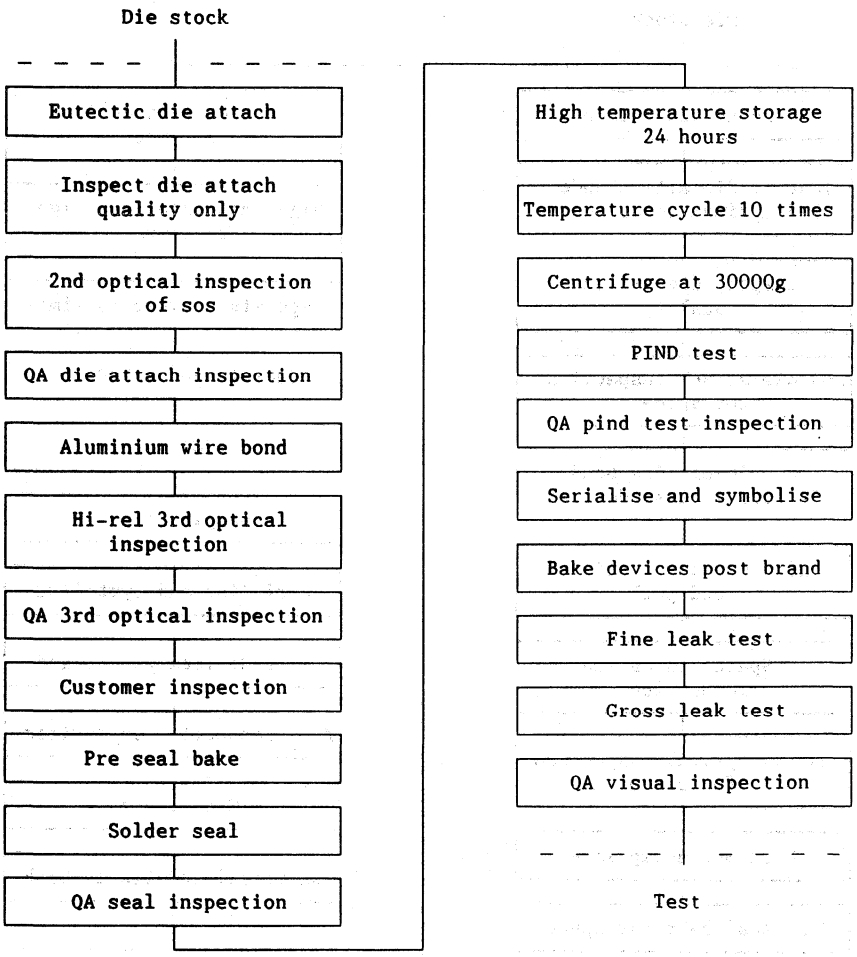
B E

Solder seal, DIL/flatpack packages with solder dip.



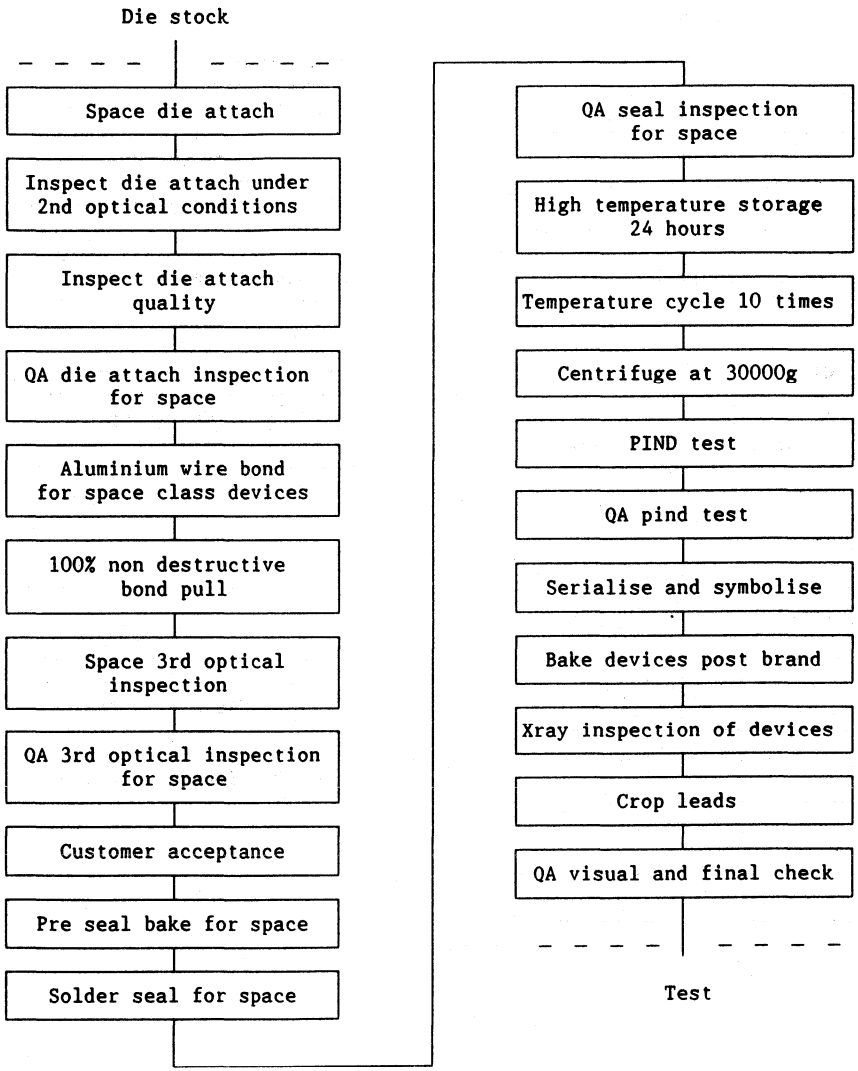
B F

Solder seal, PGA/LCC packages with PIND and customer pre cap.



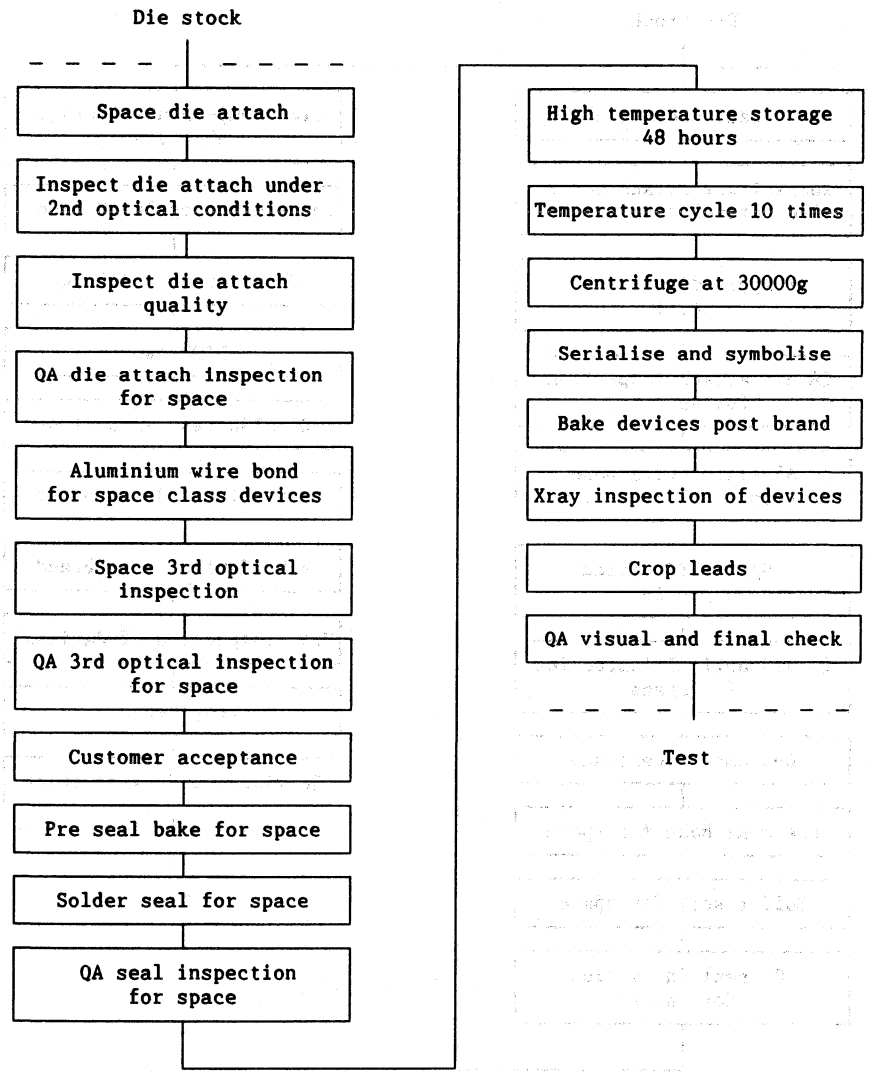
S A

Standard solder seal, DIL/flatpacks.



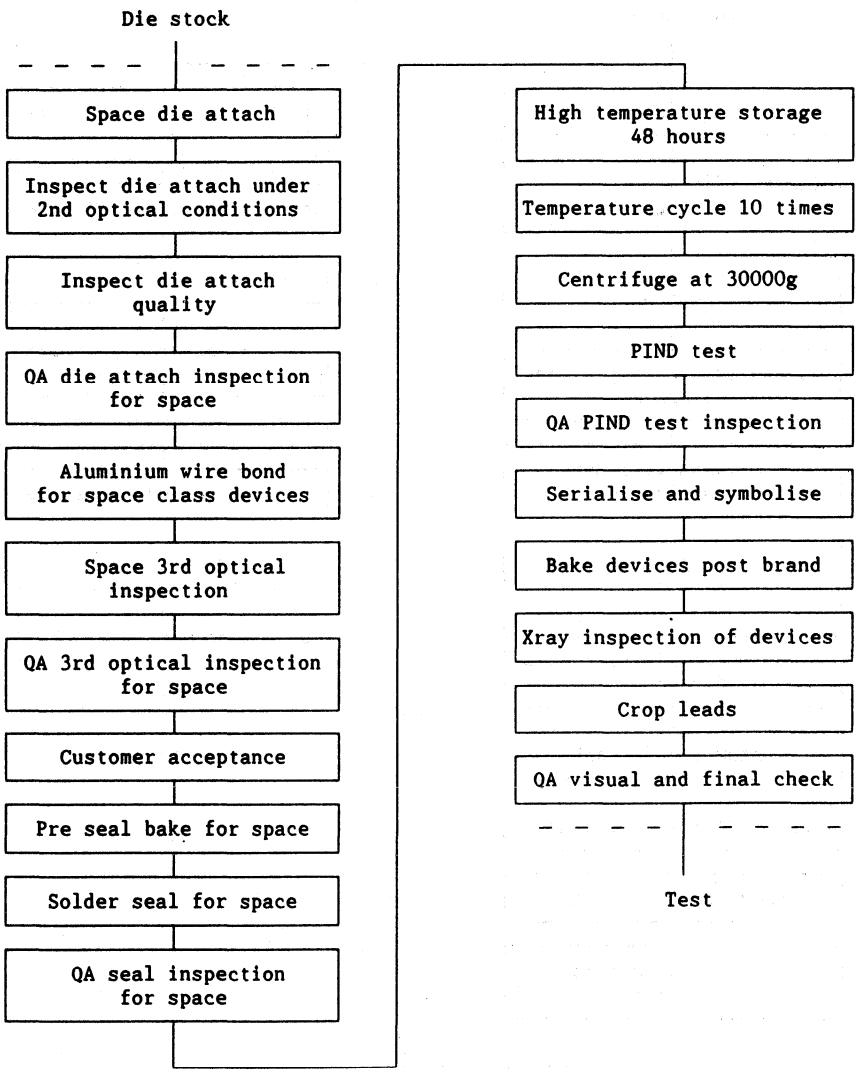
S B

Solder seal, DIL/flatpacks with no bond pull or PIND.



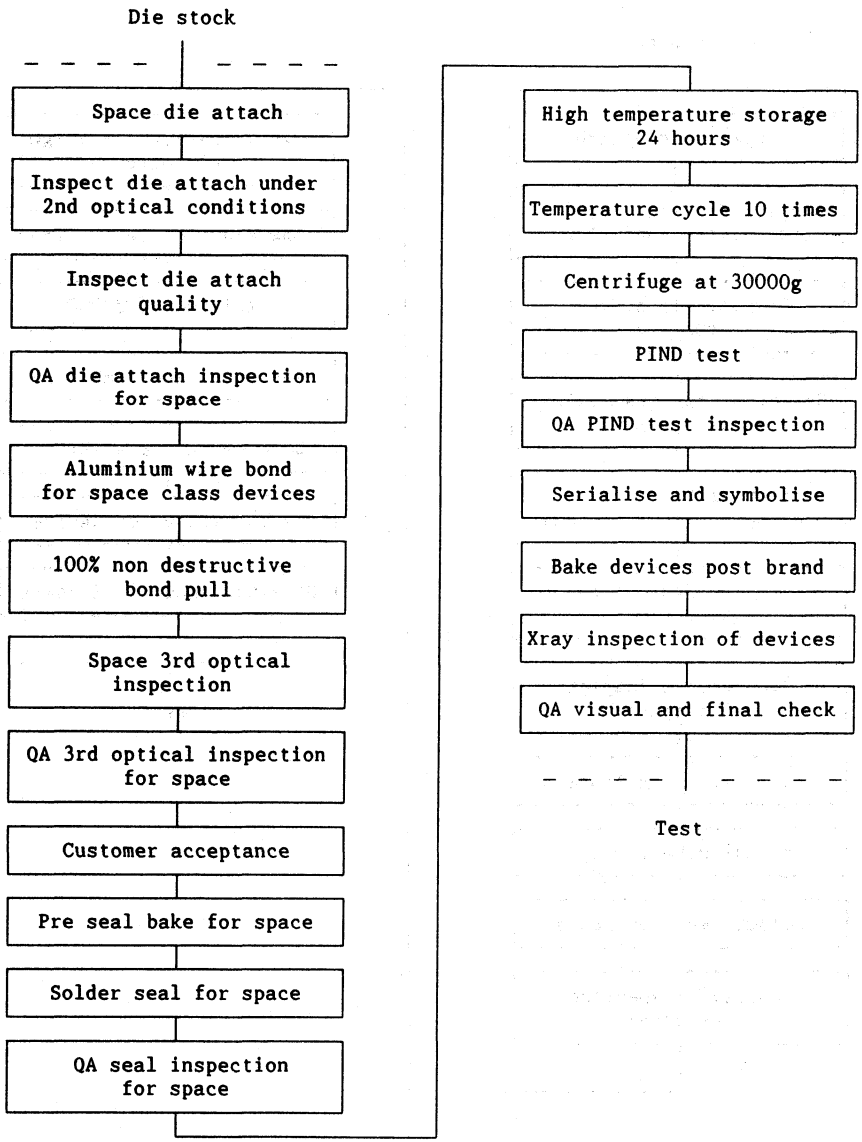
S C

Solder seal, DIL/flatpacks with PIND but no bond pull.



S D

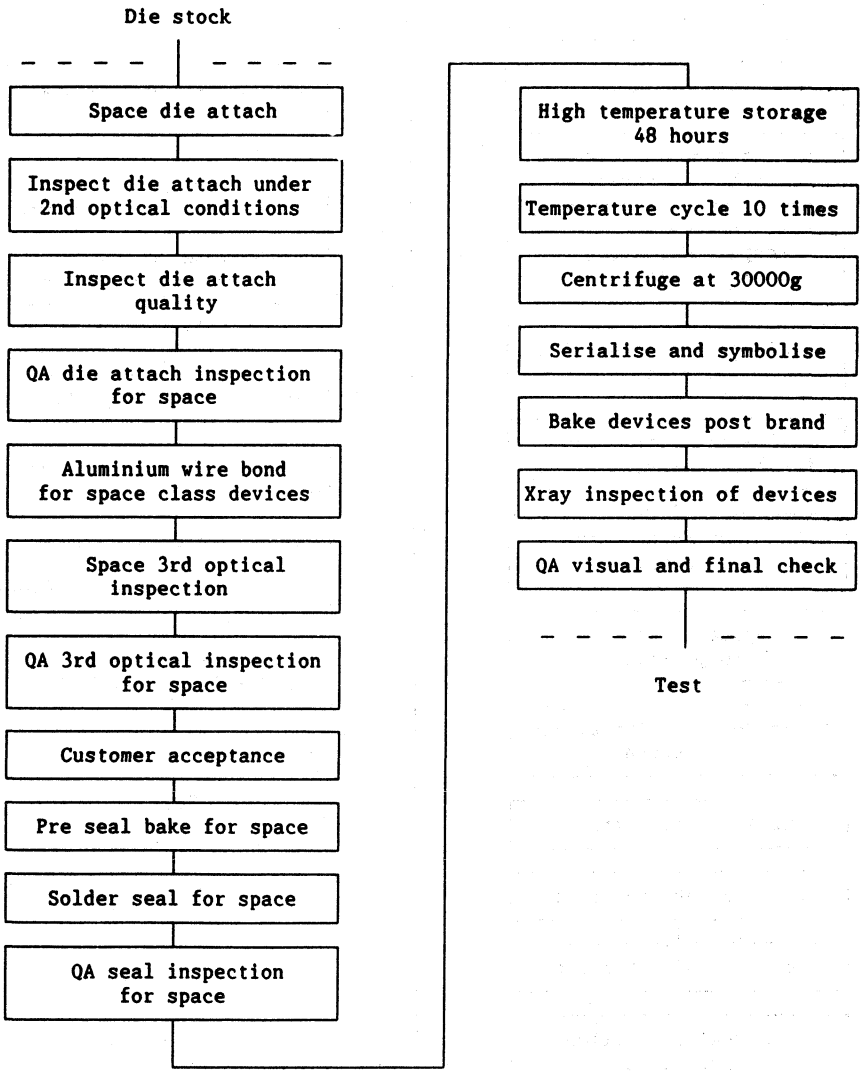
Standard solder seal, PGA/LCC packages.



9

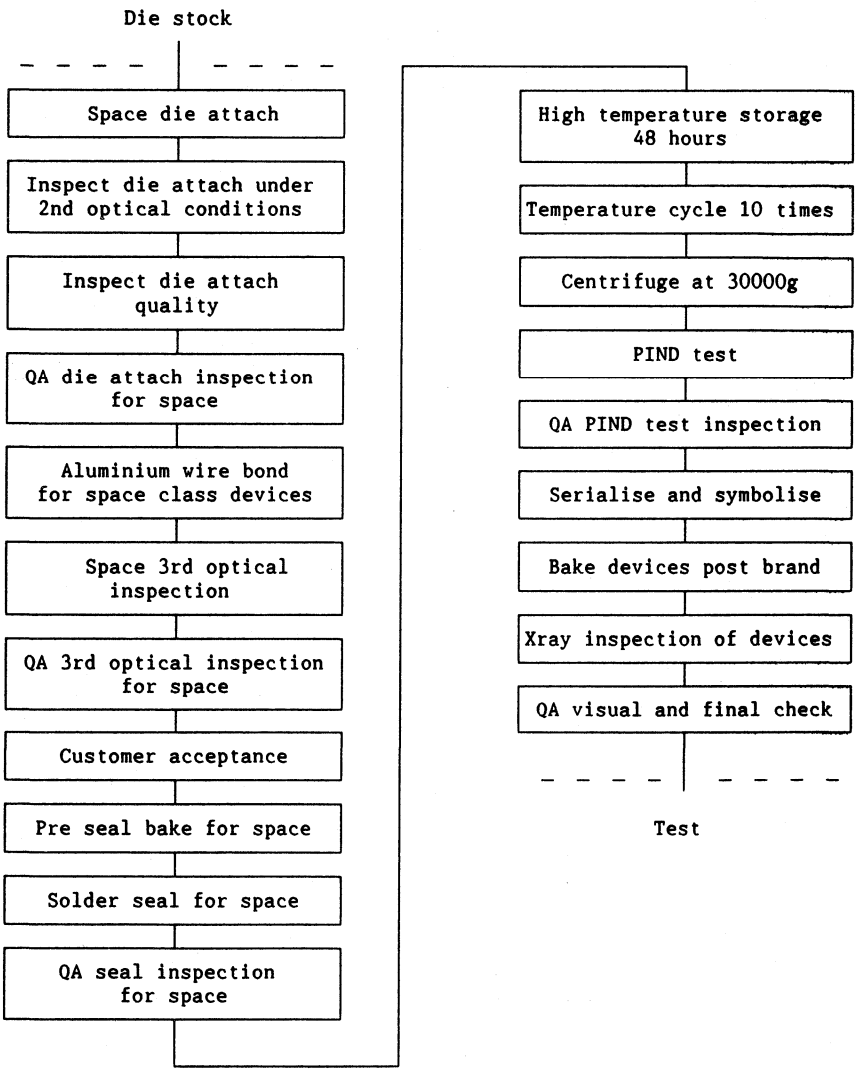
S E

Solder seal, PGA/LCC packages with no bond pull or PIND.



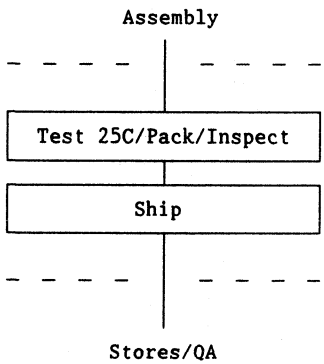
S F

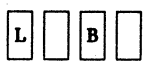
Solder seal, PGA/LCC packages with PIND but no bond pull.



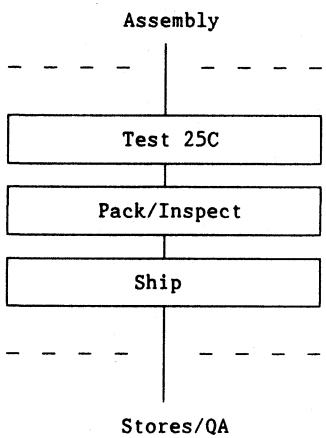
PART 3: TEST PROCESSES

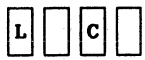
Standard Rel 0, dial2 testers.



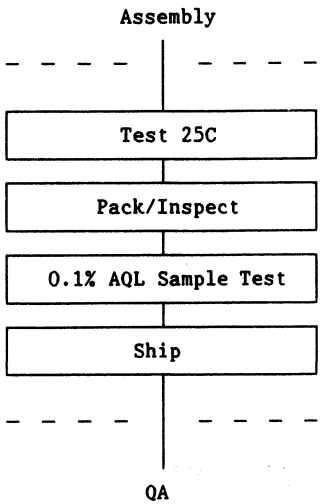


Standard rel 0, other testers.

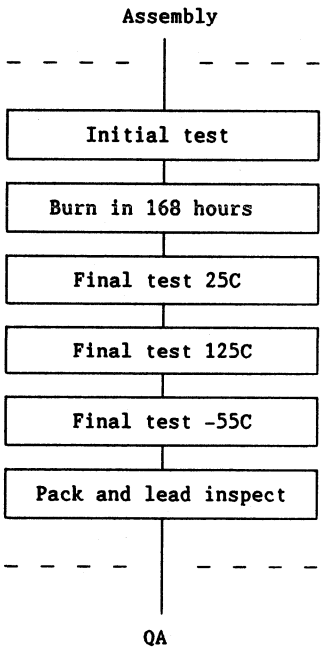




Rel 0 with sampling to 0.1% AQL.



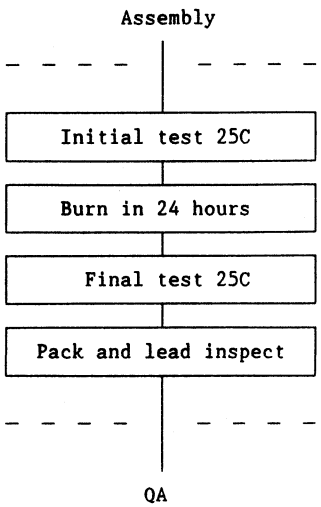
C A Standard Rel 1.



(100% 25C and sample 125C)

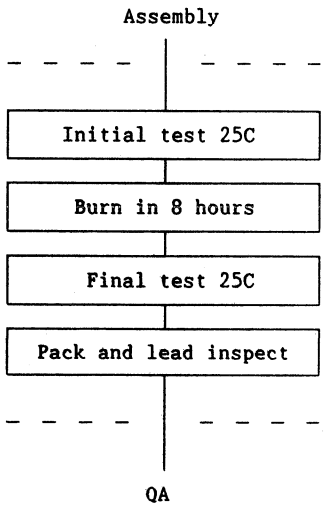
D		A	

Hermetic packages, 24 hour burnin.

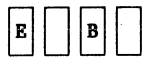


E		A	

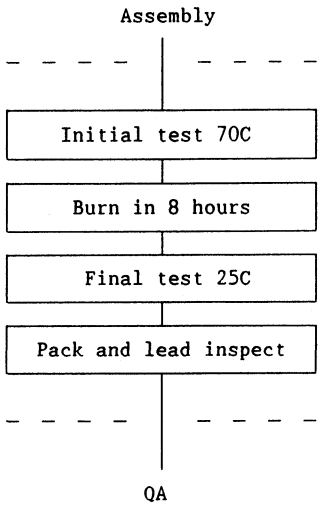
Standard 8 hour burnin.



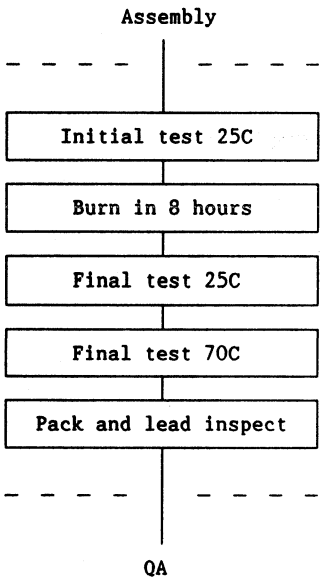
9



8 hour burnin with initial 70C test.

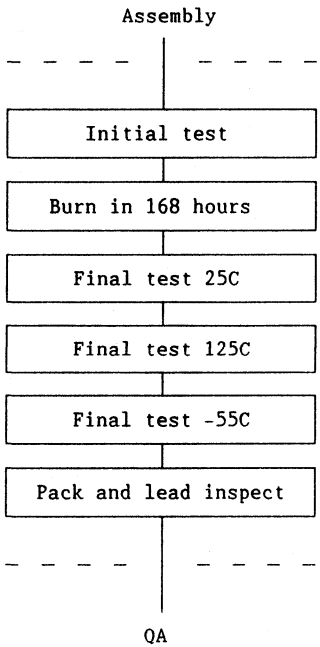


E | | C | | 8 hour burnin with final 70C test.

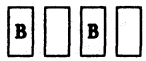


Class B Test Flows Page 1

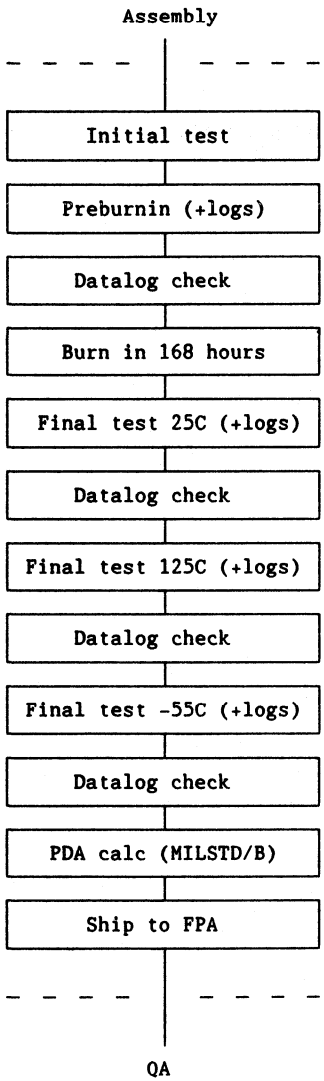
Standard MILSTD Class B.



(100% 25C and sample 125C)

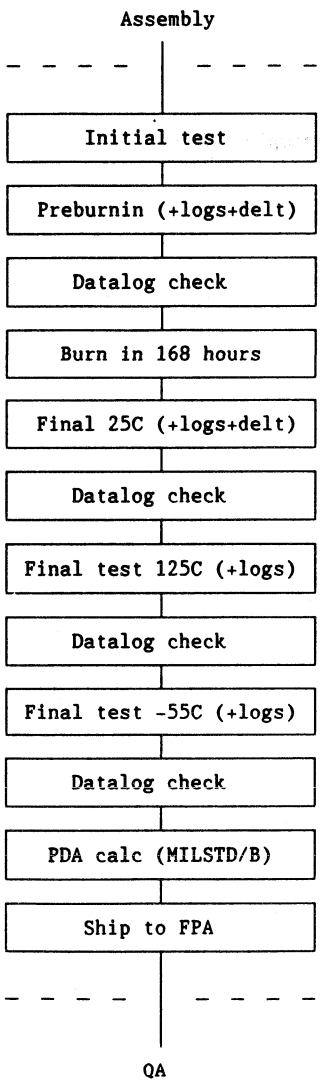


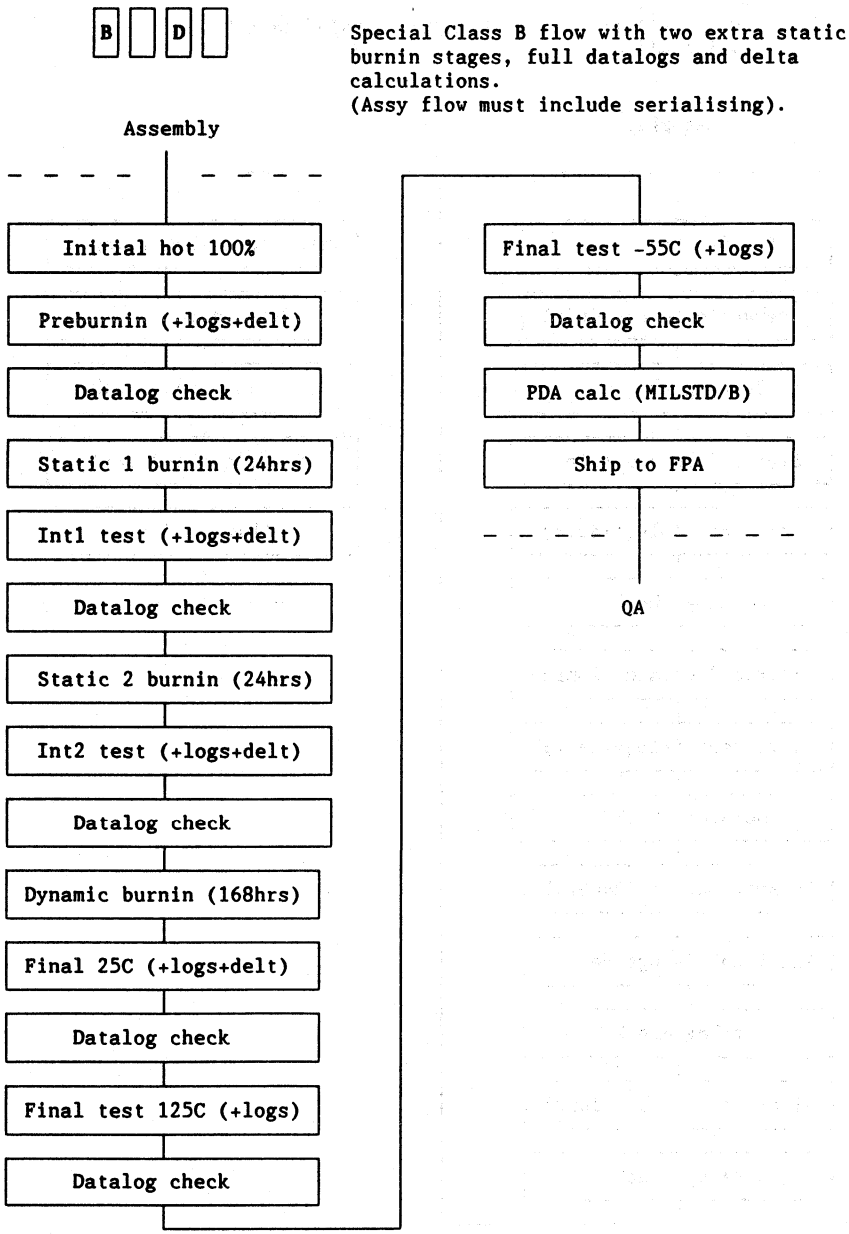
MILSTD Class B with datalogs.
(Assy flow must include serialising).



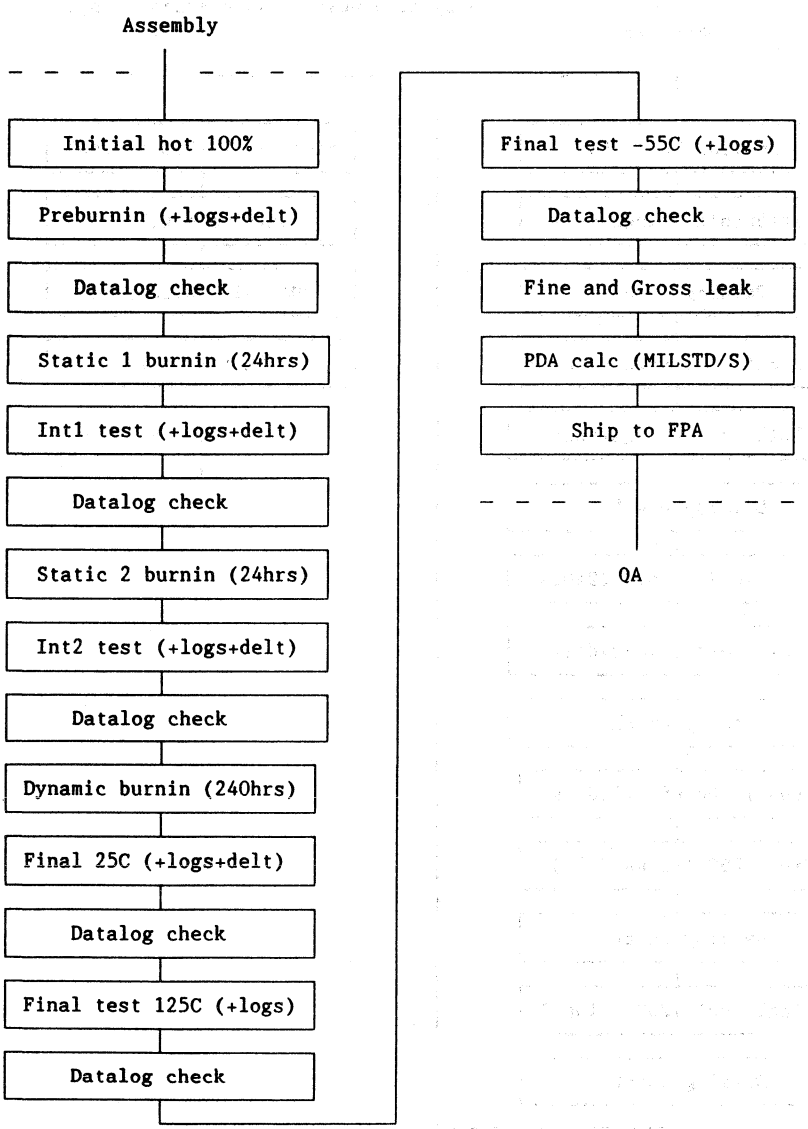
B C

MILSTD Class B with datalogs and delta calculation across burnin. (Assy flow must include serialising).



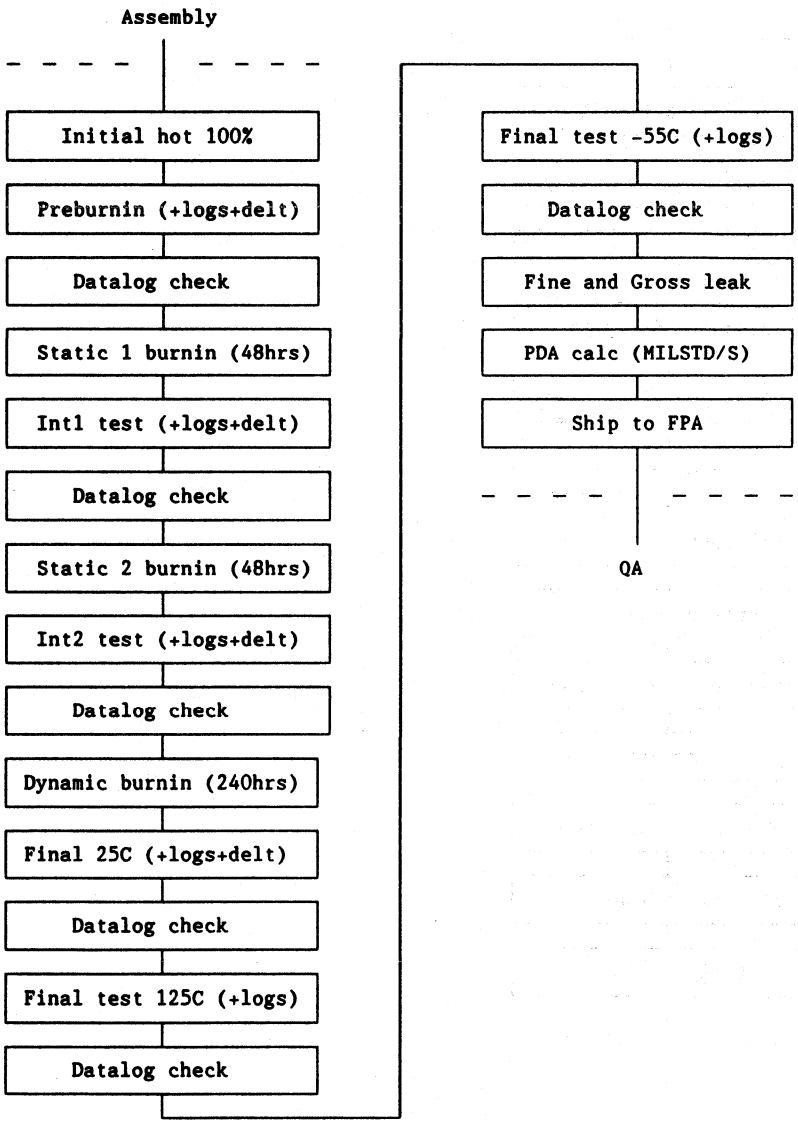

B
D
Special Class B flow with two extra static burnin stages, full datalogs and delta calculations.
(Assy flow must include serialising).
Assembly
Initial hot 100%
Preburnin (+logs+delt)
Datalog check
Static 1 burnin (24hrs)
Int1 test (+logs+delt)
Datalog check
Static 2 burnin (24hrs)
Int2 test (+logs+delt)
Datalog check
Dynamic burnin (168hrs)
Final 25C (+logs+delt)
Datalog check
Final test 125C (+logs)
Datalog check
Final test -55C (+logs)
Datalog check
PDA calc (MILSTD/B)
Ship to FPA
QA

S | | A | | Standard MILSTD Class S.

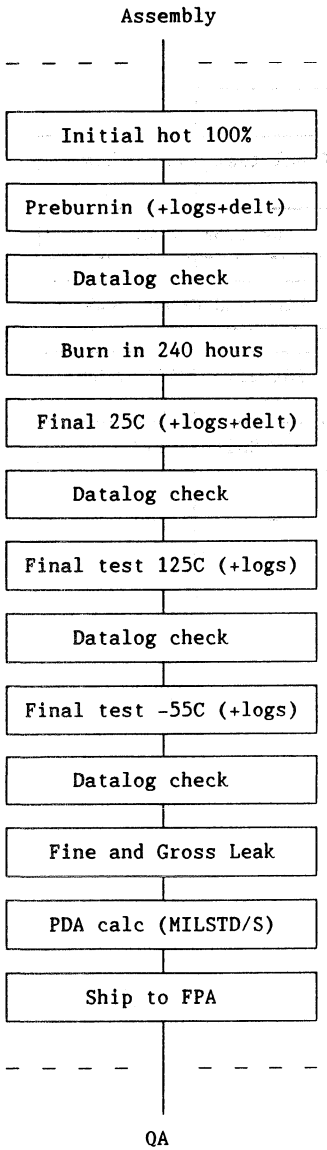


S B

MILSTD Class S with 48 hour static burnin stages.

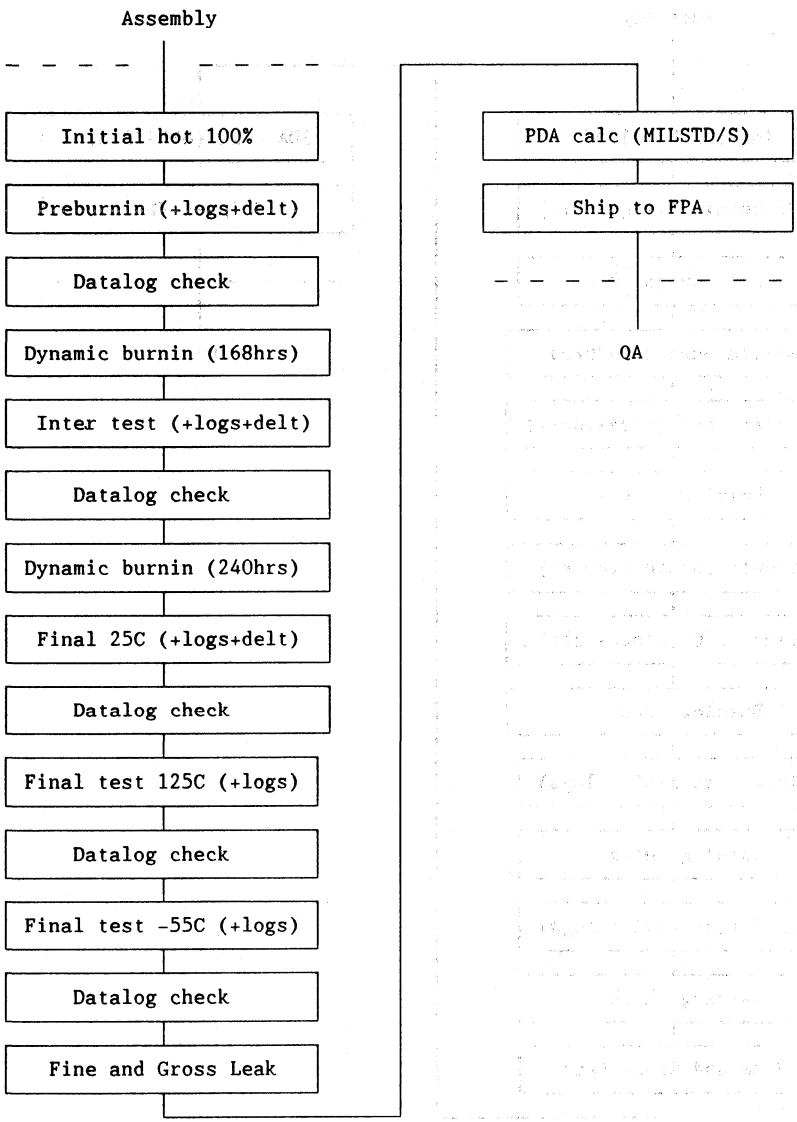


S | | C | | MILSTD Class S with single burnin.



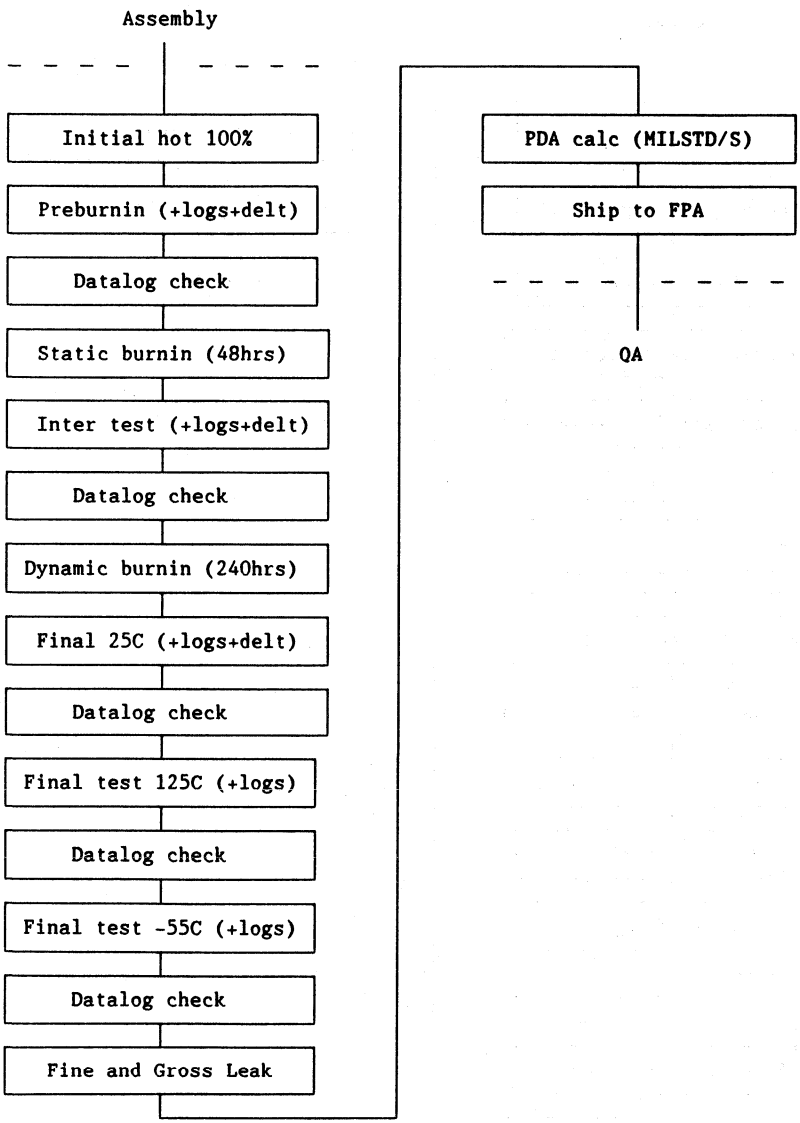
S D

MILSTD Class S with pre conditioning burnin.



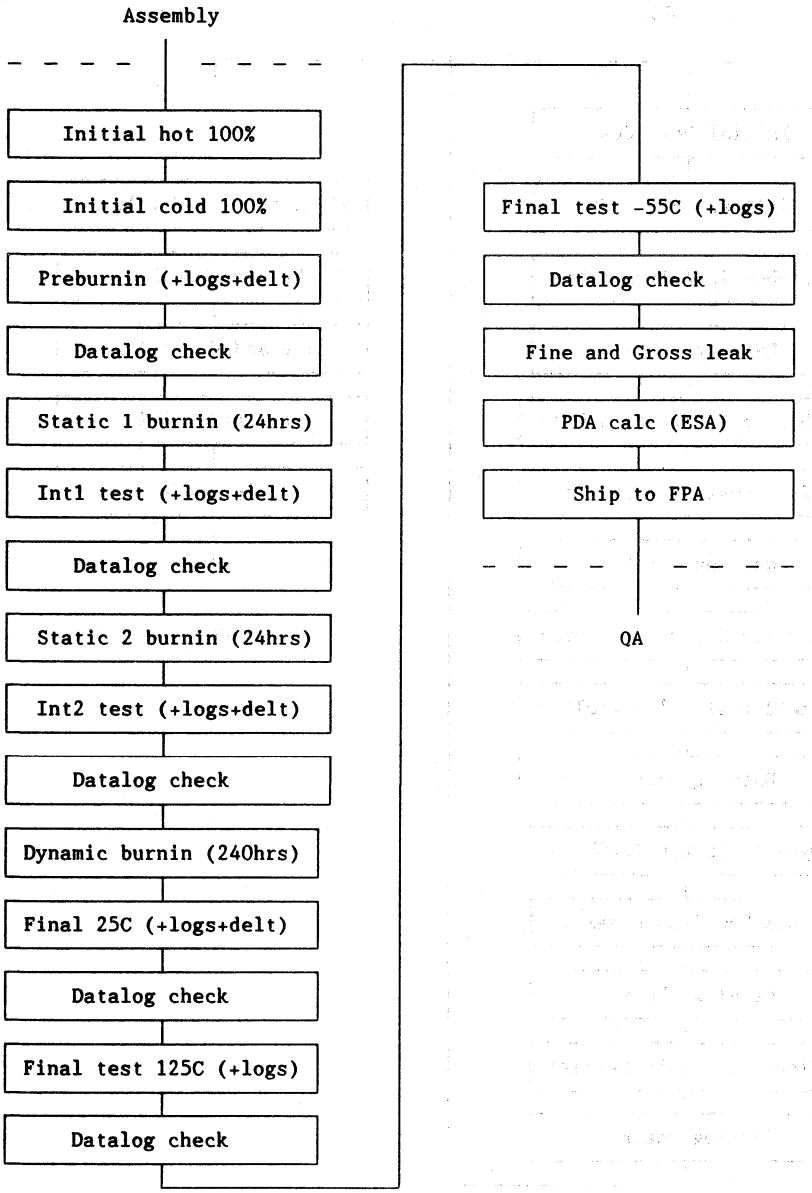
S E

MILSTD Class S with single static burnin.



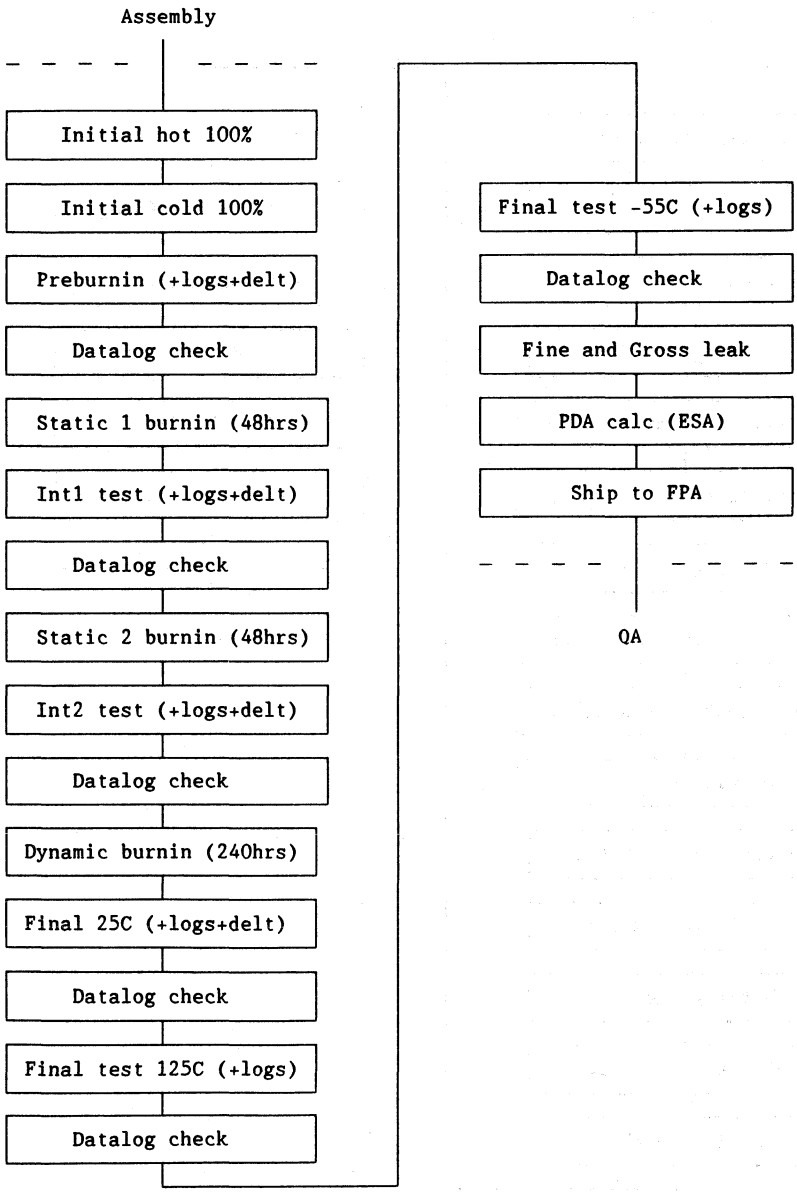
S F

ESA 9000 space class with 24 hour static burnins.

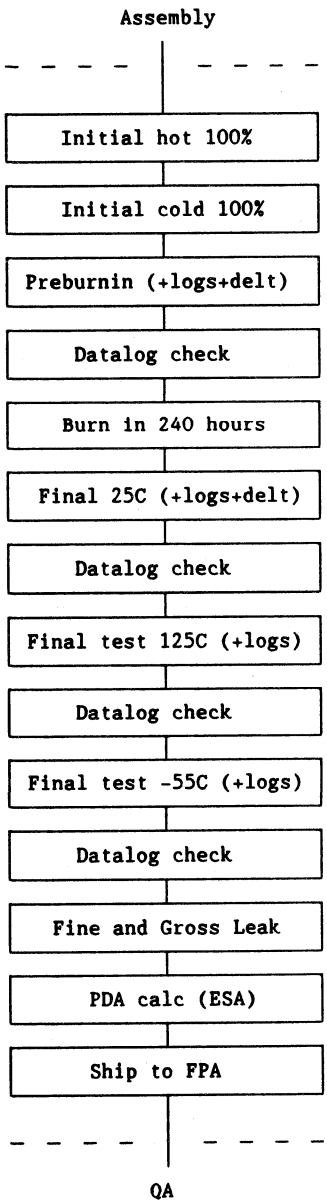


S G

ESA 9000 space class with 48 hour static burnins.



S | | H | | ESA 9000 space class with single burnin.



PART 4: QA/QCI OPTIONS

General: All groups, sub-groups and tests are derived from BS9400 unless otherwise indicated. A3a and A4a tests are carried out at 25C. For plastic options, B7b (high temp and humidity) tests are covered generically according to GPS/MEDL spec ref AG130.

L A

Rel 0 type D. Commercial plastic and hermetic.

No QCI or QA tests required.

L B

Rel 0 type E. Commercial plastic and hermetic.

Each lot
Sub-groups:
A1 : Visual inspection.
A2 : Verification of device type.
A3a and A4a : Static and dynamic tests at 25 C.

Every 6 months
Sub-groups:
C4a : Static and dynamic tests at max specified temp.
C4b : Static and dynamic tests at min specified temp.

L C

Rel 0 type F. Commercial plastic.

Each lot
Sub-groups:
A1 : Visual inspection MIL method 2009.
A2 : Verification of device type.
A3a and A4a : Static and dynamic tests at 25 C.
A5 : Marking permanence MIL method 2015.

B1 : Dimensions.
B2a : Solderability to IEC 68-2-20.
B7b : 1000hr (85C/85%) high temp and humidity (generic)

Every 6 months
Sub-groups:
C9 : Thermal Stress to IEC 68-2-20A.

(A3a and A4a end-point tests are carried out after B7b and C9).

General: All groups, sub-groups and tests are derived from BS9400 unless otherwise indicated. A3a and A4a tests are carried out at 25C.

C			A

Rel 1 standard. 20 year hermetic.

Each lot
Sub-groups:

A1	:	Visual inspection.
A2	:	Verification of device type.
A3a and A4a	:	Static and dynamic tests at 25 C.
A3 and A4	:	Static and dynamic tests at 125 and -55C.

B1	:	Dimensions.
B2a	:	Solderability.
B2b	:	Rapid temp change (10 cycles) and fine/gross leak.
B3	:	Terminal robustness.
B6	:	Acceleration.
B7	:	160hr endurance at 125 C.

Every 3 months
Sub-groups:

C3	:	Vibration, shock and 28 cycles damp heat.
C5	:	2000hr endurance at 125 C.

(A3a and A4a end-point tests are carried out after B2b, B7, C3 and C5).

General: All groups, sub-groups and tests are derived from BS9400 unless otherwise indicated. A3a and A4a tests are carried out at 25C.

D [ ] [ ] A

Rel 2 type A, 20 year hermetic.

Each lot
Sub-groups:
A1 : Visual inspection.
A2 : Verification of device type.
A3a and A4a : Static and dynamic tests at 25 C.

B1 : Dimensions.
B2a : Solderability.
B2b : Rapid temp change (5 cycles) and fine/gross leak.
B3 : Terminal robustness.
B6 : Acceleration.
B7 : 160hr endurance at 125 C.

Every 3 months
Sub-groups:
C3 : Vibration, shock and 28 cycles damp heat.
C4a : Static and dynamic tests at max specified temp.
C4b : Static and dynamic tests at min specified temp.
C5 : 2000hr endurance at 125 C.

(A3a and A4a end-point tests are carried out after B2b, B7, C3 and C5).

General: All groups, sub-groups and tests are derived from BS9400 unless otherwise indicated. A3a and A4a tests are carried out at 25C. A3a and A4a end-point tests are carried out after B2, B2b, B7, C3, C4a, C4b, C4d, C5, D3, D4, D5, D6, D8, D9, D10 and D11 when appropriate. For plastic options, B7b and C4d (high temp and humidity) tests are covered generically according to GPS/MEDL spec ref AG130.

E			A

Rel 3 type B, 10 year hermetic.

Each lot
Sub-groups:

A1	:	Visual inspection.
A2	:	Verification of device type.
A3a and A4a	:	Static and dynamic tests at 25 C.

B1	:	Dimensions.
B2a	:	Solderability.
B2b	:	Rapid temp change (5 cycles) and fine/gross leak.
B3	:	Terminal robustness.
B6	:	Acceleration.
B7	:	160hr endurance at 125 C.

Every 6 months
Sub groups:

C3	:	Vibration, shock and 28 cycles damp heat.
C4a	:	Static and dynamic tests at max specified temp.
C4b	:	Static and dynamic tests at min specified temp.
C5	:	1000hr endurance at 125 C.

E B

Rel 4 type B, 10 year plastic.

Each lot
Sub-groups:
A1 : Visual inspection.
A2 : Verification of device type.
A3a and A4a : Static and dynamic tests at 25 C.

B1 : Dimensions.
B2a : Solderability.
B2b : Rapid change of temperature (10 cycles).
B3 : Terminal robustness.
B7 : 160hr (85C/85%) high temp and humidity (generic).

Every 6 months
Sub-groups:
C4a : Static and dynamic tests at max specified temp.
C4b : Static and dynamic tests at min specified temp.
C4c : 200 cycles rapid change of temperature.
C4d : 500hr (85C/85%) high temp and humidity (generic).
C5 : 1000hr endurance at 125 C.

Every year
Sub-groups:
D11 : 500hrs storage (125C) + 10 cyls rapid temp change.

E C

Rel 5 type A, 20 year plastic.

Each lot
Sub-groups:
A1 : Visual inspection.
A2 : Verification of device type.
A3a and A4a : Static and dynamic tests at 25 C.

B1 : Dimensions.
B2a : Solderability.
B2b : Rapid change of temperature (10 cycles).
B3 : Terminal robustness.
B7 : 160hr (85C/85%) high temp and humidity (generic).

Every 6 months
Sub-groups:
C4a : Static and dynamic tests at max specified temp.
C4b : Static and dynamic tests at min specified temp.
C4c : 400 cycles rapid change of temperature.
C4d : 1000hr (85C/85%) high temp and humidity (generic).
C5 : 2000hr endurance at 125 C.

Every year
Sub-groups:
D11 : 1000hrs storage (125C) + 10 cyls rapid temp change

E D

Rel P STACK plastic.

Each lot
Sub-groups:
A1 : Visual inspection.
A2 : Verification of device type.
A3 and A4 : Static and dynamic tests at specified low and high temp limits.

B1 : Dimensions.
B2a : Solderability.
B2b : Rapid change of temperature (20 cycles).
B7 : 160hr endurance.

Every year
Sub-groups:
D3 : Permanence of mark.
D4 : Rapid temp change (10cys) + thermal shock (15cys)
D5 : 1000hr (85C/85%) high temp and humidity.
D6 : 2500hr endurance.
D7 : Rapid change of temp (1000 cycles).
D8 : Resistance to solder heat (LCC packages only).
D9 : Terminal robustness.
D10 : 1000hrs high temp storage.
D11 : Flammability.

E E

Rel C STACK hermetic.

Each lot
Sub-groups:
A1 : Visual inspection.
A2 : Verification of device type.
A3 and A4 : Static and dynamic tests at specified low and high temp limits.

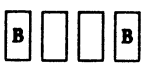
B1 : Dimensions.
B2a : Solderability.
B2b : Rapid temp change (20 cycles) and fine/gross leak.
B7 : 160hr endurance.

Every year
Sub-groups:
D3 : Vibration, mechanical shock, acceleration and fine and gross leak.
D5 : 2500hr endurance.
D6 : Permanence of mark.
D7 : Thermal shock (15 cycles).
D8 : Resistance to solder heat (LCC packages only).
D9 : Terminal robustness.
D10 : 1000hrs high temp storage.
D11 : Internal water vapour to MIL method 1018.

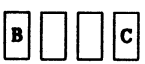
Class B QA/QCI Options Page 1

General: All Class B options include the supply of a certificate of conformance and a test performance report.
All group and sub-group names refer to MIL STD 883 method 5005 for class B. Good devices required for group C, D3 and D4 tests are shipped with the order. All other devices used for QCI are scrapped. For LCC packages, group D7 tests are not performed. "Devices required" indicates the number of devices over and above the quantity ordered that will be required for QCI.

No QCI required. Lot/traveller verification only.
Devices required : 0

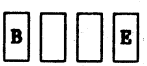


Group A tests to MIL STD 883 method 5005, table 1.
Devices required : 0



Group A tests to MIL STD 883 method 5005, table 1.
Group B2a, B3 and B5a tests to MIL STD 883 method 5005.
Devices required : 4

Group A tests to MIL STD 883 method 5005, table 1.
Group B2a, B3 and B5a tests to MIL STD 883 method 5005.
Supply of generic data for group C and D tests.
Devices required : 4



Group A tests to MIL STD 883 method 5005, table 1.
Group B2a, B3 and B5a tests to MIL STD 883 method 5005.
Group Ca and Cb tests to MIL STD 883 (using group A test endpoint parameters at 25C, 125 and -55C with read and record data).
Devices required : 49

Group A tests to MIL STD 883 method 5005, table 1.
Group B2a, B3 and B5a tests to MIL STD 883 method 5005.
Group Ca and Cb tests to MIL STD 883 (using group A test endpoint parameters at 25C, 125C and -55C with read and record data).
Supply of generic data for group D tests.
Devices required : 49

B [ ] [ ] G

Group A tests to MIL STD 883 method 5005, table 1.
Group B2a, B3 and B5a tests to MIL STD 883 method 5005.
Group Ca and Cb tests to MIL STD 883 (using group A test endpoint parameters at 25C, 125C and -55C) with read and record data.
Group D1, D2a, D3a, D3b, D3c, D3d, D3e, D3f, D4a, D4b, D4c, D4d, D4e, D4f, D5a, D5b, D5c, D6, and D7 tests (using group A test endpoint parameters at 25C for D3 and D4 tests, with read and record data).
Devices required : 84

B [ ] [ ] H

No group A tests.
Group B2a, B3 and B5a tests to MIL STD 883 method 5005.
Devices required : 4

B [ ] [ ] I

No group A tests.
Group B2a, B3 and B5a tests to MIL STD 883 method 5005.
Supply of generic data for group C and D tests.
Devices required : 4

B [ ] [ ] J

No group A tests.
Group B2a, B3 and B5a tests to MIL STD 883 method 5005.
Group Ca and Cb tests to MIL STD 883 (using group A test endpoint parameters at 25C, 125 and -55C with read and record data).
Devices required : 49

B [ ] [ ] K

No group A tests.
Group B2a, B3 and B5a tests to MIL STD 883 method 5005.
Group Ca and Cb tests to MIL STD 883 (using group A test endpoint parameters at 25C, 125C and -55C with read and record data).
Supply of generic data for group D tests.
Devices required : 49

B [ ] [ ] L

No group A tests.
Group B2a, B3 and B5a tests to MIL STD 883 method 5005.
Group Ca and Cb tests to MIL STD 883 (using group A test endpoint parameters at 25C, 125C and -55C) with read and record data.
Group D1, D2a, D3a, D3b, D3c, D3d, D3e, D3f, D4a, D4b, D4c, D4d, D4e, D4f, D5a, D5b, D5c, D6, and D7 tests (using group A test endpoint parameters at 25C for D3 and D4 tests, with read and record data).
Devices required : 84

Class S QA/QCI Options Page 1

General: All options include the supply of a datapack containing the following:

Certificate of Conformance
SEM reports
Test Performance report
Radiographic report
PDA calculations
Failed components list
Radiation test results (where appropriate)
Lead certificate
List of devices shipped
List of devices retained
QCI report
Electrical read and record data (in paper or ASCII file form)
Appendix containing any other information (eg concessions)

"Devices required" indicates the number of devices over and above the quantity ordered that will be required for QCI assuming a single device type (QCI quantities may be lotted up across members of a structurally similar chipset if required).

For LCC packages, group D7 tests are not performed.

Options A to O cater for MILSTD S requirements.

For MILSTD S options, good devices required for B5,B6,D3 and D4 tests are shipped with the order, other QCI devices are scrapped. Group B tests listed refer to MILSTD 883 method 5005, table 11a for class S.

Options P to R cater for ESA9000 requirements.

For ESA9000 options, end point electrical tests for LAT1 and LAT2 are performed at 25C.
Good devices required for LAT1 and LAT2 are shipped with the order. LAT3 electrical verification units are shipped as flight quality units. Destructive test units are scrapped.

MILSTD/S Options

S _ _ A	No QCI required. Lot/traveller verification only. Devices required : 0
S _ _ B	Group A tests to MILSTD 883 method 5005, table 1. Devices required : 0

S C

Group A tests to MILSTD 883 method 5005, table 1.
Generic data supplied for group B and D tests.
Devices required : 0

S D

No group A tests.
Group B1a, B2a, B2b, B2c, B2d, B3, B4a, B4b, B5a, B5b, B5c, B6a, B6b, B6c, B6d, B6e tests to MILSTD 883 method 5005.
Endpoint parameters for B5 are the group A requirements at 25, 125 and -55C with read and record data.
Endpoint parameters for B6 are the group A requirements at 25C with read and record data.
Devices required : 64

S E

No group A tests.
Group B1a, B2a, B2b, B2c, B2d, B3, B4a, B4b, B5a, B5b, B5c, B6a, B6b, B6c, B6d, B6e tests to MILSTD 883 method 5005.
Endpoint parameters for B5 are the group A requirements at 25, 125 and -55C with read and record data.
Endpoint parameters for B6 are the group A requirements at 25C with read and record data.
Generic data supplied for group D tests.
Devices required : 64

S F

Group A tests to MILSTD 883 method 5005, table 1.
Group B1a, B2a, B2b, B2c, B2d, B3, B4a, B4b, B5b, B5c, B6b, B6c, B6d, B6e tests to MILSTD 883 method 5005.
Endpoint parameters for B5 are the group A requirements at 25, 125 and -55C with read and record data.
Endpoint parameters for B6 are the group A requirements at 25C with read and record data.
Generic data supplied for group D tests.
Devices required : 64

S G

Group A tests to MILSTD 883 method 5005, table 1.
Group B2a, B2b, B2c, B2d, B3, B5b, B5c, B6b, B6c, B6d and B6e tests to MILSTD 883 method 5005.
Group D1, D2a, D3a, D3b, D3c, D3d, D3e, D3f, D4a, D4b, D4c, D4d, D4e, D4f, D5a, D5b, D5c, D6 and D7 tests to MILSTD 883 method 5005. (One fail allowed for D6).
Endpoint parameters for B5 are the group A requirements at 25, 125 and -55C with read and record data.
Endpoint parameters for B6 and D3/D4 are the group A requirements at 25C with read and record data.
Devices required : 99

S [ ] [ ] H

No group A tests.
Group B2a, B2b, B2c, B2d, B3, B5a, B5b, B5c, B6a, B6b, B6c, B6d and B6e tests to MILSTD 883 method 5005.
Group D1, D2a, D3a, D3b, D3c, D3d, D3e, D3f, D4a, D4b, D4c, D4d, D4e, D4f, D5a, D5b, D5c, D6 and D7 tests to MILSTD 883 method 5005. (One fail allowed for D6).
Endpoint parameters for B5 are the group A requirements at 25, 125 and -55C with read and record data.
Endpoint parameters for B6 and D3/D4 are the group A requirements at 25C with read and record data.
Devices required : 99

S [ ] [ ] I

Group A tests to MILSTD 883 method 5005, table 1.
Group B2a, B2b, B2c, B2d, B3, B5b, B5c, B6b, B6c, B6d and B6e tests to MILSTD 883 method 5005.
Group D1, D2a, D3a, D3b, D3c, D3d, D3e, D3f, D4a, D4b, D4c, D4d, D4e, D4f, D6 and D7 tests to MILSTD 883 method 5005. (One fail allowed for D6).
Endpoint parameters for B5 are the group A requirements at 25, 125 and -55C with read and record data.
Endpoint parameters for B6 and D3/D4 are the group A requirements at 25C with read and record data.
Devices required : 84

S [ ] [ ] J

Group A tests to MILSTD 883 method 5005, table 1.
Group B1a, B2a, B2b, B2c, B2d, B3, B4a, B4b, B5b, B5c tests to MILSTD 883 method 5005.
Endpoint parameters for B5 are the group A requirements at 25, 125 and -55C with read and record data.
Devices required : 49

S [ ] [ ] K

Group A tests to MILSTD 883 method 5005, table 1.
Group B1a, B2a, B2b, B2c, B2d, B3, B4a, B4b, B5b, B5c tests to MILSTD 883 method 5005.
Endpoint parameters for B5 are the group A requirements at 25, 125 and -55C with read and record data.
Generic data supplied for group D tests.
Devices required : 49

S [ ] [ ] L

No group A tests.
Group B1a, B2a, B2b, B2c, B2d, B3, B4a, B4b, B5a, B5b, B5c tests to MILSTD 883 method 5005.
Endpoint parameters for B5 are the group A requirements at 25, 125 and -55C with read and record data.
Devices required : 49

S M

No group A tests.
Group B1a, B2a, B2b, B2c, B2d, B3, B4a, B4b, B5a, B5b, and B5c tests to MILSTD 883 method 5005.
Endpoint parameters for B5 are the group A requirements at 25, 125 and -55C with read and record data.
Generic data supplied for group D tests.
Devices required : 49

S N

Group A tests to MILSTD 883 method 5005, table 1.
Group B2a, B3, B4a, B4b, B5b, B5c tests to MILSTD 883 method 5005.
Group D3a, D3b, D3d, D3e, D3f, D4a, D4b, D4c, D4d, XRAY D4f and D6 tests to MILSTD 883 method 5005.
Endpoint parameters for B5c and A groups are those from final electrical test at 25, 125 and -55C with read and record data. Endpoint parameters for D3f are the group A requirements at 25C. B5b includes read and record data at 240 and 500 hours.
Devices required : 28

S O

Group A tests to MILSTD 883 method 5005, table 1.
Group B1a, B2a, B3, B4a, B5b, B5c tests to MILSTD 883 method 5005.
Group D3a, D3b, D3c, D3d, D3e, D3f tests to MILSTD 883 method 5005.
Endpoint parameters for D3f and D5c are the group A requirements at 25C.
Devices required : 7

ESA9000 Options

S [ ] [ ] P

LAT1 : Tests carried out as follows:

LEVEL1	LEVEL2	LEVEL3
Shock	Operating life	25C test
Vibration	Test (during)	125C test
Acceleration	External visual	-55C test
Mark permanence		External visual
Thermal shock		Solderability
Moisture		Term strength
Seal test		
25C electrical		
External visual		

(Devices required : 56)

S [ ] [ ] Q

LAT2 : Tests carried out as follows:

LEVEL1	LEVEL2	LEVEL3
No tests	Operating life	25C test
	Test (during)	125C test
	External visual	-55C test
		External visual
		Solderability
		Term strength

(Devices required : 40)

S [ ] [ ] R

LAT3 : Tests carried out as follows:

LEVEL1	LEVEL2	LEVEL3
No tests	No tests	25C test
		125C test
		-55C test
		External visual
		Solderability
		Term strength

(Devices required : 25)

section 10
LOCATIONS

Worldwide Locations

HEADQUARTERS OPERATIONS

UNITED KINGDOM — **Plessey Semiconductors Ltd.,** Cheney Manor, Swindon. Wiltshire SN2 2QW. United Kingdom. Tel: (0793) 518000, Tx: 449637, Fax: 0793 518411.

NORTH AMERICA — **Plessey Semiconductors,** Sequoia Research Park, 1500 Green Hills Road, Scotts Valley, California 95066, United States of America. Tel:(408) 438 2900, ITT Telex: 4940840, Fax: (408) 438 5576.

CUSTOMER SERVICE CENTRES

FRANCE and BENELUX — **Plessey Semiconductors,** Z.A. Courtaboeuf, Miniparc-6, Avenue des Andes, Bat. 2-BP 142, 91944 Les Ulis Cedex A. Tel: (1) 64 46 23 45, Fax: (1) 64 46 06 07, Tlx: 602 858 F.

GERMANY (FDR), AUSTRIA and SWITZERLAND — **Plessey GmbH,** Ungererstraße 129, 8000 Munchen 40. Tel: 089/36 0906-0, Fax: 089/360906-55, Tlx: 523980.

ITALY — **Plessey SpA,** Viale Certosa, 49 20149 Milano. Tel: (02) 33 00 10 44/55, Fax: (GR3) 31 69 04, Tlx: 331347.

NORTH AMERICA — **Plessey Semiconductors,** Sequoia Research Park, 1500 Green Hills Road, Scotts Valley, California 95066, United States of America. Tel: (408) 438 2900, ITT Telex: 4940840, Fax: (408) 438 7023.

SOUTH EAST ASIA — **Plessey Semiconductors Singapore Pte. Ltd.,** 152 Beach Road, #04-05 Gateway East, Singapore 0718. Tel: 2919291, Fax: 2916455.

UNITED KINGDOM and SCANDINAVIA — **Plessey Semiconductors Ltd,** Unit 1,Crompton Road,Groundwell Industrial Estate, Swindon, Wilts.SN2 5AY. Tel. (0793) 518510, Tx: 444410, Fax: (0793) 518582.

WORLD-WIDE AGENTS

AUSTRALIA and NEW ZEALAND — **Plessey Semiconductors Australia Pty Ltd.,** P.O.Box 2, Villawood, NSW 2163. Tel: 2 72 0133, Tx: AA20384, Fax: 2 7260669.

EASTERN EUROPE — **CTL Empexion Ltd.,** Falcon House, 19 Deer Park Road, London SW19 3WX Tel: (081) 543 0911, Tx: 928472, Fax: (081) 540 0034.

GREECE — **Impel Ltd.,** 30 Rodon Str, Korydallos, Piraeus, Greece. Tel: 010 30 1 49 67815, Tlx: 213835, Fax: 01 49 54041.

JAPAN — **Cornes & Company Ltd.,** Maruzen Building, 2-3-10 Nihonbashi, Chuo-ku, Tokyo 103.Tel: 3 272 5771, Tx: 24874, Fax: 3 271 1479.
Cornes & Company Ltd., 1-Chome Nishihonmachi, Nishi-Ku, Osaka 550. Tel: 6 532 1012, Tx: 525-4496, Fax: 6 541-8850.
Microtek Inc., Itoh Bldg, 7-9-17 Nishishinijuku, Tokyo 160. Tel: 3 371 1811, Tx: 27466, Fax: 3 369 5623.

HONG KONG — **YES Products Ltd.,** Block E, 15/F Golden Bear Industrial Centre, 66-82 Chaiwan Kolk Street,Tsuen Wan, N.T. Hong Kong. Tel: 4442416, Tx: 36590, Fax: 4993065.

KOREA — **KML Corporation,** 3rd Floor, Bang Bae Station Building, 981-15 Bang Bae, 3-Dong Shucho-Gu, Seoul, Korea, CPO Box 7981. Tel: 2 588 2011/6, Tx: K25981, Fax: 2 588 2017.

MALAYSIA — **Plessey Malaysia,** 1602 Pernas International Building, Jalan Sultan Ismail, Kuala Lumpur 50250. Tel: 3 2611477, Tlx: 30918, Fax: 3 2613385.

SCANDINAVIA

Denmark — **Scansupply A/S,** 18-20 Nannasgade, DK-2200 Copenhagen N. Tel: 31 83 50 90, Tx: 19037, Fax: 31 83 25 40.
Scansupply Randers, Østervang 17, Øbjerregrav 8900, Randers. Tel: 8645440, Fax: 86454640.

Finland — **Oy Ferrado AB,** P.O.Box 54, SF-00381 Helsinki 38. Tel: 98 0550 002, Tx: 122214, Fax: 98 0551 117.

Norway — **Skandinavisk Elektronikk A/S,** Ostre Aker Vei 99, 0596 Oslo. Tel: 2 64 11 50, Tx: 71963, Fax: 2 643443.

Sweden — **Swedesupply AB,** Vastra Vagen 5, P.O.Box 1028, 171 21 Solna. Tel: 08735 81 30, Tx: 13435, Fax: 0883 9033.

SPAIN — **Anatronic SA,** Avda de Valladolid 27, 28008 Madrid. Tel: 91 542 4455, Tx: 47397, Fax: 91 2486975.

TAIWAN — **Artistex International Inc.,** B2, 11th Floor, 126, Nanking East Road, Section 4, Taipei, Taiwan, Republic of China. Tel: 2 7526330, Tx: 27113, Fax: 2 721 5446.

THAILAND — **Westech Electronics Co. Ltd,** 77/113 Moo Ban Kitikorn, Ladprao Soi 3, Ladprao Road, Ladyao, Jatujak, Bangkok 10900, Thailand Tel: 2 5125531, Fax: 2 2365949.

TURKEY — **Empa,** Refik Saydam Cad No.89 Kat 5, 80050 Sishane, Istanbul, Turkey. Tel: 0 143 621213, Fax: 0 143 6549.

WORLD-WIDE DISTRIBUTORS

AUSTRALIA — **Plessey Semiconductors Australia Pty Ltd.,** P.O.Box 2, Villawood, New South Wales 2163. Tel: 2 720133, Tx: AA20384, Fax: 2 7260669.

AUSTRIA — **Moor-Lackner GesmbH,**Elektrotechnik Eiektronik Datentechnik, A-1232 Wien/Austria, Lamezanstrasse 10. Tel: 222 610620, Tx: 135701, Fax: 222 61062151.

BELGIUM — **Heynen,** De Koelen 6, B-3530 Koutmalen. Tel: 011/52 57 57, Tlx: 39047, Fax: 011/52 57 77.

FRANCE — **Mateleco:**
Ile de France, 66 Avenue Augustin Dumont, 92240 Malakoff. Tel: 010 33 1 46 57 70 55, Tx: 203436.
Rhone-Alpes, 2, Rue Emile Zola, 38130 Echirolles. Tel: 010 33 76 40 38 33, Tx: 980837.
ICC:
Bordeaux, Rue de la Source, 33170 Gradignan. Tel: 56 31 17 17, Tx: 541539, Fax: 61 48 11 25.
Clermont-Ferrand, 2 bis, Avenue Fonmaure, 63400 Chamalieres. Tel: 73 36 71 41, Tx: 990928.
Z.A. Artizanord 11, 13015 Marseille. Tel: 91 03 12 12, Tx: 441313.
78, Chemin Lanusse, 31200 Toulouse. Tel: 61 26 14 10, Tx: 520897.
CGE Composants S.A:
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UNITED STATES OF AMERICA	**Plessey Semiconductors,** Sequoia Research Park, 1500 Green Hills Road, Scotts Valley, California 95066. Tel: (408) 438 2900 ITT Telex: 4940840 Fax: (408) 438-5576.
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Centre/Pays-de-Loire, Allee de la Detente, 86360 Chasseneuil du Poitou. Tel: 49 52 88 88, Tx: 791525 F.
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Aquitech:
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Aquitech, 25 rue de la Chalotais 35000 Rennes, Tel: 99 78 31 32, Fax: 99 79 21 80
Aquitech, 2 rue Alexis de Tooqueville 92189 Antony, Tel: (1) 40 96 94 94, Tx: 550529, Fax: (1) 40 96 93 00

Rhonalco, 3 Rue Berthelot, 69627 Villeurbanne, Tel: 33 78 53 00 25, Tx: 380284, Fax: 33 72 34 67 72.

GERMANY(FDR)
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Astronic GmbH, Gruenwalderweg 30, 8024 Deisenhofen. Tel: 089 6130303, Tx: 5216187, Fax: 089 6131668.
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SWITZERLAND
Basix fuer Electronik AG, Hardturmstr 181, CH-8010 Zurich Tel: 01 2761111, Tlx: 822966, Fax: 01 2761199
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UK EXPORT

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GEC Plessey Semiconductors

Publication No. S00000FDB Issue 1 January 1991

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